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Development of SALSAS ASIC

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EPIC Collaboration meeting

06/05/2026

Introduction

ASIC Specifications

Interfaces

Status and next steps

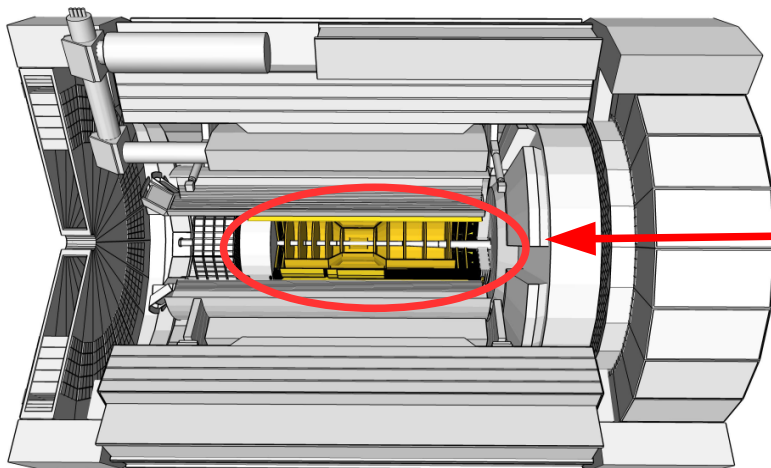
ASIC final production and tests

Documentation

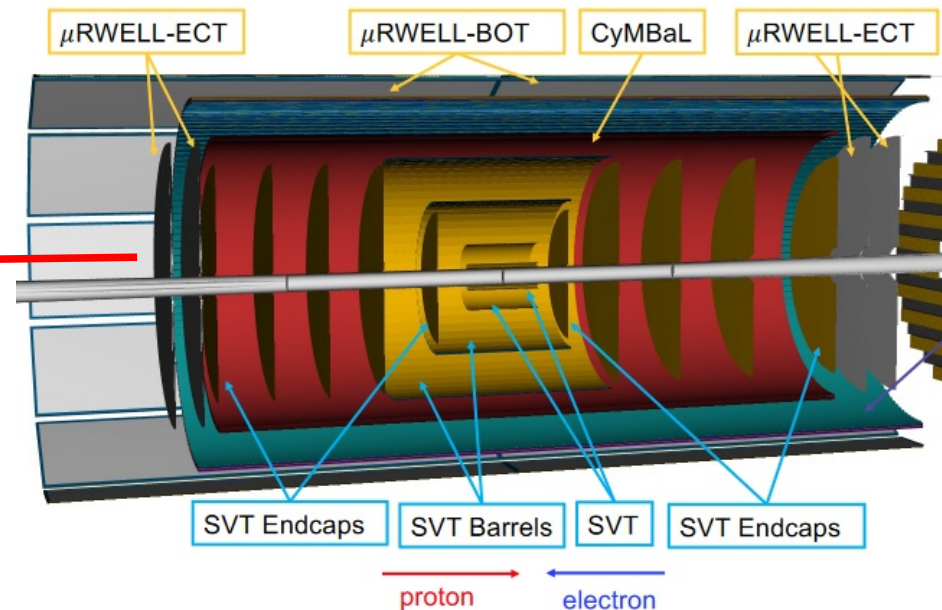
MPGD detectors foreseen in EPIC

- Cylindrical Micromegas barrel layer (CyMBaL) → ~36 k.channels
- μ RWell barrel outer tracker (μ RWell-BOT) → ~100 k.channels
- μ RWell end cap tracker (μ RWell-ECT) → ~32 k.channels
- Same readout ASIC to read all MPGD trackers → **SALSA**

EPIC detector



Central trackers





■ Motivations of the project

- New versatile multi-channel readout chip for the EIC project and beyond
 - adapted to streaming readout DAQs
 - for MPGD trackers and also TPC, photon detectors,...
 - a base of future developments for other detector kinds, with specific constraints
- Front-end ASIC integrating digitization and first data processing
- Wide specifications, to adapt to a large range of MPGD applications: input capacitance, peaking times, gain ranges, input rates, ADC precision and rates, DSP for data reduction, radiation hardness

■ Actors of the projects

- Sao Paulo University (USP): expertise in on-chip ADC and digital processing, developed SAMPA
- CEA Saclay IRFU: expertise in low-noise radiation-hard generic front-ends and in low-jitter PLL, developed MPGD front-end ASICs (AFTER, AGET, DREAM,...) and other kinds (SAMPIC)
- Large amount of complementary competences to collaborate on a common versatile front-end chip including digitization and digital processing
- 10 participants (engineers, physicists) at IRFU (FTE ~4), and 10 at USP (FTE ~3)



Goals of the reviews:

Provide a comprehensive assessment of the ASICs and Discrete Readout from design to production

- **Specifications & Requirements - frontend, processing, interfaces, power and packaging (including form factors where applicable).**
- Digital Interfaces - commands & controls
- Status & Steps to Completion - with schedule and to include testing/validation with detectors
- Production Outlook - to include final production review, production timeline and QA/QC testing
- Documentation - Functionality (e.g. User's Manual/Spec sheets) and QA/QC Plans, and with planned availability for FEB final designs and Engineering Articles, bump/wire bonding.



■ Front-end stage vs EPIC MPGD needs

- 64 channels, based on CSA + shaper, each block can be by-passed
- Input capacitance range: optimized for 50-200 pF, reasonable gain up to 1 nF → **200 pF**
- Peaking times: 50-500 ns (8 values) → **100-200 ns**
- Gain ranges: 0-50, 0-250, 0-500 fC or 0-5 pC → **0-250 fC**
- Low noise level → **< 0.5 fC, to get factor 10 on signal / threshold**
- Input rates: up to 100 kHz/ch with fast CSA reset → **< 25-100 kHz**
- Reversible polarity (depends on detector type) → **negative**
- Embedded protection against ESD, detector spark protection requires external circuit
- 5 to 50 MS/s 12-bit ADC for each channel, > 10 effective bits

■ Digital processing

- Continuous or triggered readout
- DSP for parallel processing of digital samples from 64-channel ADCs
 - ▷ pedestal subtraction
 - ▷ common mode noise correction
 - ▷ baseline following algorithm
 - ▷ digital filtering
 - ▷ zero suppression
 - ▷ external trigger and calibration request management
- Packet building with sample or featured data, independently for each channel
- Feature extraction, time and amplitude, from samples
- Up to 4 output gigabit serial links → **1 link**



■ Interfaces

- 2 input interfaces: traditional (clock + sync inputs + I2C), unified (gigabit link with all signals)
- 4 gigabit data output links + 1 for trigger primitives generated by the ASIC

■ General characteristics

- Die size $\leq 1 \text{ cm}^2$, implemented on TSMC 65nm CMOS technology
- Expected power consumption $\sim 25\text{-}30 \text{ mW/channel}$ at 1.2V
- Radiation hardened (SEU, $> 300 \text{ Mrad}$, $> 10^{13} \text{ n}_{\text{eq}}/\text{cm}^2$) $\rightarrow \sim \mathbf{10 \text{ krad, } 10^{11} \text{ n}_{\text{eq}}/\text{cm}^2}$

■ Packaging

- Requirements: standard available package, optimal electronics performance (inductance, thermal, power), determined early to speed-up front-end board development
- $300 \times 300 \text{ }\mu\text{m}^2$ pitch C4 matrix on SALSA chip
- ~ 140 different signal expected $\rightarrow \sim 18 \times 18 \text{ mm}^2$ BGA package with 1 mm ball pitch (324 balls)
- Same BGA package with compatible pin-out for SALSA2 (32 ch) and SALSA3 (64 ch) prototypes



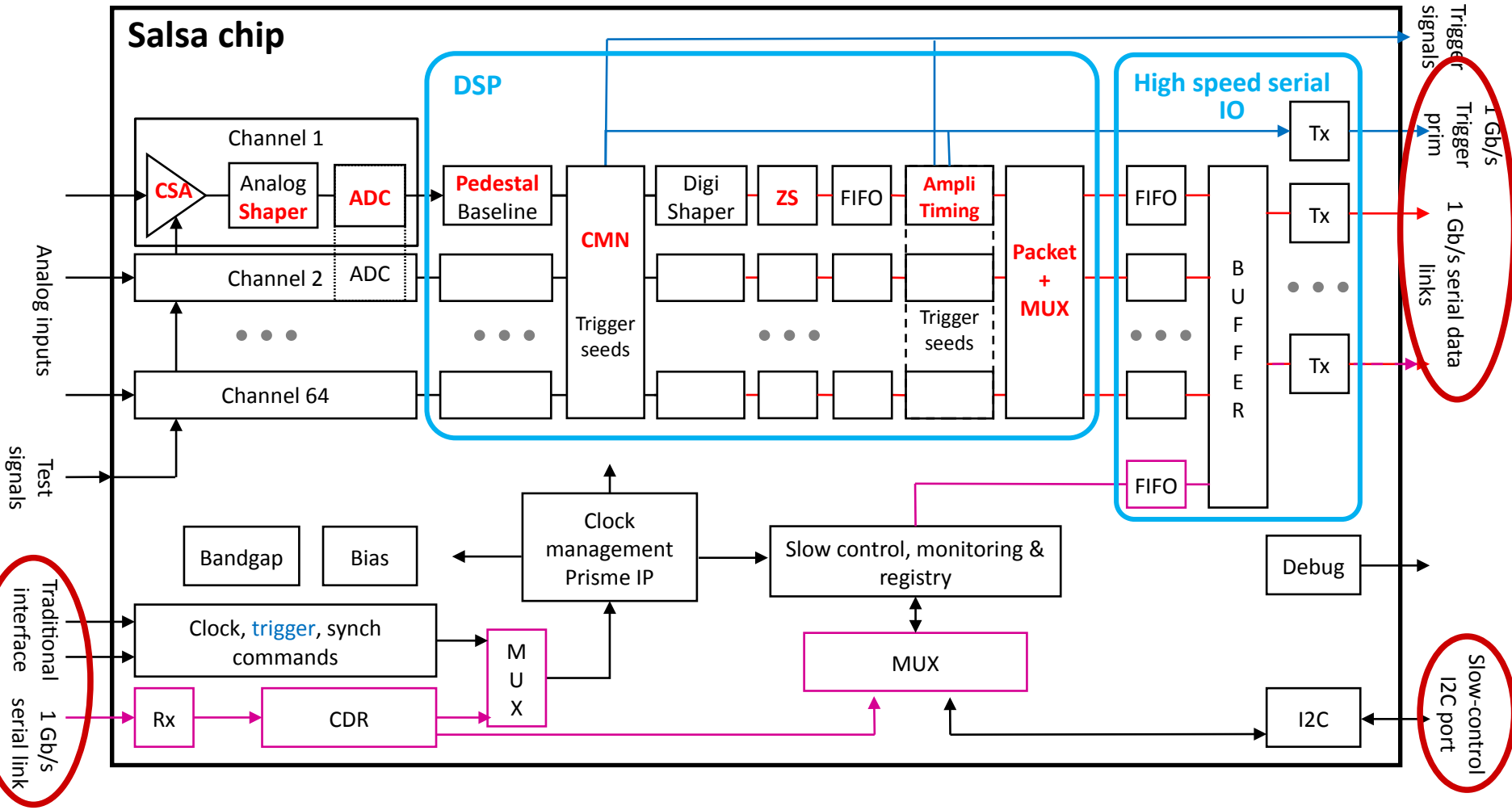
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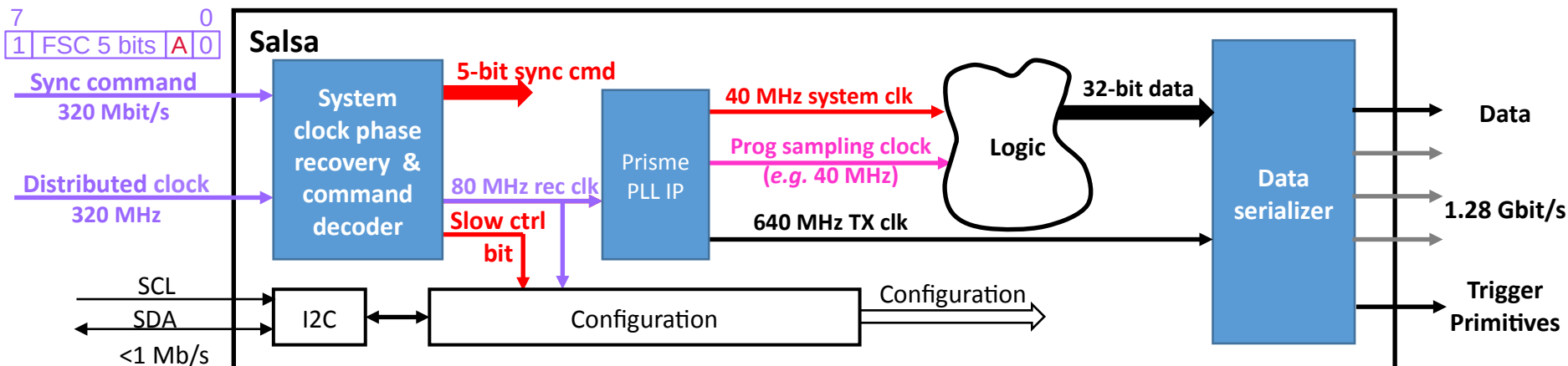
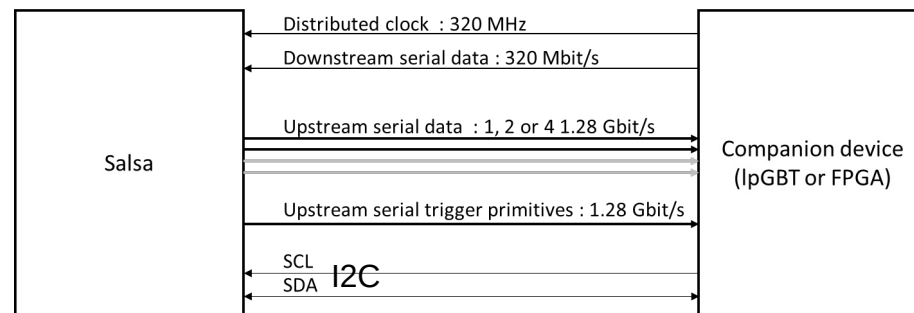
— Data path
— Trigger path





Traditional heterogeneous interface

- 1 differential input for clock
- 1 differential input for fast sync commands + asynchronous slow-control command input
- 1 SDA + SDC I2C I/O
- Up to 4 data links and a dedicated trigger primitive one
- Interface to be used with IpGBT and VTRX
- **Baseline for ePIC MPGD front-end boards**





List of SALSA fast synchronous commands

- Synchronization commands: Idle, **Ntf_T0Sync** (new timeframe), **Resync_acq**, Reset_TfCounter, Reset_TrigId
- Data flux: **Start, Stop, Pause, Resume**
- Data management: Ext trig, **Calib_1-4**, Pulse
- ASIC management: **Heartbeat, Monitor_1-4**, Latch_Stat
- Expert commands: Expert_mode, Reset_Cold, **Reset_Warm**, Reset_Stat, Reset_Dsp, Reset_Mem, Resync_TxPrimLnk, Resync_TxSecLnk, Resync_TxTrgLnk

Important fast commands for ePIC

- **Reset_Warm**, to prepare chip for a new run: reset all counters including time frame one, empty buffers, reset multiplexer, reset statistics, send info packet (configurable)
- **Start / Stop**, to manage readout: reset Tf counter, (de-)activate readout in DSP, send info packet (cfg.)
- **Ntf_T0Sync**, at new time frame: reset timestamp counters + statistics, increase time frame counter, sampling clock resync, send info packet (cfg.)
- **Pause / Resume**, to manage pauses in readout: (de-)activate readout in DSP
- **Resync_acq**, when ASICs no more synchronized: empty buffers, reset multiplexer
- **Calib_1-4**, to send calibration data: generate calibrations type 1 to 4
- **Monitor_1-4**, to send for information data: generate information packets type 1 to 4
- **Heartbeat**, to ask if ASIC still alive: generate heartbeat packet



Output links

- 4 gigabit links to transmit data
- 1, 2 or 4 can be activated in the same time
- 1 additional gigabit link to transmit trigger primitives

Output data

- Packets of 32-bit words, optionally extended with Reed-Solomon FEC (32+8 bits)
- Packet types: data (samples, signal features, calibrations), synchro, infos, trigger primitives
- Structure: header + data words + configurable additional words + trailers
- Information provided: type of packet, chip address, channel number, time frame number, timestamp, samples, flags, packet size, link ID, packet number in link

Example of
sample data
packet

	Bits	31					24	23					16	15			11		8	7			1	0								
R-S FEC	Header	P	1	1	Type of packet 3b	Chip address 3b	Channel number 6b					Time frame number 4b				Sampling timestamp 13b																
R-S FEC	Additional word	P	0	1	111	Trigger number 13b					Trigger timestamp (command clock) 13b																					
R-S FEC	Sample word	P	0	0	Flags 5b			Value of sample 1 12b					Value of sample 0 12b																			
R-S FEC	Sample word	P	0	0	Flags 5b			Value of sample 3 12b					Value of sample 2 12b																			
R-S FEC	Sample word	P	0	0	Flags 5b			Value of sample 5 12b					Value of sample 4 12b																			
R-S FEC	Trailer 1	P	1	0	Size of packet in number of words 6b			Infos 3b		Checksum or error word 8b				Link ID 3b		Packet number in link 9b																
R-S FEC	Trailer 2	P	1	0	Vertical parity word 29b																											



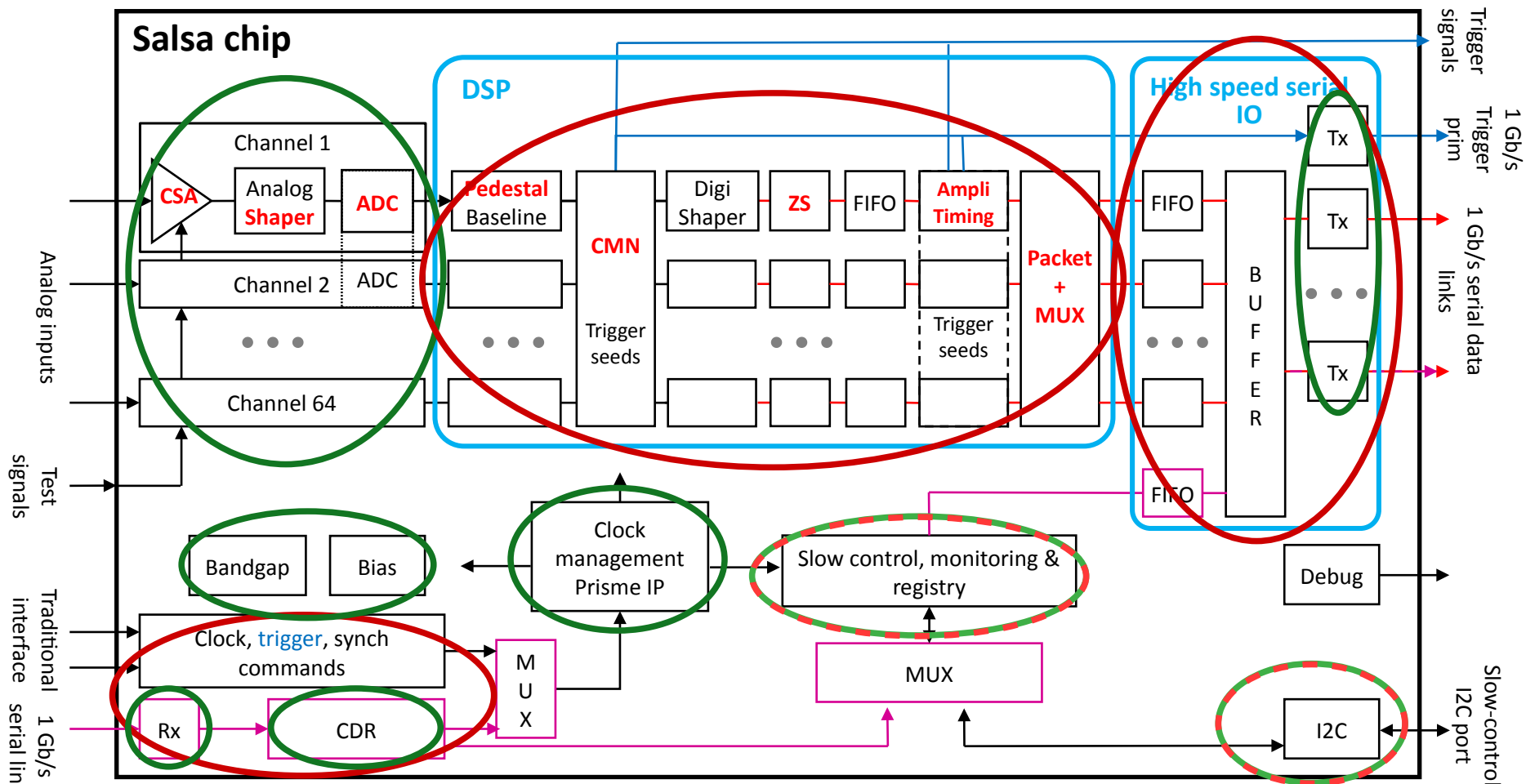
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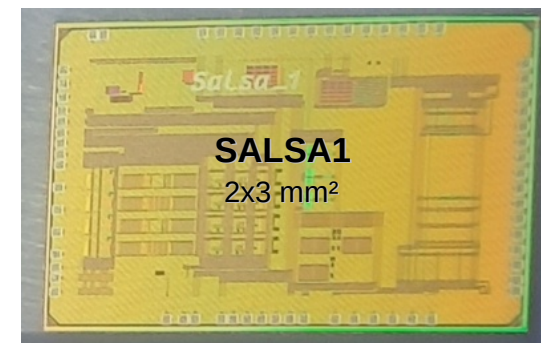
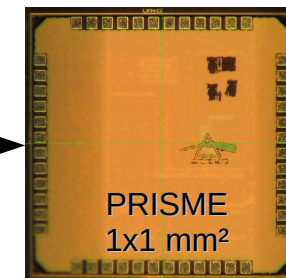
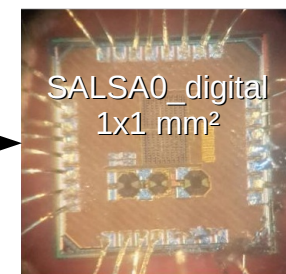
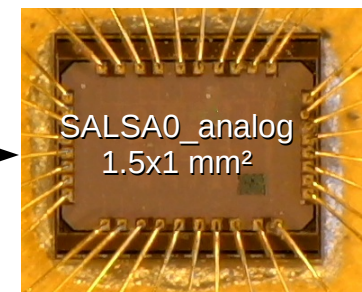


- Exists in prototype
- Development in progress
- Data path
- Trigger path

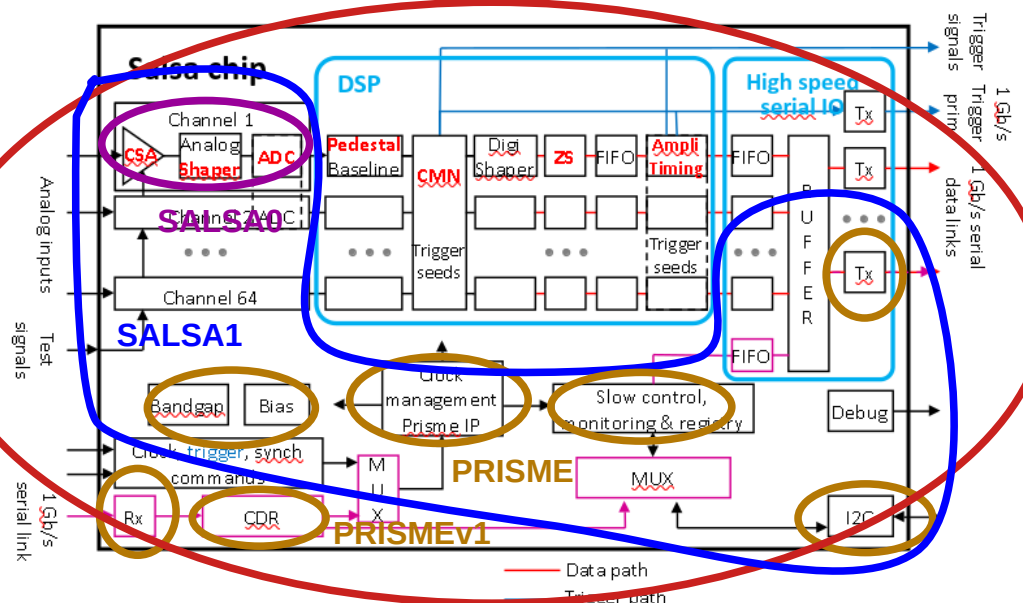


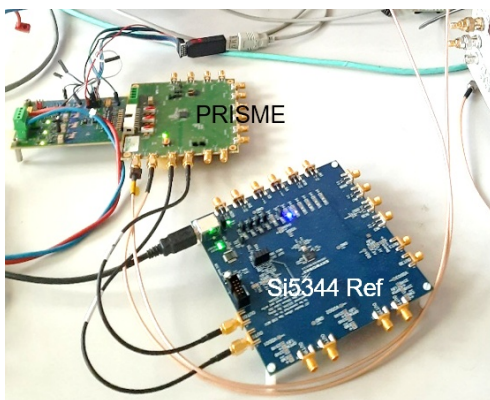
Steps of SALSA development

- 2022-23: **SALSA0** prototypes to study first designs
 - ▶ **SALSA0_analog** featuring 4 front-end channels
 - ▶ **SALSA0_digital** featuring an ADC block
- 2023: **PRISME** prototype of PLL block + general services (blocks partly from CERN)
- 2023-24: **SALSA1** prototype to test full front-end + ADC chains
- 2024-25: **PRISMEv1** prototype with updated PLL, including part of CDR
- 2024-27: **SALSA2** 32-channel prototype with partial DSP
- 2026-28: **SALSA3** prototype with 64 channels and final DSP

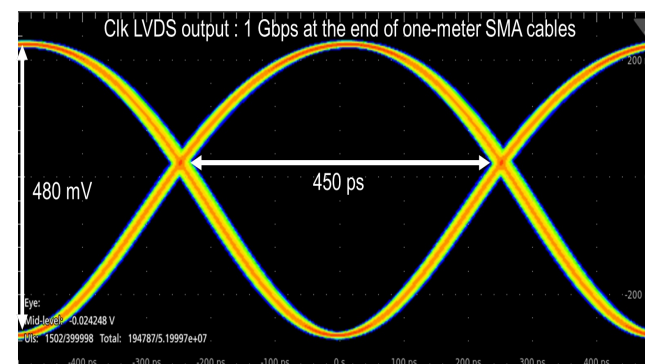
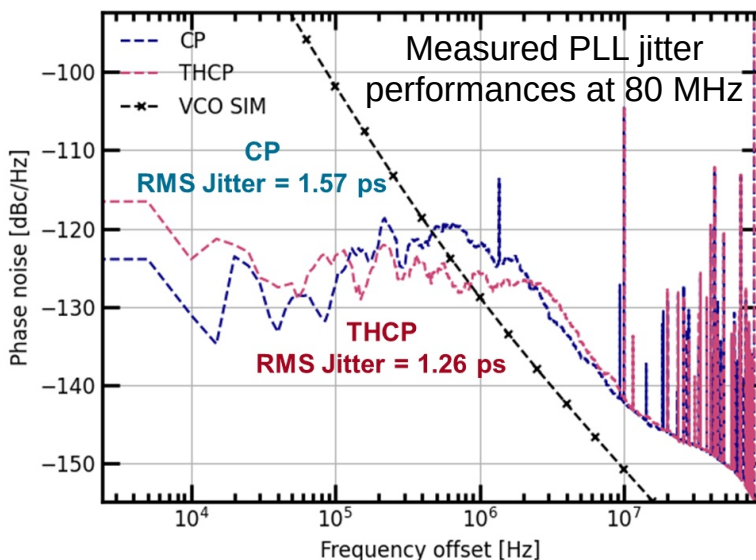


SALSA2
(most of DSP features)
SALSA3





PRISMEv1-PLL performance summary	
Technology	CMOS 65 nm
Power voltage	1.2V
Input reference frequency range	59-105 MHz
VCO frequency	1.18-2.1 GHz
Number of output clocks	4
Output frequency	Programmable fractions of VCO frequency, up to 1 GHz
Phase shifter step	< 500 ps
RMS jitter (Int. range)	1.26 ps @ 80 MHz Ref. clock (5 kHz-80 MHz)
PLL Power consumption	6.2 mW @ 1.6 GHz
PLL Active area	~0.07 mm ²
Radiation mitigation	TMR target :SEL free, TID up to 4 MGy

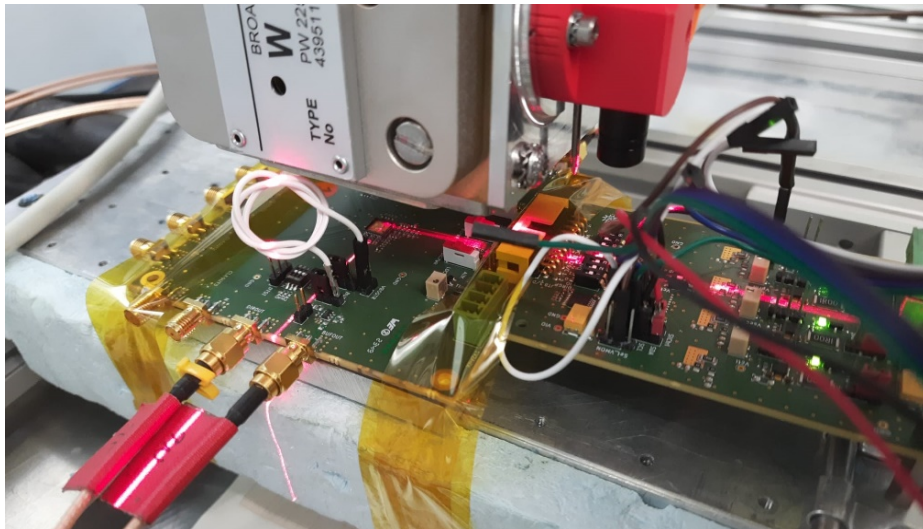


- Modern mixed digital-analog PLL architecture
- Improved PLL compared to PRISMEv0 (improved jitter)
- **Wide input range, with RMS jitter < 2 ps**

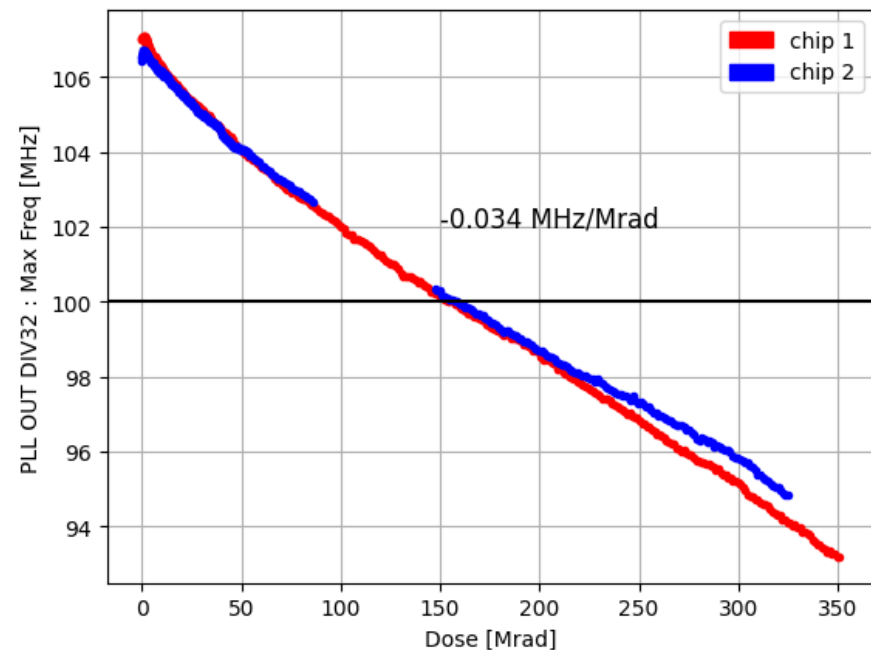
Tests of I/O high-speed links:
1 GHz LVDS output clock after 1m SMA cable, with widely open eye diagram

TID tests on PRISMEv0

- Goal: study evolution of frequency limit vs dose
- Results
 - decrease of frequency limit vs dose
 - nominal frequency reachable up to 150 Mrad
- **No impact for EPIC**, as much lower expected radiation level there (~10 krad)
- PRISMEv1 with improved radiation hardness design, TID tests foreseen as soon as a facility is available

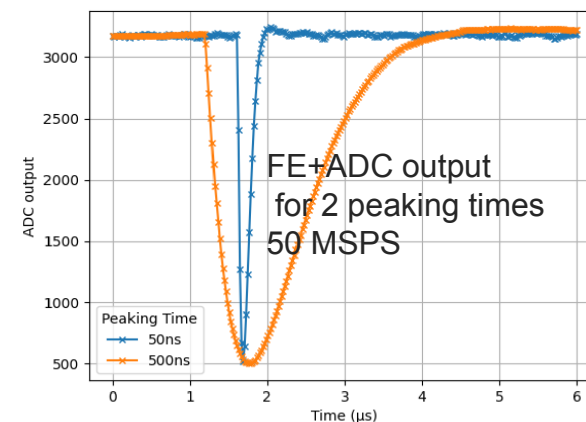
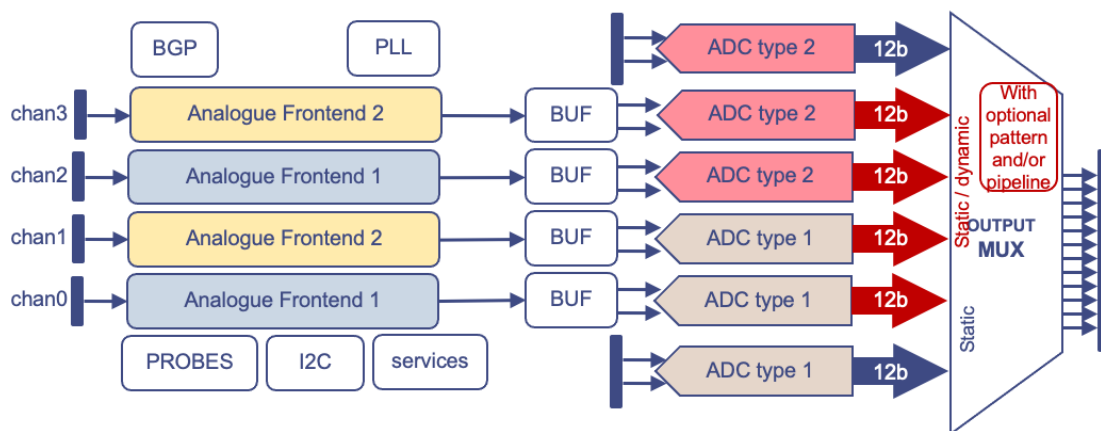


TID setup at CERN



SALSA1

- Goal: front-end + ADC validation
- 2 types of analog front-end (FE): SALSA0 FE + new FE with improved pole-zero cancellation
- 2 types of ADC: SAR (successive approximation) + SAR-TDC (hybrid architecture)



Test results

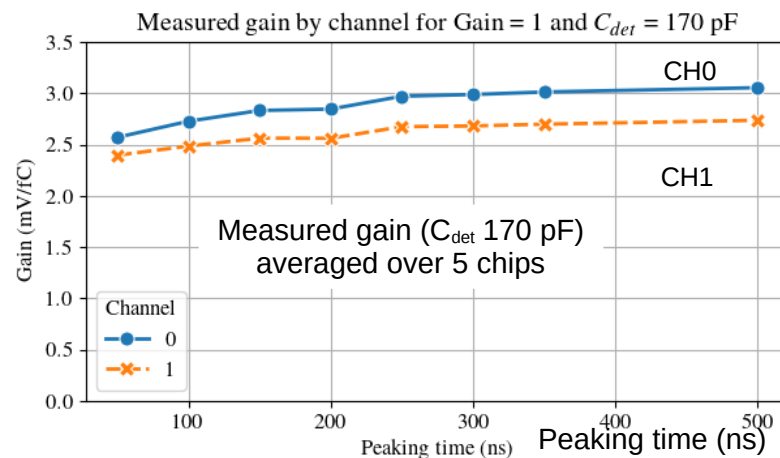
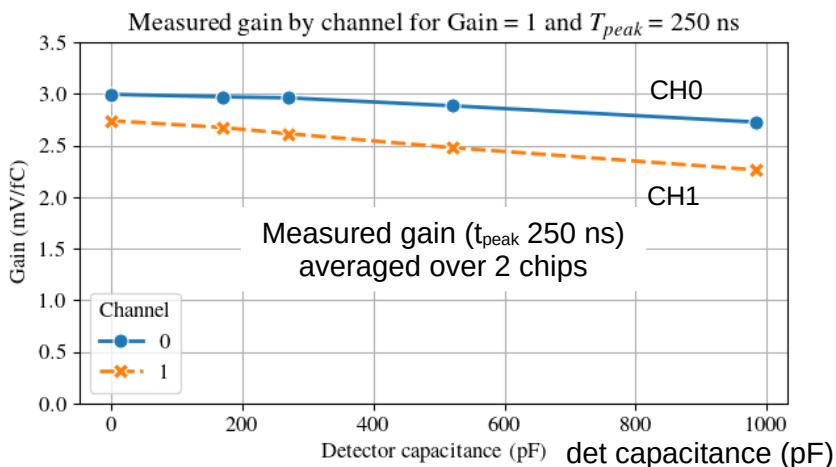
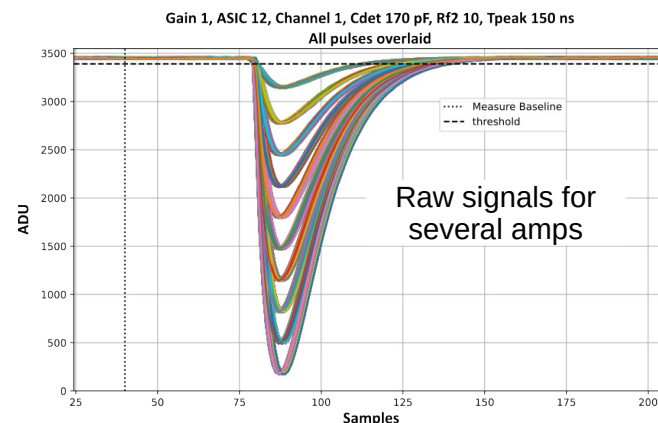
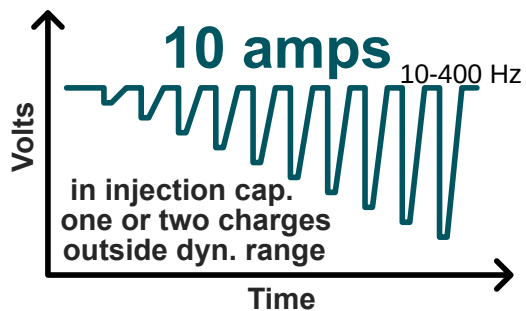
- All blocks tested: I2C, clock synthesis, static multiplexing, internal injection → all OK
- 5 chips measured, 2 for large input capacitances
- Results on performance measurements in next slides
- TID tests delayed due to CERN facility busy with BPOL issue, to be done soon
- SALSA1 main blocks ready to go to SALSA2





Gain measurements

- Step signals injected through 5pF capacitor, with slow return slope to zero
- 10 different amplitudes covering 120% dynamic range
- Good linearity, with residual < 20 ADC
- Stable gain up to 200pF detector capacitance

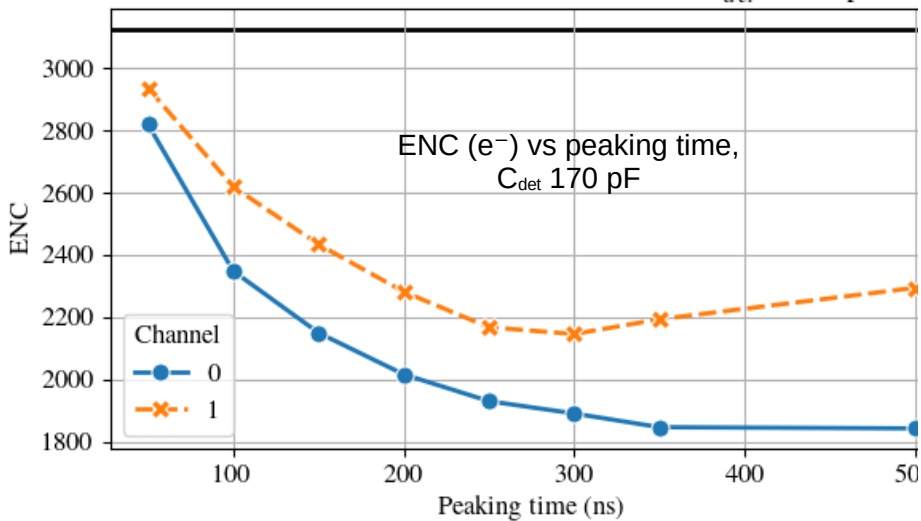




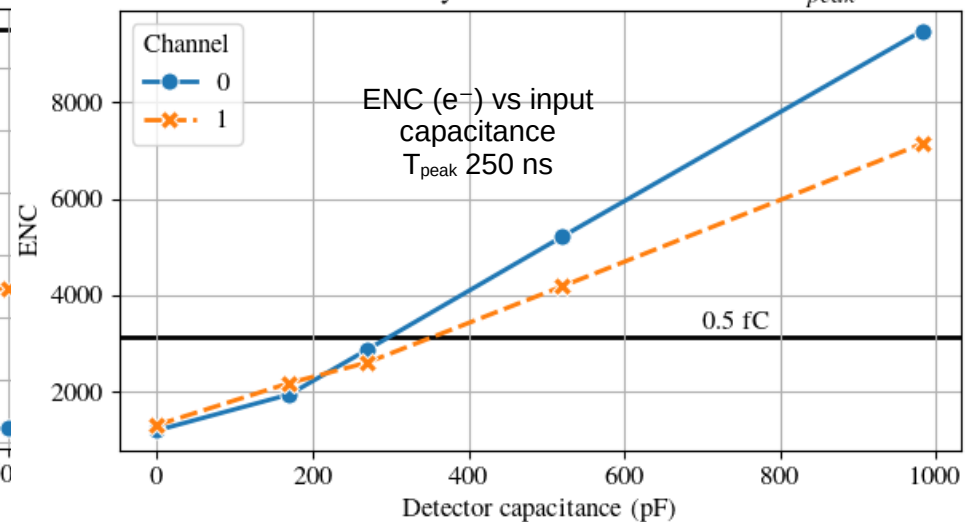
Noise measurements

- ENC vs peaking time, < 0.5 fC for most of t_{peak} and ASICs
- ENC < 0.5 fC for input capacitance lower than 300-350 pF
- Lower ENC for CH1 compared to CH0, for capacitance above 200 pF

Mesured baseline ENC for Gain = 1 and $C_{det} = 170$ pF



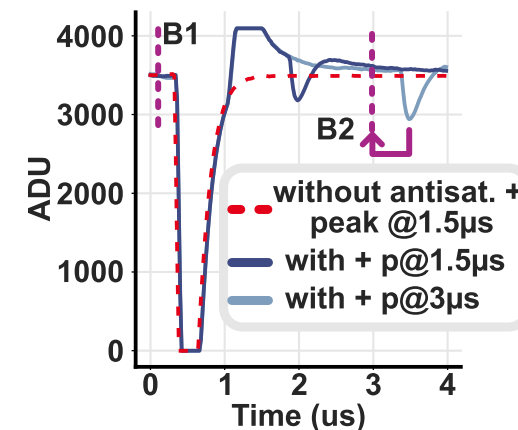
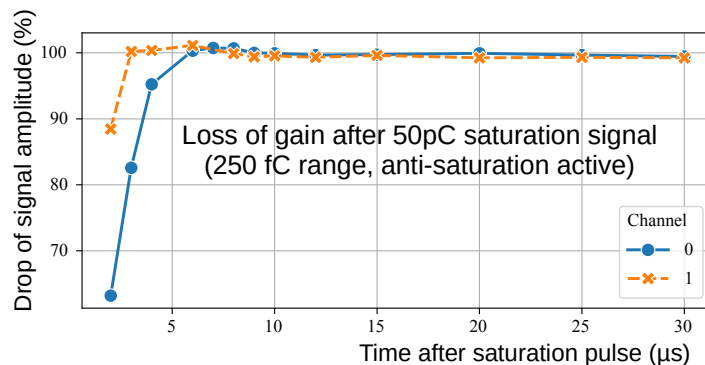
Mesured baseline ENC by channel for Gain = 1 and $T_{peak} = 250$ ns





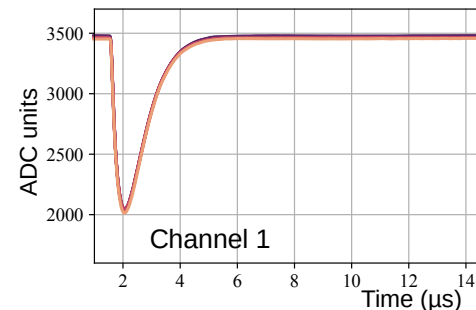
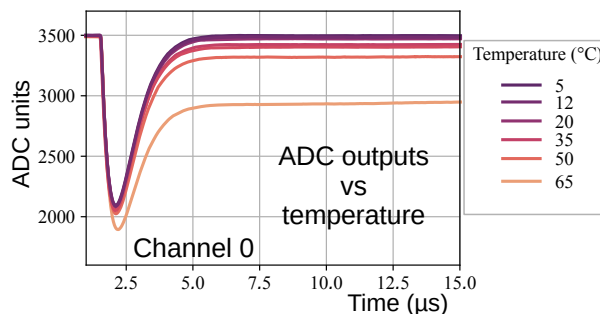
Saturation measurements

- Signal sent after 50pC saturating charge
- Without anti-saturation no detection during $> 12\mu\text{s}$
- With anti-saturation, signal can be measured even at $1.5\mu\text{s}$
- Baseline instabilities for CH0, no such problem with CH1



Stability with temperature

- Temperature tests between 5 and 65°C
- → channel 1 with stable response vs temperature



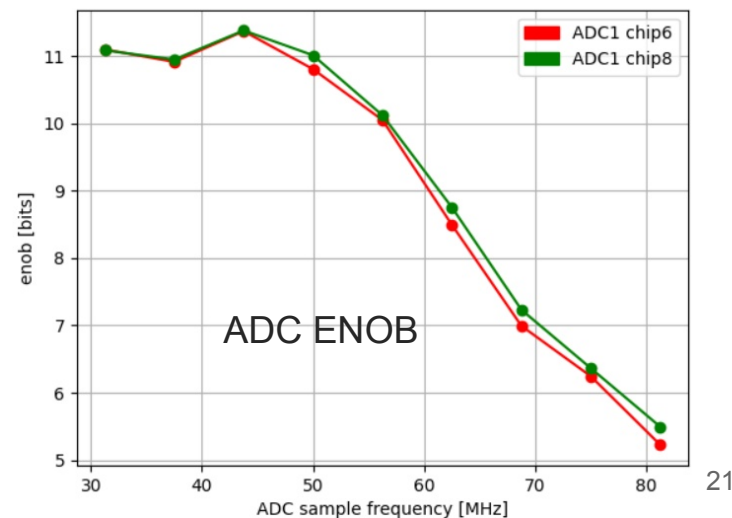
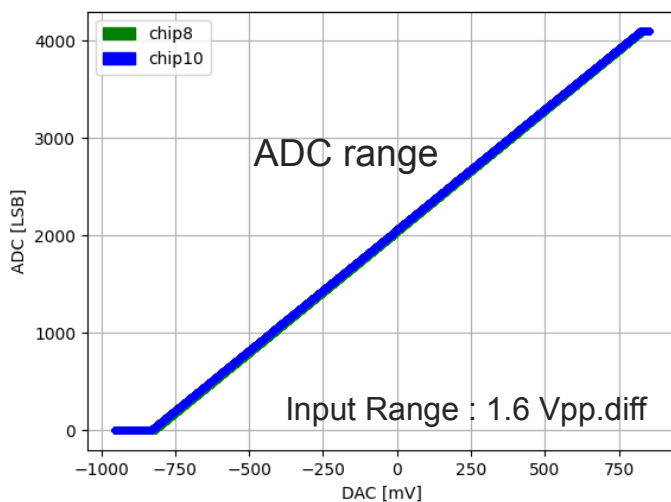
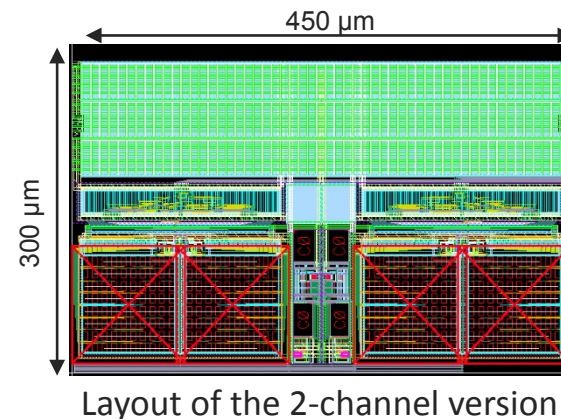
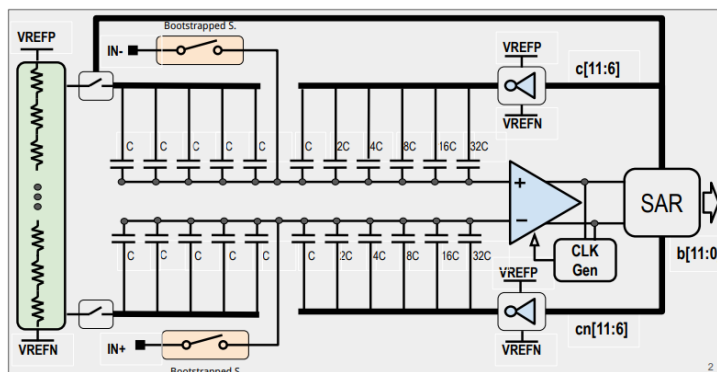
→ CH1 front-end channel selected for SALSA



12-bit SAR ADC

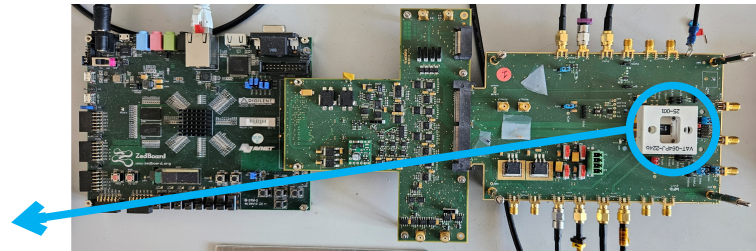
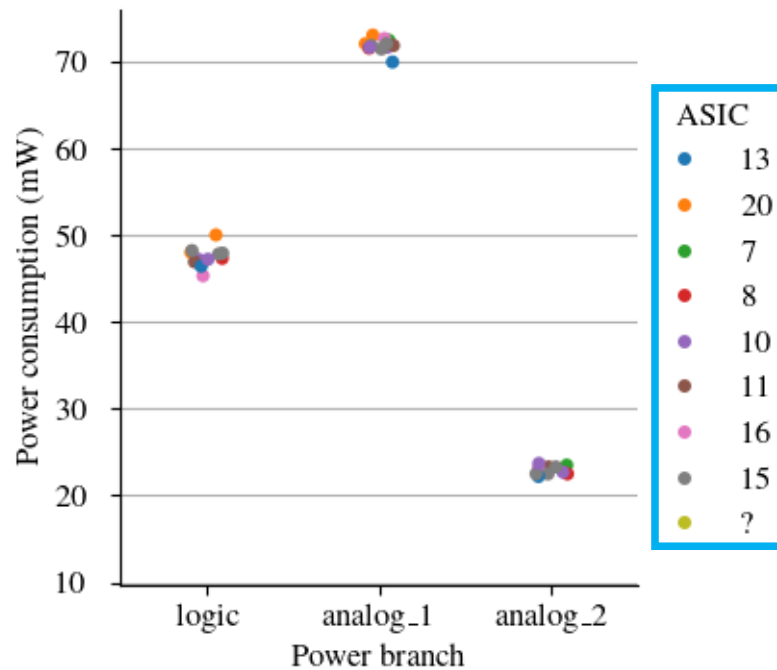
- Developed at USP
- Fast sampling rate at 50 MHz
- Tested on SALSA1, very reproducible (5 chips), 11-bit ENOB
- Selected for SALSA2

Performance summary	
Technology	CMOS 65 nm
Resolution	12 bits
Input range	1.6 Vpp.diff
Fs	50 MS/s (up to 56)
Power	2.05 mW
ENOB	11 bits
Area	0.0675 mm ²



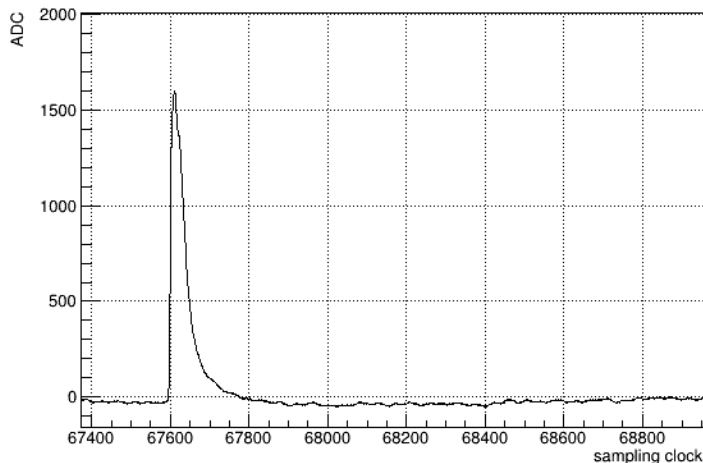
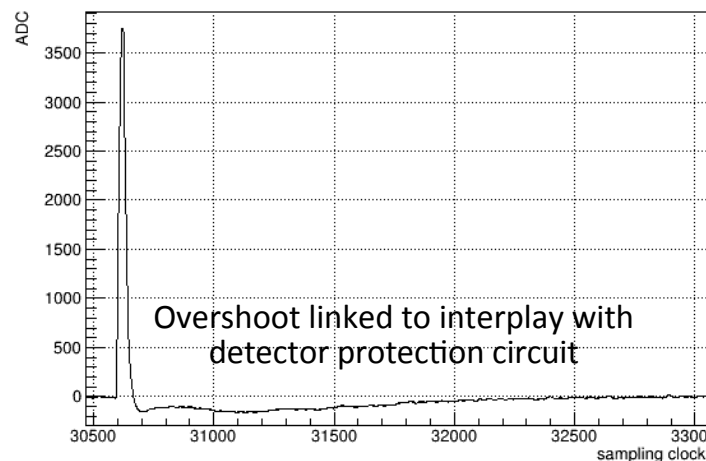
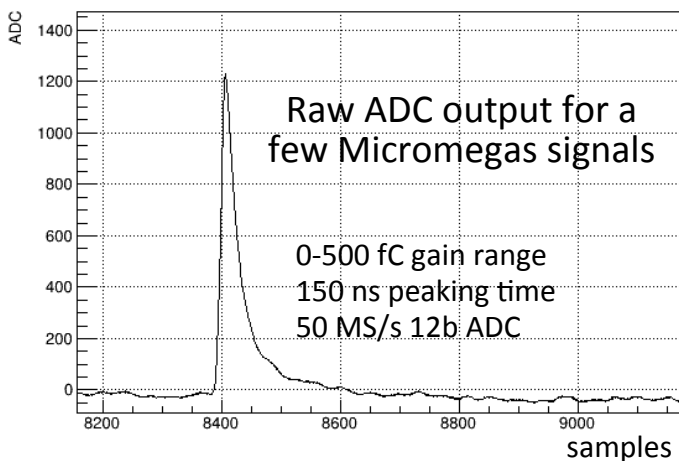
Power consumption

- 3 power inputs at 1.2V
 - analog_1: front-ends including buffers before ADCs
 - analog_2: ADCs
 - logic: digital logic including serial buffers and drivers, I2C, etc...
- Results: logic ~48mW, front-end ~72mW, ADC ~22mW, for 4 channels (+ other elements)
→ ~21mW per channel



Tests with Micromegas detector

- Tests on SALSA1 connected to real MPGDs, 1 strip connected to 1 channel
- Tests with ^{55}Fe source and cosmics, also with some sparks
- Study ongoing on effects of large signals (large HV on detector) and sparks on CSA charge amplifier



- Good readout of MM detectors
- Optimization of front-end parameters needed
- Interest of DSP to improve signals (baseline correction)



Goals of SALSA2

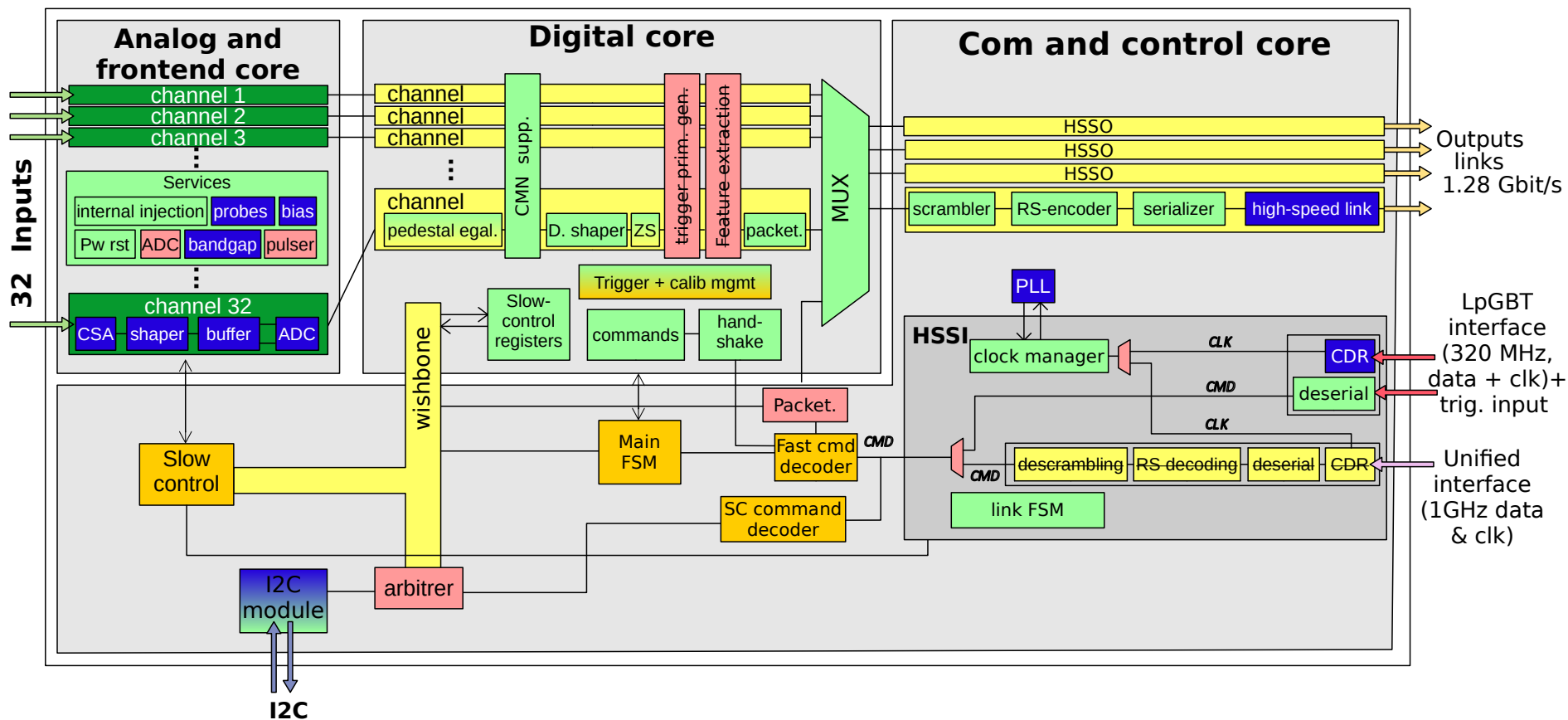
- 1st prototype including DSP to process samples, with 32 channels
- Most of targeted DSP features for SALSA present: pedestal correction, common mode correction, baseline following algorithm, digital filtering, zero-suppression, external triggers, calibrations,...
- Most digital service blocks included: slow-control, I/O, state machine, fast command management, clock management, short information packets, etc...
- A major milestone of the project

Present status

- Front-end
 - ▷ whole schematic done with 2x16-channel block + central service block (bandgap, biases, probes, but no SC ADC)
 - ▷ layouts: 16-channel blocks done, 1st version of service block done
- DSP
 - ▷ RTL code mostly finished and tested in simulation, a few modules with updates to be done (pattern generation, ZS with neighbor channels, calib sample flagging, statistics)
 - ▷ Tests of code in FPGA ongoing (next slides)
 - ▷ First trials of synthesis ongoing, lead to size around 23 mm², power consumption being evaluated
- I/O core
 - ▷ Most RTL code done, stress-test scenarios ongoing, in particular when sampling clock resynchronization happens
 - ▷ Classical input link done, tests ongoing
 - ▷ Statistics code ongoing
- Control core
 - ▷ Fast command decoding code ongoing with review of their specifications
 - ▷ Main state machine ongoing
 - ▷ Monitor packetizer still to be done



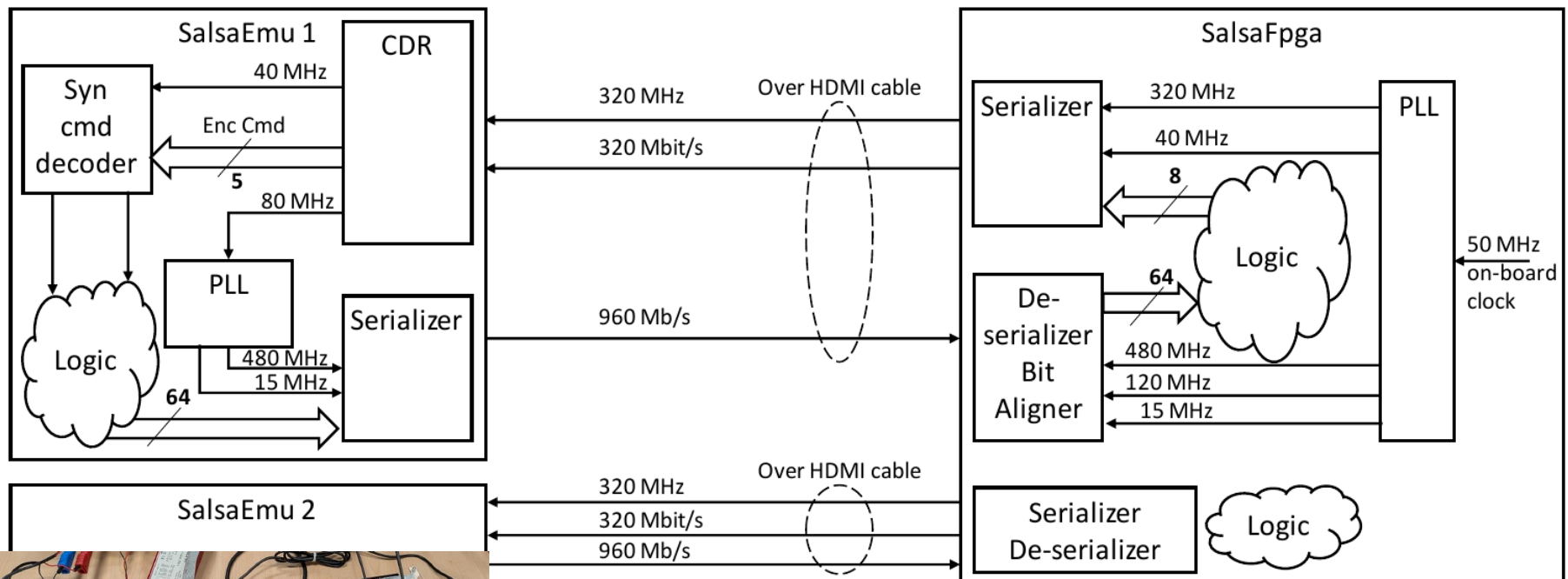
SALSA2 block structure and status of developments



- Tested in prototypes
- RTL/schematics done, tests ongoing
- Layout done
- RTL/schematics ongoing
- RTL/schematics tested, layout ongoing
- RTL/schematics not started

Test of SALSA I/O on FPGA

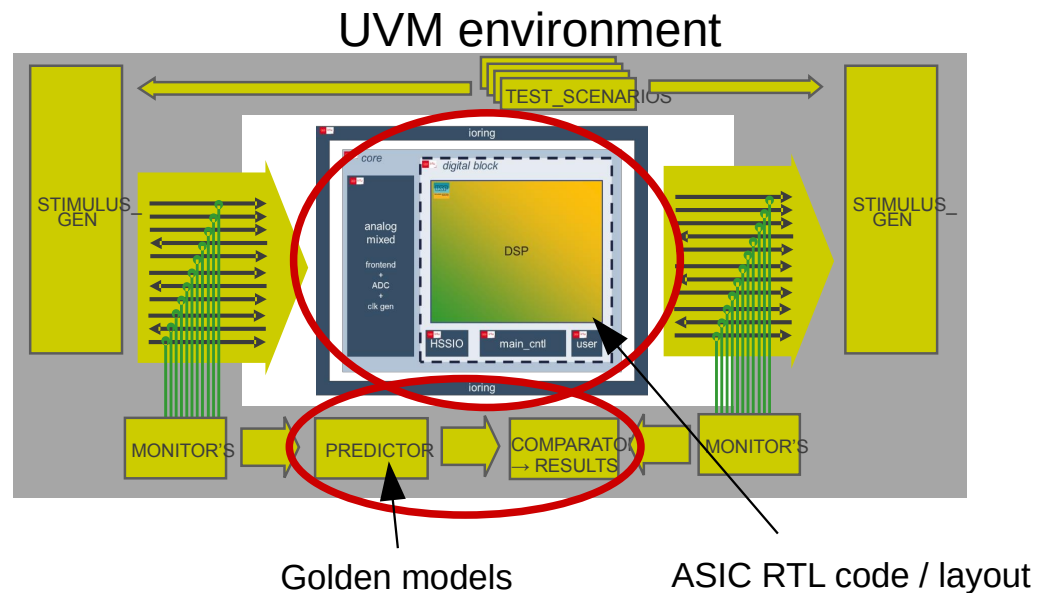
- Goal: test communication RTL code in FPGA, including synchronization with rest of DAQ chain
- 2 FPGA emulating SALSA + 1 emulating receptor
- LpGBT-like interface with 320 MHz clock, 320 Mbit/s downlink, and 960 Mbit/s uplink
- ARTIX 7 boards from ALINX



**Stable operation over hours with synchronization at 50 ps level
Fixed latency over series of resets and synchronization phases**

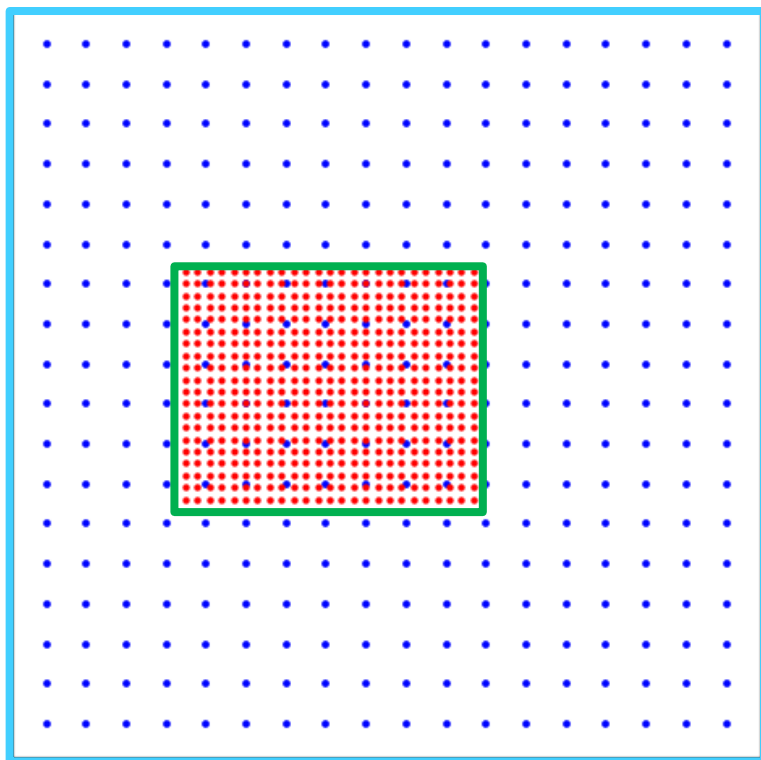
UVM environment

- Environment for verification of simulated ASIC behavior, compared to golden models
- 3 macro-blocks defined: digital_core only, com_and_ctrl_core only, and the whole chip
- 1st version of workspace created for each macro-block, for local verification
- Updates ongoing with alignments of golden models and RTL codes
- Next steps: introduction of complex scenarios to verify general behaviors of each macro-block

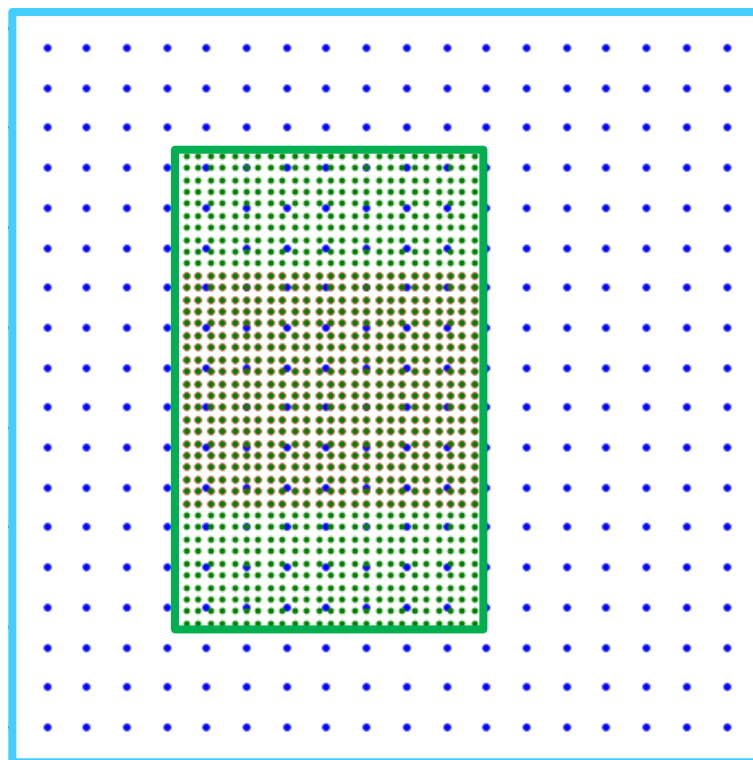




Implementation of SALSA2 and 3 in 18x18mm² BGA package



SALSA2



SALSA3: same BGA pinout with 64 channel ASIC

Package

ASIC



ASIC bumps: 300 µm pitch



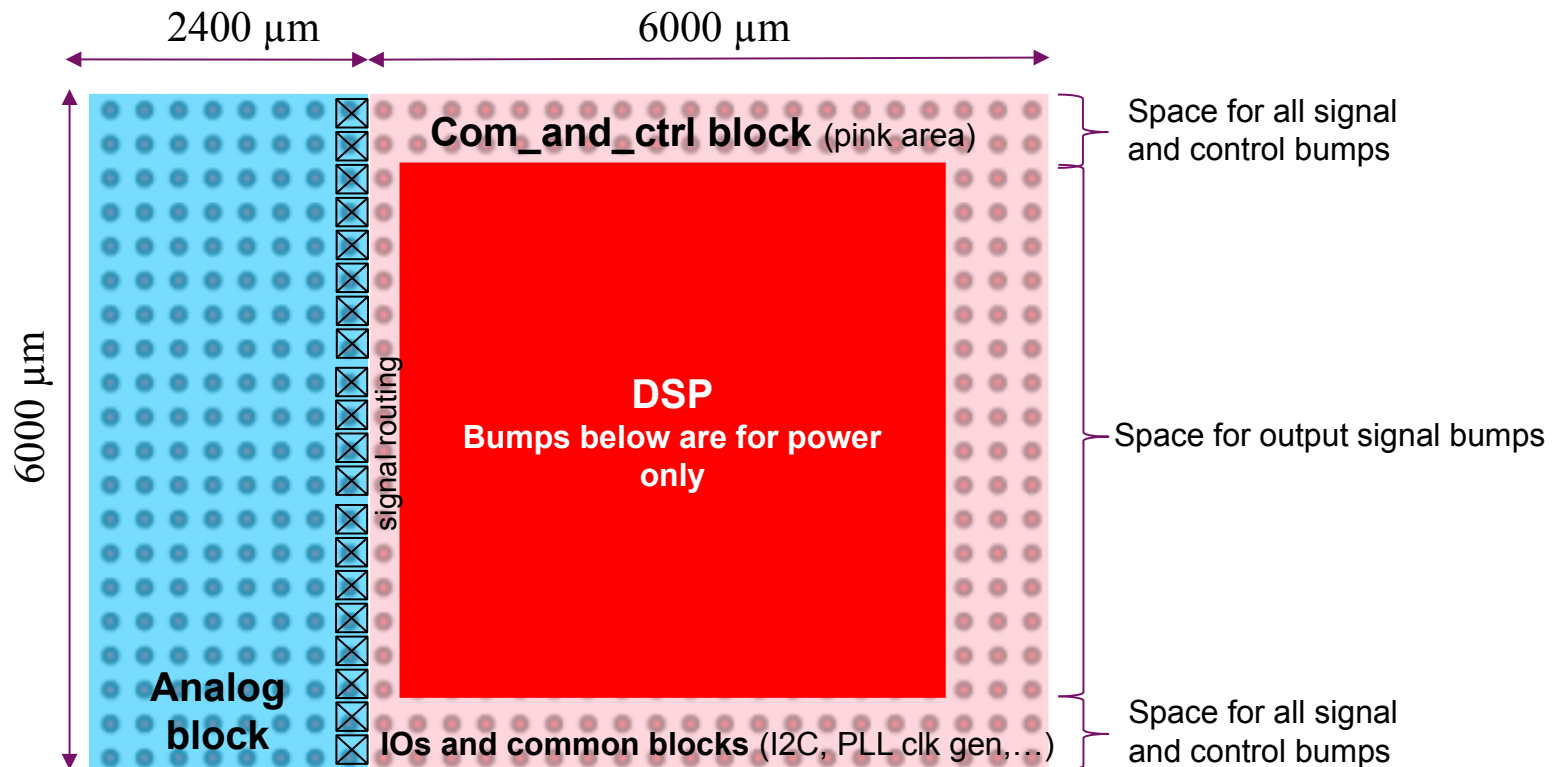
BGA balls : 1 mm pitch (324 balls)

Discussions with BGA provider has already begun



Preliminary floor plan for SALSA2

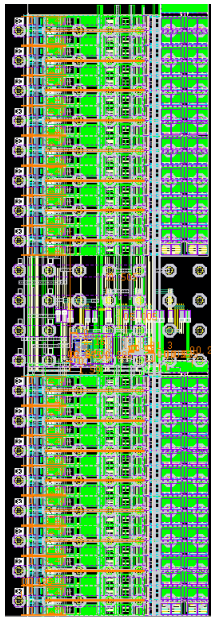
- Size of analog part well defined (cf next slide)
- DSP size still under study, initial synthesis lead to around 23mm²
- Rough estimation of size of communication and control core, test synthesis soon
- SALSA2 full size still very preliminary



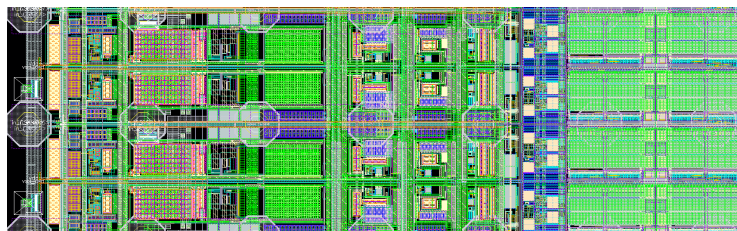


Size consideration for analog part

- Number and size of channels known ($150\mu\text{m} \times 2100\mu\text{m}$)
→ 7+1 column of bumps
- Strategy to have same pin-out between SALSA2 and 3
- → all common services in the middle, only inputs and power bumps on the sides
- Drivers for I/O through bumps ok
- SALSA3: only add more inputs and power on sides

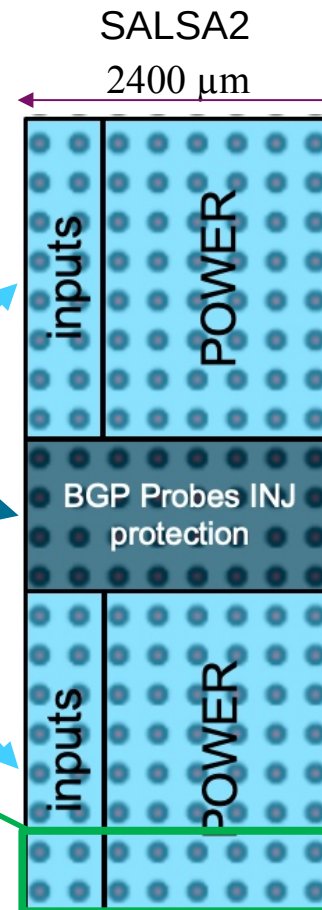


4 front-end channels = 2x7 bumps

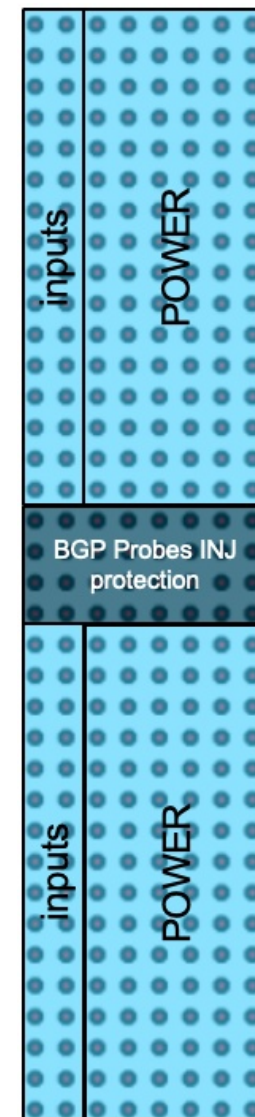


common service block

2x16 channels



SALSA3



● ● ASIC bumps: $300\mu\text{m}$ pitch



SALSA2

- Expected submission in Fall, request sent to CERN/IMEC for November
- Chips available for lab tests in Spring 2027
- Then diffusion to other groups from Summer 2027
- Tests with detectors: small prototypes, large Cymbal detectors, beam tests for validation in real condition

SALSA3

- = SALSA2 after bug corrections, with 64 channels and added features in DSP (amplitude/time extraction, trigger primitives) and in communication and control core (large monitoring packets)
- Start of development right after SALSA2 submission, expected submission in Spring 2028
- Lab tests in Fall 2028
- Diffusion to other groups from beginning 2029
- Tests with MM prototypes, very likely with microRWell as well, test using Cymbal front-end board prototypes, then beam tests to validate the whole setup

Final SALSA

- = SALSA3 after bug corrections
- Validations of all features to be done: functional, performance, environment, system-level
- Final production readiness review Spring 2029
- Production from Summer 2029



Goals of the reviews:

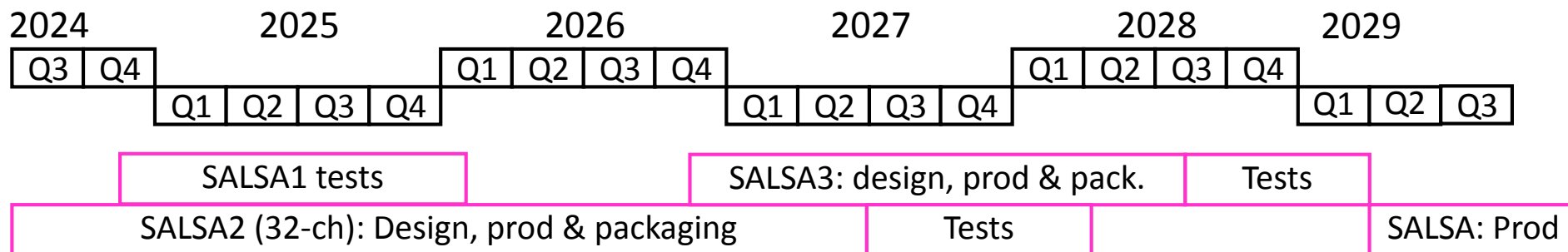
Provide a comprehensive assessment of the ASICs and Discrete Readout from design to production

- Specifications & Requirements - frontend, processing, interfaces, power and packaging (including form factors where applicable).
- Digital Interfaces - commands & controls
- Status & Steps to Completion - with schedule and to include testing/validation with detectors
- **Production Outlook - to include final production review, production timeline and QA/QC testing**
- Documentation - Functionality (e.g. User's Manual/Spec sheets) and QA/QC Plans, and with planned availability for FEB final designs and Engineering Articles, bump/wire bonding.



Steps to complete the project

- Development of SALSA2, submission November 2026, packaging from Spring 2027
- Tests of SALSA2 in Summer 2027
- Design of SALSA3 starting after SALSA2 submission
- Submission of SALSA3 Spring 2028, tests from Fall 2028
- Pre-prod + full production from Summer 2029, 5000 ASICs foreseen for EPIC





■ Green light from Production Readiness Revue, based on

- Functional validation
- Performance validation
- Environmental validation: radiation dose and SEU/SET, temperature, voltage
- System-level validation, including readout chain with DAQ components and protocols

■ Production

- Expected ~5000 chips for all MPGDs, including prototyping and QA tests
- Low enough for in-house validation
 - Robotized automated test stand possibly operating on multiple ASICs in parallel
- Validation strategy
 - Performance characterization on 5% of chips
 - Functional validation of the rest with subsets of parameters covering ePIC needs

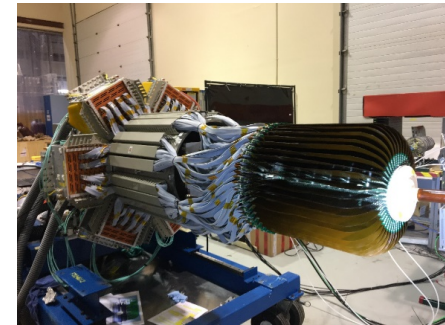
■ Time taken by validation procedure

- Based on experience with HgCRoC and Coluta (ATLAS LAR ADC)
- ~10 min per ASIC → 40/day, 1000 / month
- 1 robot with 2 production test-benches → 3 months in total



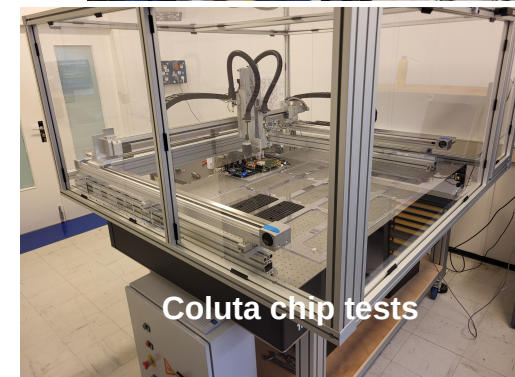
■ Expertise in system-level development

- Detector → readout electronics → DAQ software → analysis
- Design, production, commissioning, maintenance
 - ▷ CLAS12 MVT, T2K TPC, Asakusa tracker, ALICE TPC
- Respect of ES&H regulations of host labs (BNL, CERN, JLab, J-PARC)



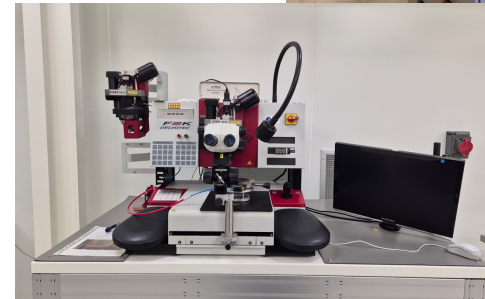
■ Expertise at Saclay in large scale production

- In-house: automated ASIC tester robots, FE board test-benches
- In industry: development of turn-key test-benches
 - ▷ Ex: 40k Rafael and 80k Catia ASICs for CMS Ph2 upgrade
 - ▷ Ex: 700 Alice Solar, 170 LTDB Atlas, 150 Class12 FEU boards
 - ▷ Ex: 40k Coluta ADC chips being tested at Saclay



■ Rich set of equipment for test-benches

- High-end LeCroy and Textronic oscilloscopes
- High performance phase noise analyzer
- Low jitter precision clock sources
- Climate chamber
- Bonding machine



■ Expertise in harsh environment ASIC designs

- Radiation facilities at Saclay, Sao Paulo, CERN and in Europe
- High magnetic field facilities at Saclay and CERN





Goals of the reviews:

Provide a comprehensive assessment of the ASICs and Discrete Readout from design to production

- Specifications & Requirements - frontend, processing, interfaces, power and packaging (including form factors where applicable).
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SALSA specification document

- Base of the ASIC development
- Summary version foreseen for users

User manual for each prototype

- Requirement vs features
- Pin-out, communication protocols
- Slow-control registers
- Best configurations based on tests

Software repository

- Slow-control configurations
- FPGA code for interface with SALSA I/O
- Data decoding and processing

PRISME Technical Documentation

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1. Abstract
2. Requirements vs Features
 - 2.1. PRISME_v0 and the EIC project
 - 2.2. Requirements
 - 2.3. Features
3. Pin Assignments and Description
4. Registers and Bit description
5. Functional Description
6. Timing and Electrical Specifications
7. Mechanical Data
8. Weaknesses Identified

SALSA1_v0 Developer Manual

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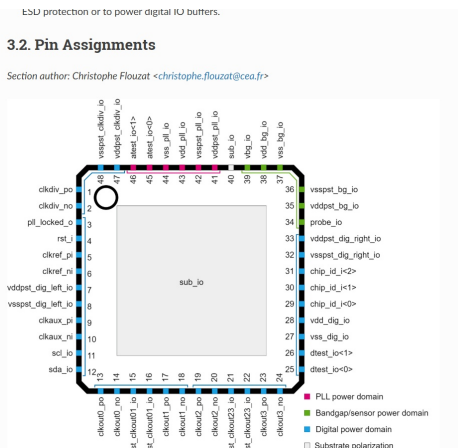
1. Abstract
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- temperature sensor
- total ionizing dose sensor

2.3. Features

The PRISME_v0 chip includes the features listed in [Table 2.1](#).

Table 2.1 Features of PRISME_v0

Variable	Value	Remark
Technology node	TSMC 65 nm	compatibility with SALSA
Radiation Hardening	Full TMR for digital	
Low jitter	Low jitter PLL design	
Input Clock Frequency	40 MHz ; 75-125 MHz	typical case is 100 MHz
Nb Generated Clock Outputs	4	
Output Frequency Clock	3.125-800 MHz	8-bit configuration of clock dividers
Output Phase Shift	0-320ns step 1.25ns	8-bit configuration
Slow control	I2C	with configurable address

Previous

Next

14	14.6	10M
15	135	1M

4.2.18. REGFRONTEND_2

Table 4.34 REGFRONTEND_2 - ADDRESS: 17 - RW

Bit #	Name	Reset	Function
6:0	CARAC_RF2	42	PZC configuration (from 0 to 255) for channel 1 and 3 (see below).
7	CARAC_POS	0	Enables positive polarity of the channel (connection to the cathode of the detector)

RF2 doesn't describe a resistor, it describes the whole configuration of the PZC. It's a combination of several bits and therefore, only few RF2 values over the 255 are relevant. For each gain, 3 different values of the reset resistor are available: 100MOhms, 10 MOhms and 1MOhms. Depending on the counting rate and noise requirements, one may tune the reset at high values (low noise, low rate) or low values (high rate, high noise). The different allowed values and corresponding code are listed in [Table 4.35](#) By default, it is tuned to 42 which means that the gain is tuned at 1 and the corresponding reset resistor is internally set to 10MOhms.

Table 4.35 RF2 recommended values

RF2	Cf	Target Rf
12	200F	100MOhms
44	200F	10MOhms
108	200F	1MOhms