

CALOROC for SiPM Readout at EIC

Internal ASIC Review

May 13 2026



Frederic DULUCQ



ASIC & Discrete Readout Internal Reviews

Goals of the reviews:

- Provide a comprehensive assessment of the ASICs and Discrete Readout from design to production
 1. Specifications & Requirements - frontend, processing, interfaces, power and packaging (including form factors where applicable).
 2. Digital Interfaces - commands & controls
 3. Status & Steps to Completion - with schedule and to include testing/validation with detectors
 4. Production Outlook - to include final production review, production timeline and QA/QC testing
 5. Documentation - Functionality (e.g. User's Manual/Spec sheets) and QA/QC Plans, and with planned availability for FEB final designs and Engineering Articles, bump/wire bonding.

Review Schedule:

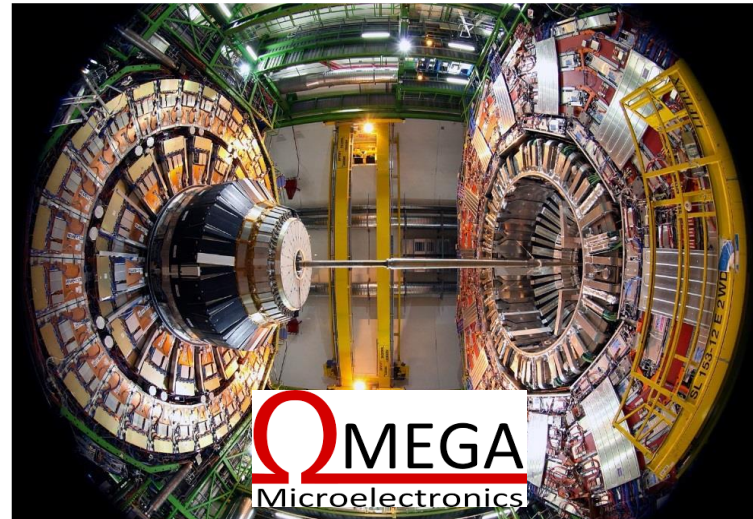
- EICROC - 1 April 2026
- ALCOR - 22 April 2026
- SALSA - 6 May 2026
- **CALOROC - 13 May 2026**
- FCFD - 20 May 2026
- Discrete - 27 May 2026

H2GCROC for the endcap calorimeter – Phase II

6M of Silicon channels
(+ 240k of SiPM)

Radhard (200 Mrad)
Low Power (15 mW per chn)
Precise timing (25 ps)

Total of 150k ASICs needed
Pre-prod this year



CALOROC for EIC

Same ASIC structure (floorplan)
Same ADC and TDC
Same readout

Common interfaces

HEP trend => imaging calorimetry

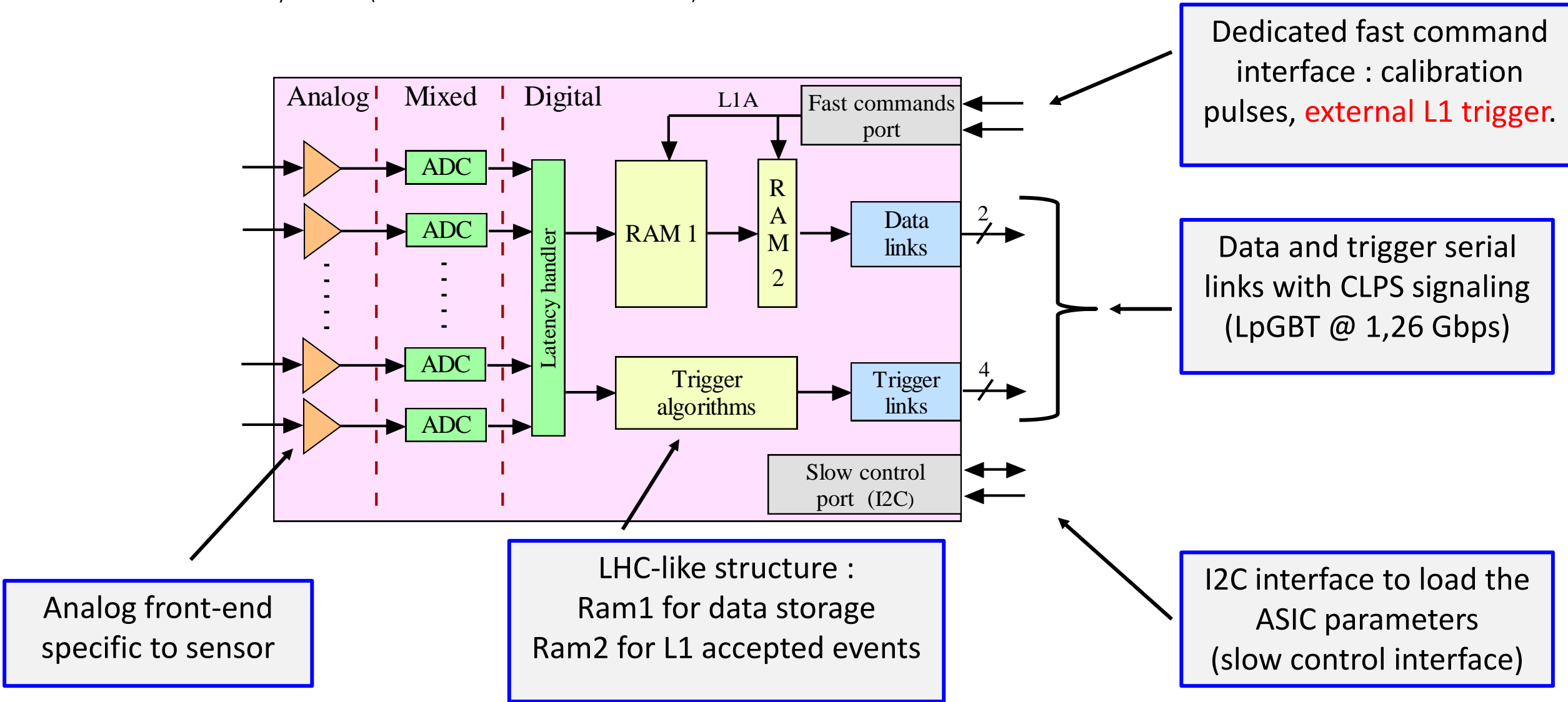
- High number of channels
- Charge and precise timing (<100 ps)
- Low power + System-On-Chip

Based on H2GCROC, CALOROC will provide a versatile and low-power solution for SiPM readout

ROC chips standard structure

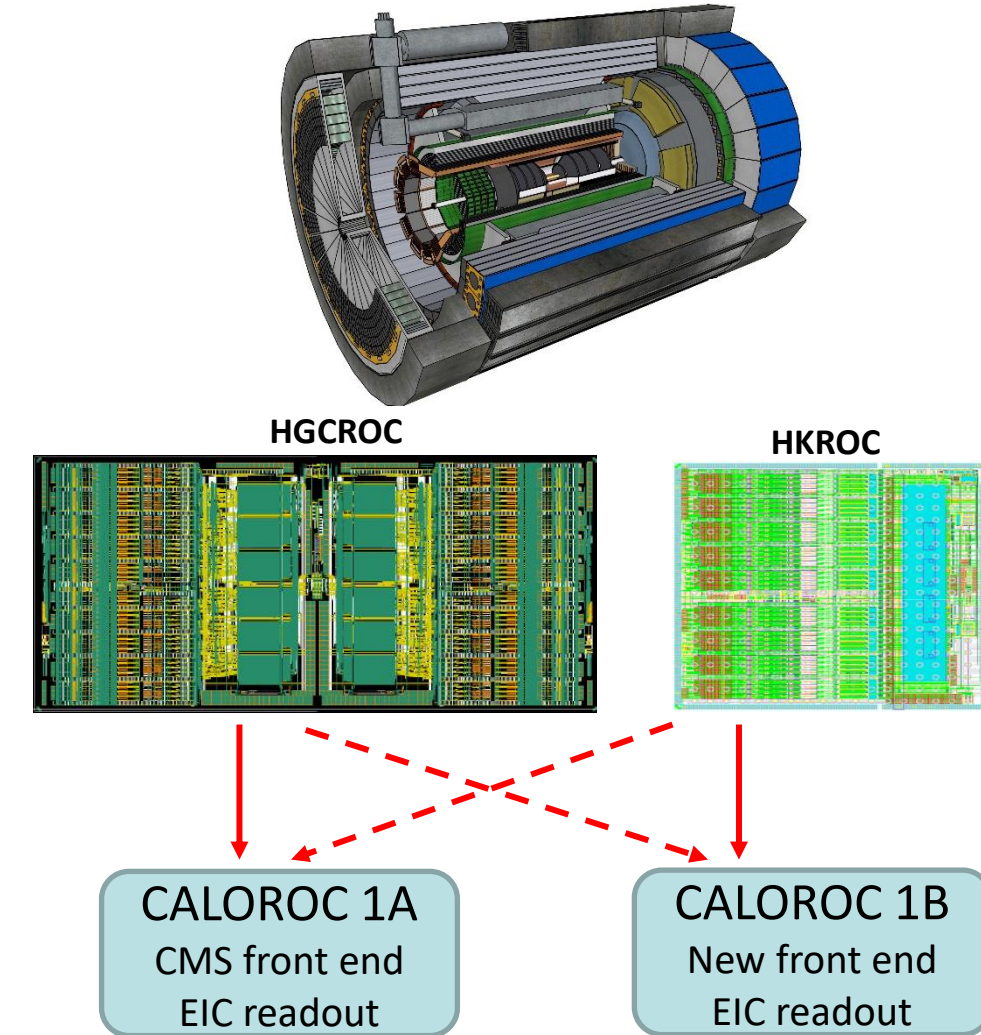
❑ H2GCROC (for SiPM readout) is an HL-LHC colored ASICs (external L1 trigger)

❑ Below is an calorimetry structure (but interfaces for CALOROC will similar)



What is CALOROC ?

- ❑ CALOROC will be available in 2 versions for SiPM readout:
 - ❑ SiPM range capacitance from 560 pF to 8.96 nF
 - ❑ ~ 10-15 mW / channel
 - ❑ **Radiation hardening (HL-LHC levels)**
 - ❑ 200 Mrad and 10^{16} n_{eq} / cm² (1 MeV equivalent neutrons)
 - ❑ SEE hardening on control logic
 - ❑ Charge and time measurement
- ❑ Streaming readout (no external trigger required)
- ❑ Conservative CALOROC1A based on CMS H2GCROC:
 - ❑ H2GCROC (ADC, TOT) analog/mixed reuse
 - ❑ Back-end compatible with EIC + zero-suppress
- ❑ New CALOROC1B based on gain switching:
 - ❑ New analog part without TOT (dynamic gain switching)
 - ❑ Backend « à la HKROC »: auto-trigger, zero-suppress – EIC compatible

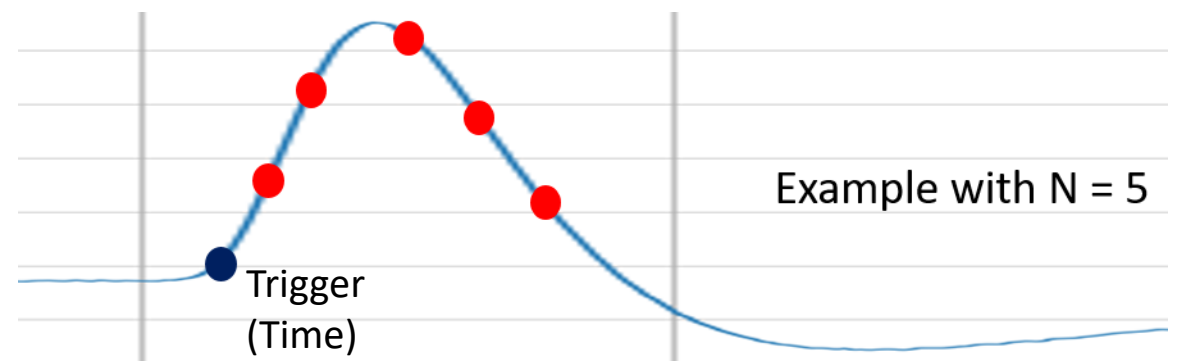


CALOROC1 received beginning of April 2026

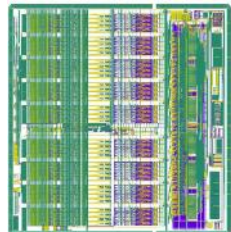


❑ CALOROC main changes:

- ❑ Released in 2 versions: CALOROC-A and CALOROC-B
- ❑ New 6-layer substrate – BGA (common)
- ❑ New EIC digital processing (common)
- ❑ New testboards (common)

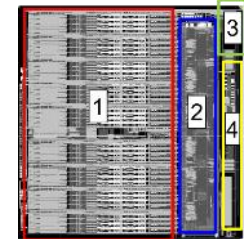


CALOROC 1A
CMS front-end
100-600pF SiPM capacitance

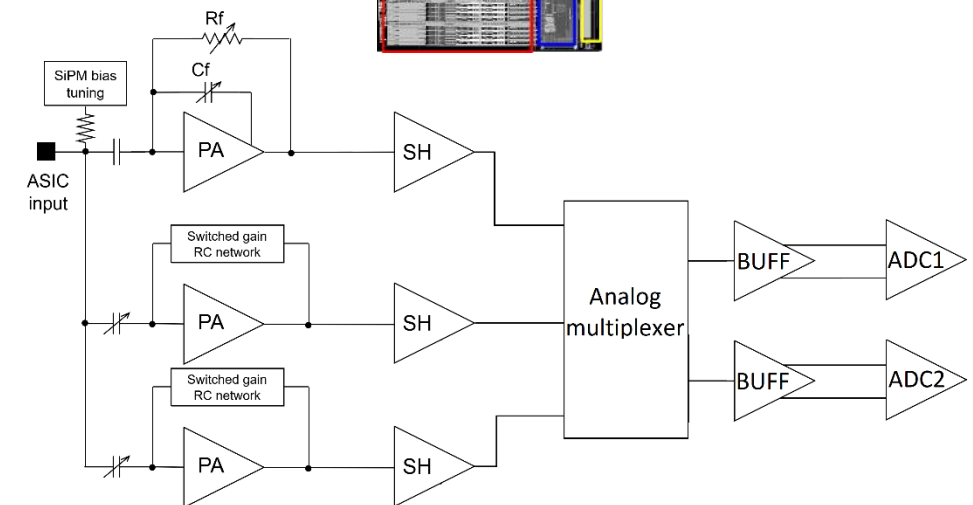
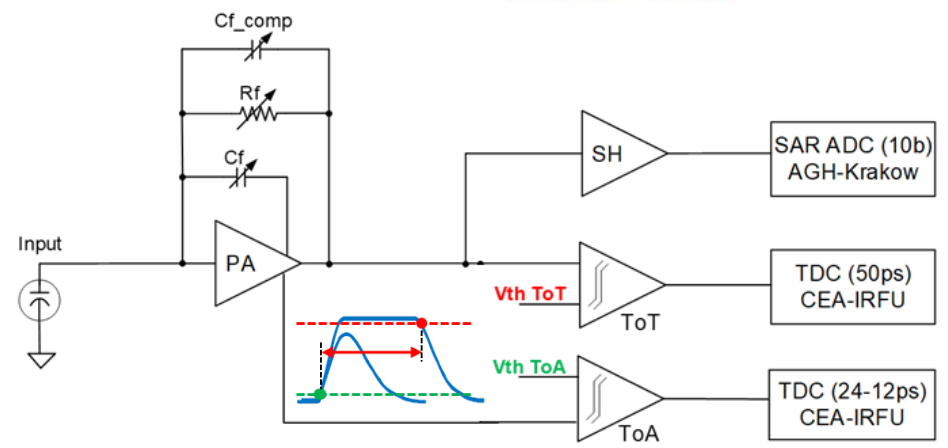


Measurements
not started

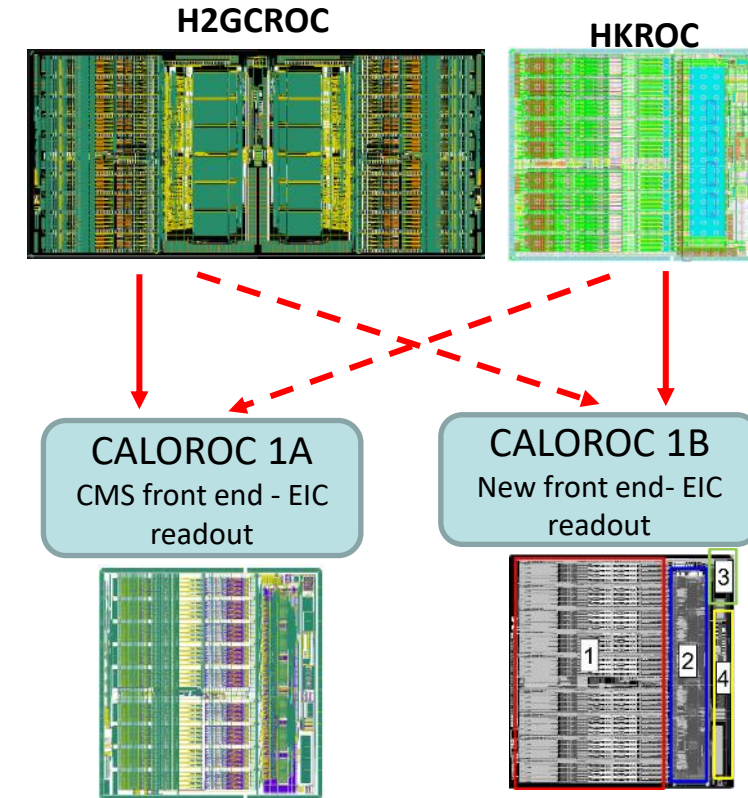
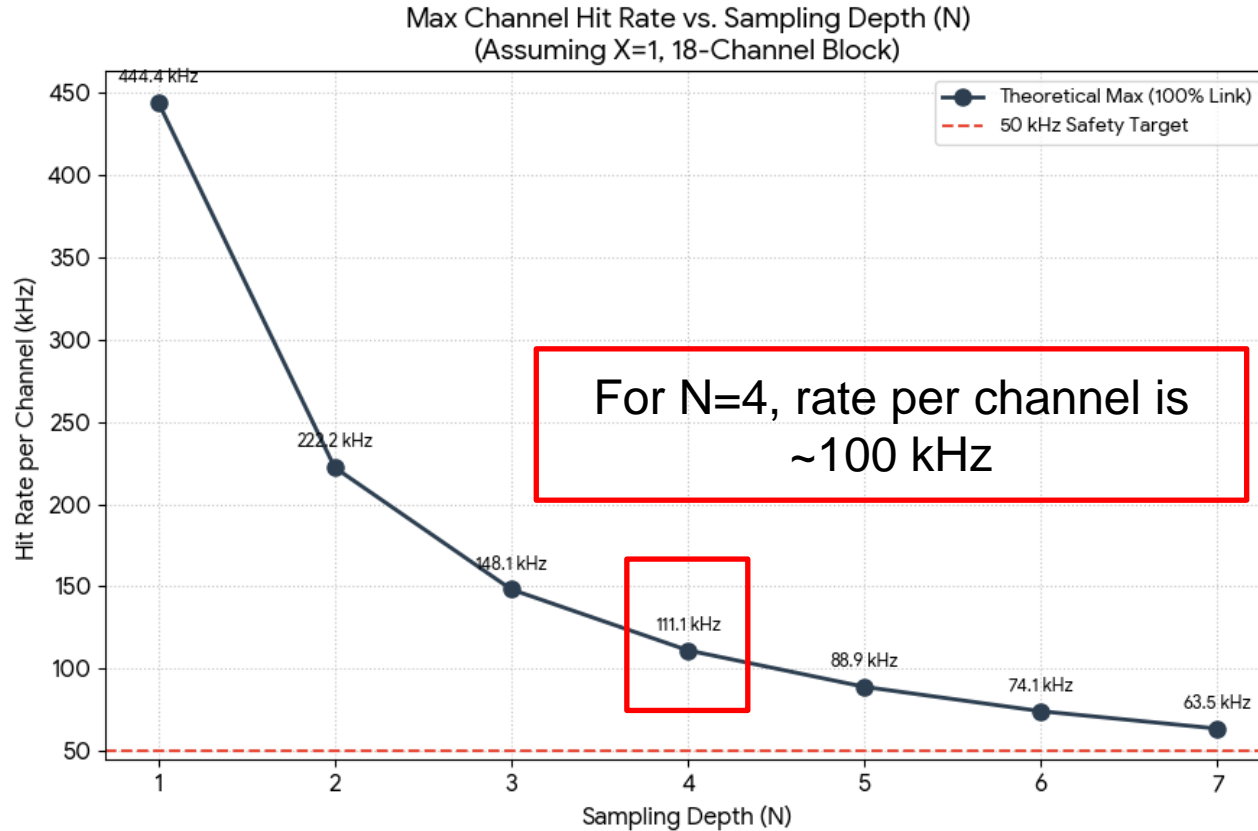
CALOROC 1B
New switched-gain front-end
600p-10nF SiPM capacitance



Measurements
in progress



- ❑ Channel rate calculated with:
 - ❑ Uniform distribution
 - ❑ Worst case = always 1 channel readout over 18
 - ❑ Example with N=4 and
 - ❑ 2 separated in time hit → 40 words read out
 - ❑ 2 in-time hits → 24 words read out

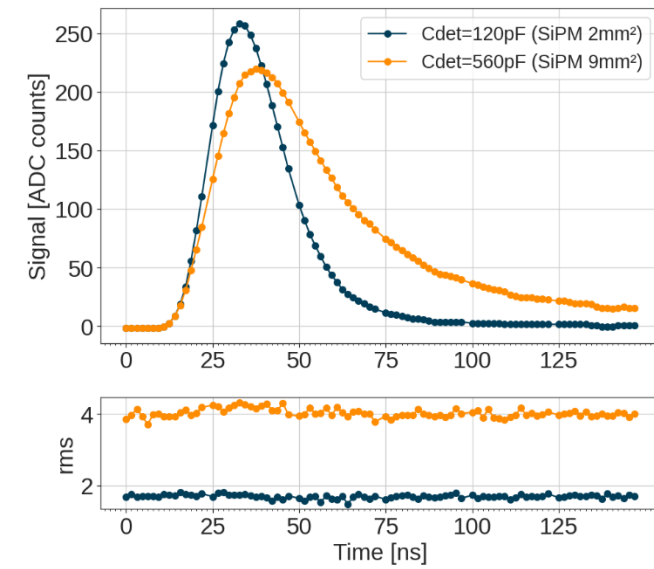
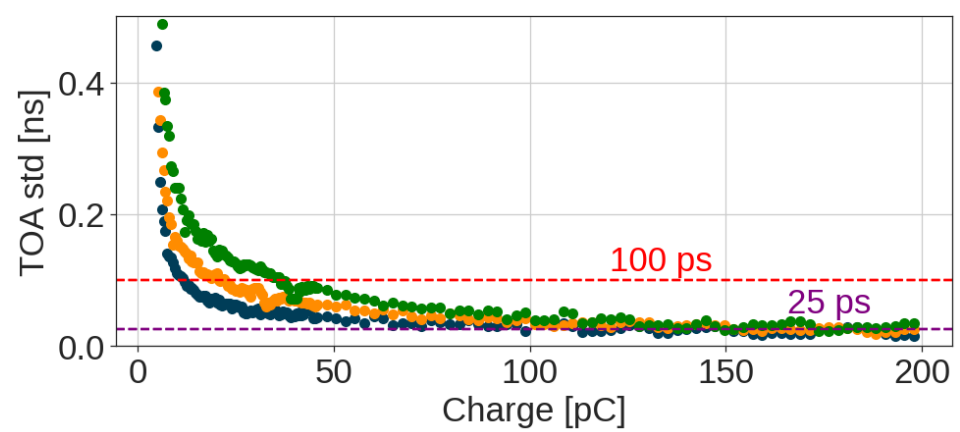
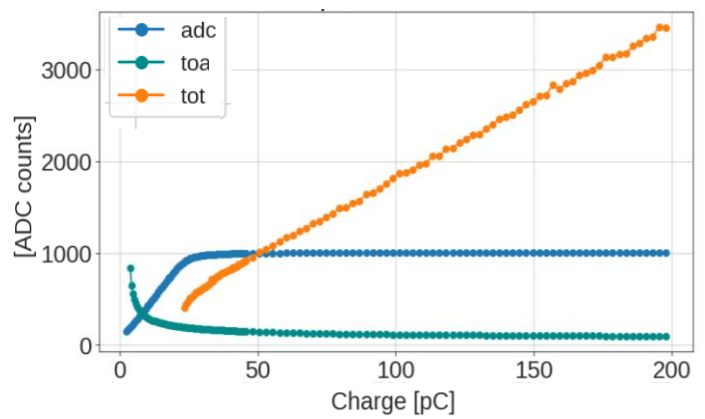
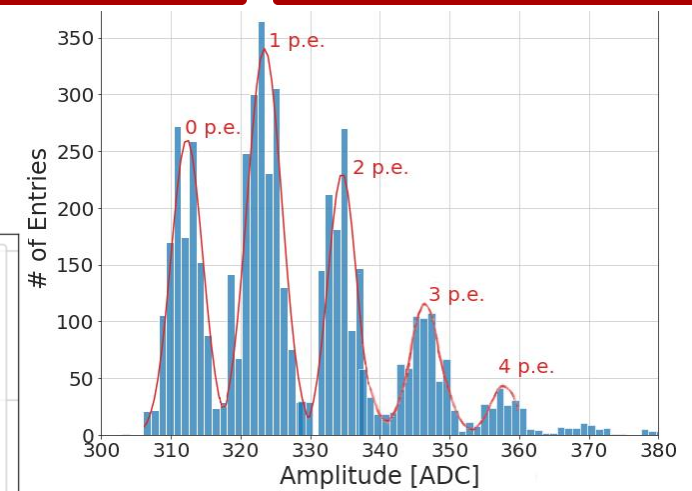
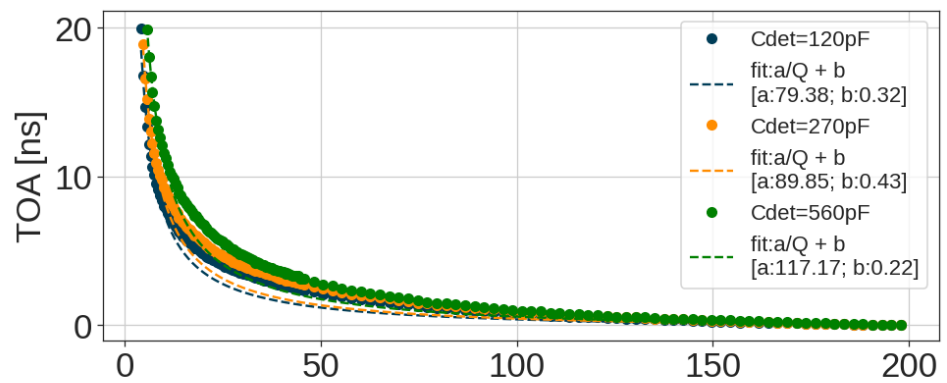
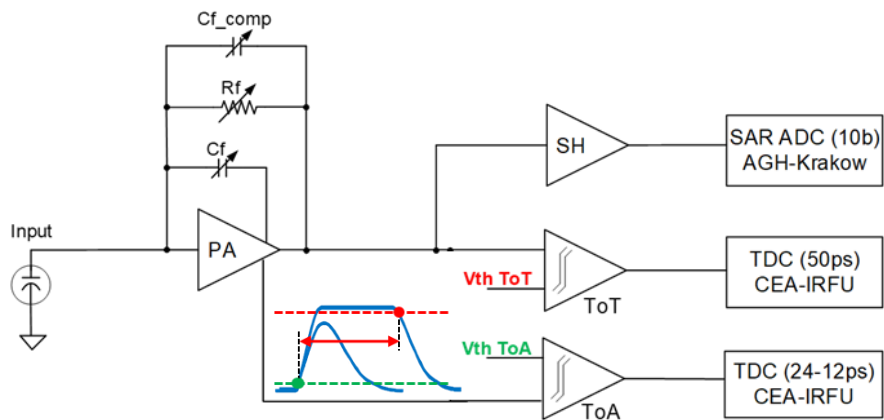


1. The Readout Model

$$T_{\text{readout}} = N \times (X + 4) \times 25 \text{ ns}$$

☐ Reuse of analog front-end based on ADC/TOT and TOA: fully characterized *

☐ 15 mW per channel / Radiation performance / SiPM range 100-600 pF



☐ CALOROC1A only update its back-end to be EIC compatible

* TWEPP 2023 → <https://doi.org/10.1088/1748-0221/19/04/C04005>

❑ New dynamic frontend with switched gain:

- ❑ 1 high gain preamplifier
- ❑ 2x low power preamplifier
- ❑ 1 analog multiplexer

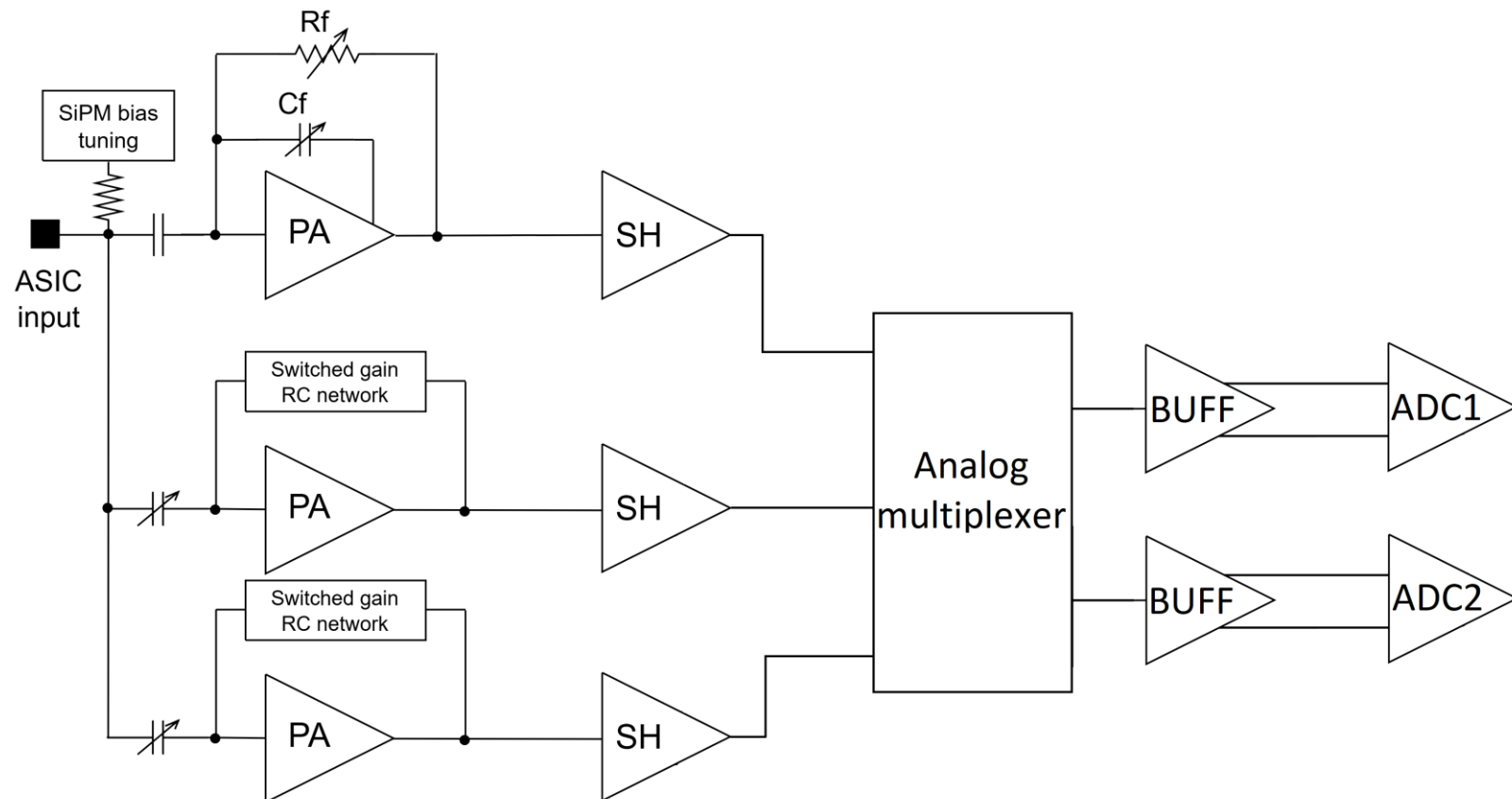
❑ Reuse CMS-H2GCROC ADCs and TDCs:

- ❑ 10-bit 40 MHz ADC (Krakow)
- ❑ 25 ps TDC (Saclay)

❑ Shared CALOROCs backend

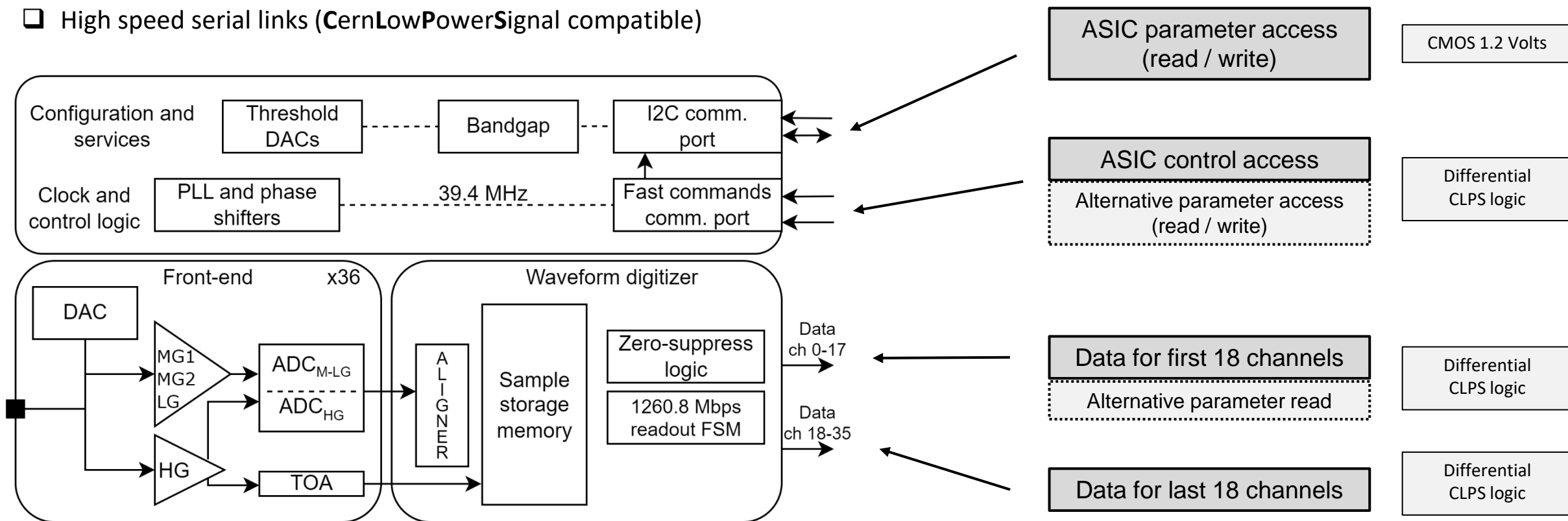
❑ Common specifications:

- ❑ SiPM from 560 pF to 2.24 – 8.96 nF
- ❑ ~ 10-15 mW/channel
- ❑ CMS HL-LHC Radiation level 200 Mrad



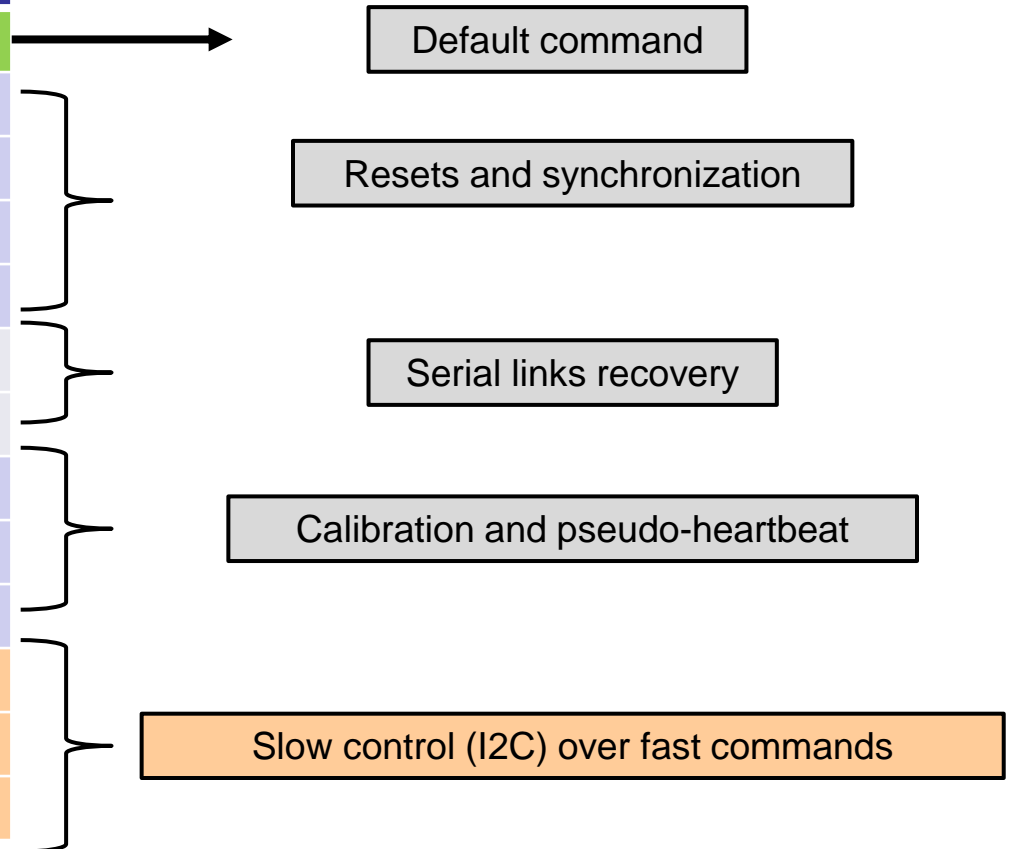
❑ CALOROCs will have the same interfaces (comparable to CMS ones):

- ❑ 1 clock @ 315.2 MHz + 2 resets (hard + soft)
- ❑ Fast command to dynamically control the ASIC (differential)
- ❑ I2C to set the parameters
- ❑ High speed serial links (**CernLowPowerSignal** compatible)



- ❑ Commands to interact dynamically with the ASIC
 - ❑ 8 bits commands synchronized with incoming 315.2 MHz clock – MSB first
 - ❑ Only idle needed – others have a known latency
 - ❑ Detailed in the datasheet

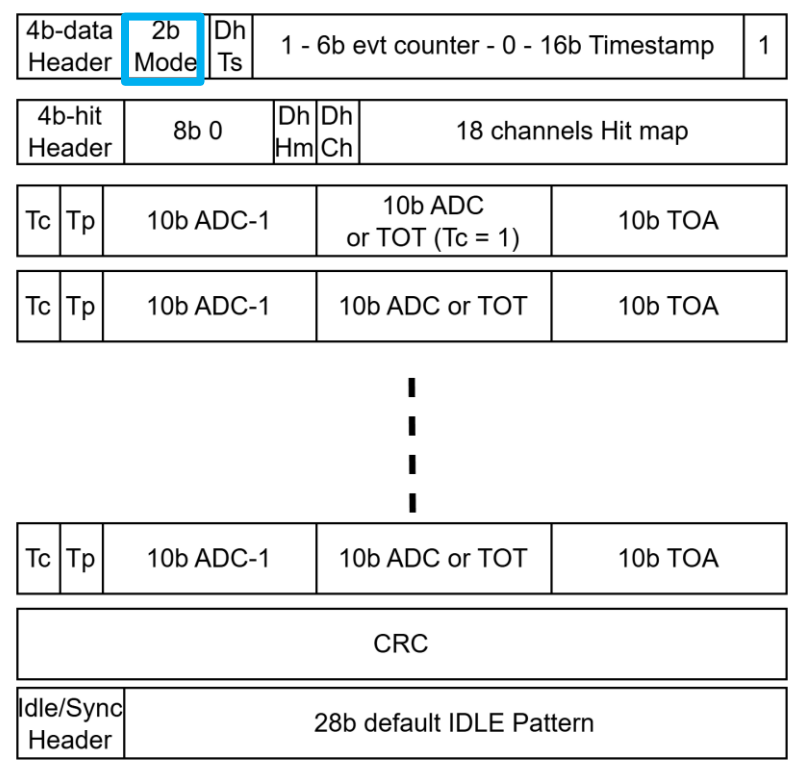
Fast commands	Value	Description
Idle	00110110	Default command inside
ChipSync	11010010	Reset FSM, buffers and counters
BCR	00011101	Reset timestamp counter to a default value
EBR	11010001	Empty readout buffers
PING	10011001	Ping status and counters
LinkResetROCD	10011010	Transmission of synchronization patterns
ROC-Serializer-Reset	10011100	Reset serializer link module only
L1A	01001011	External trigger (all channels)
CalPulseInt	00101101	800 ns internal calibration pulse
CalPulseExt	01111000	100 ns external calibration pulse
SC_0	01011010	I2C over fast command - send '0'
SC_1	01011100	I2C over fast command - send '1'
SC_Valid_Reset	10001011	Valid or reset (2 consecutives) current transaction



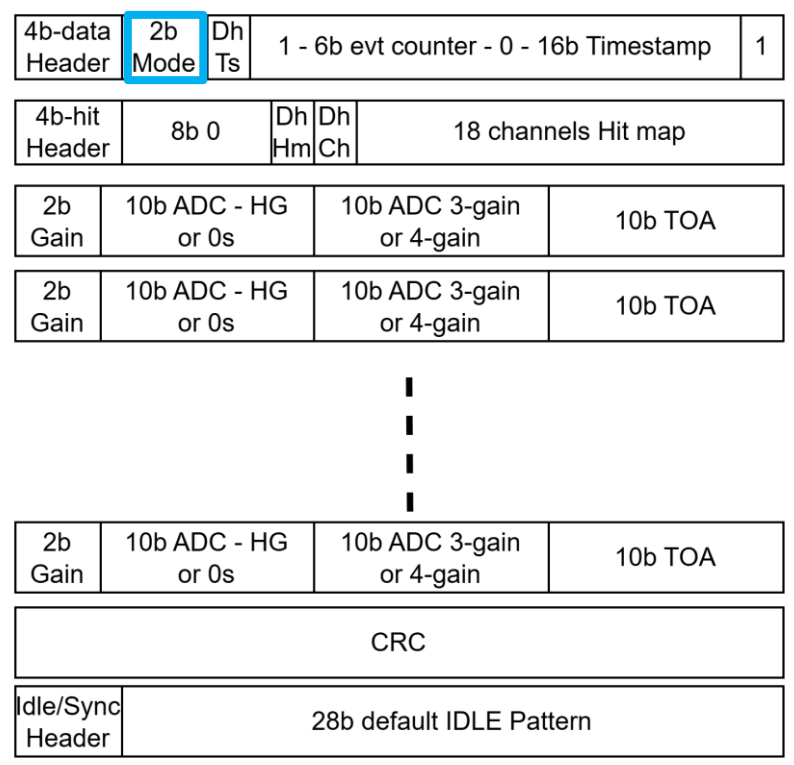
CALOROC: Readout Frames

For charge measurements, CALOROC-A based on ADC/TOT, CALOROC-B only ADCs

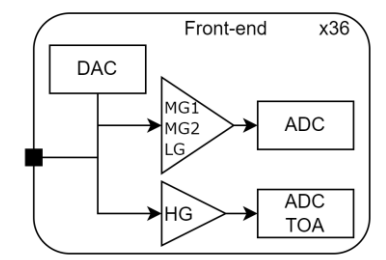
CALOROC A (CMS-like)



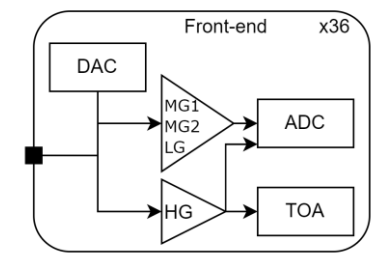
CALOROC B – 2 ADCs or 1 ADC (4 gains)



CALOROC B (2 ADCs)

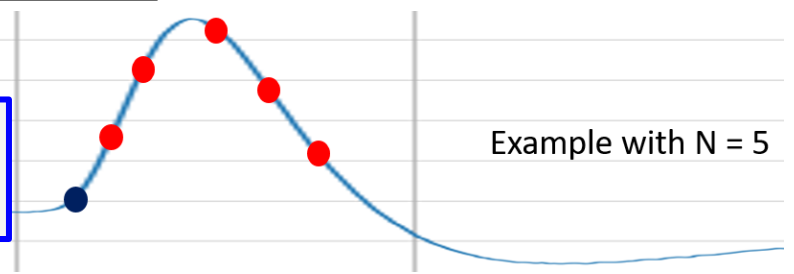


CALOROC B (1 ADCs)



In ZS mode, for **X** (1-18) hit channels and **N** samples, number of 32-bit words is:

$$N \times (2\text{Headers} + X + 2\text{Trailers})$$



Measurements done on HKROC modified motherboard:

- Part of the channels accessible with detector capacitance of 2.2 nF
- Measurements using internal injection DAC (20fC / DAC , maximum of 82pC)
- Firmware + software (LLR – OMEGA)

Python scripts



Monitor
Program
Test

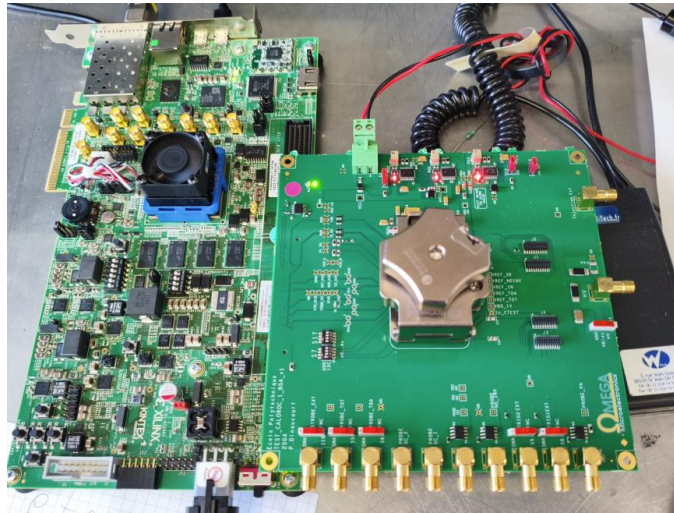
Commercial
KCU105 board

CALOROC
BGA socket

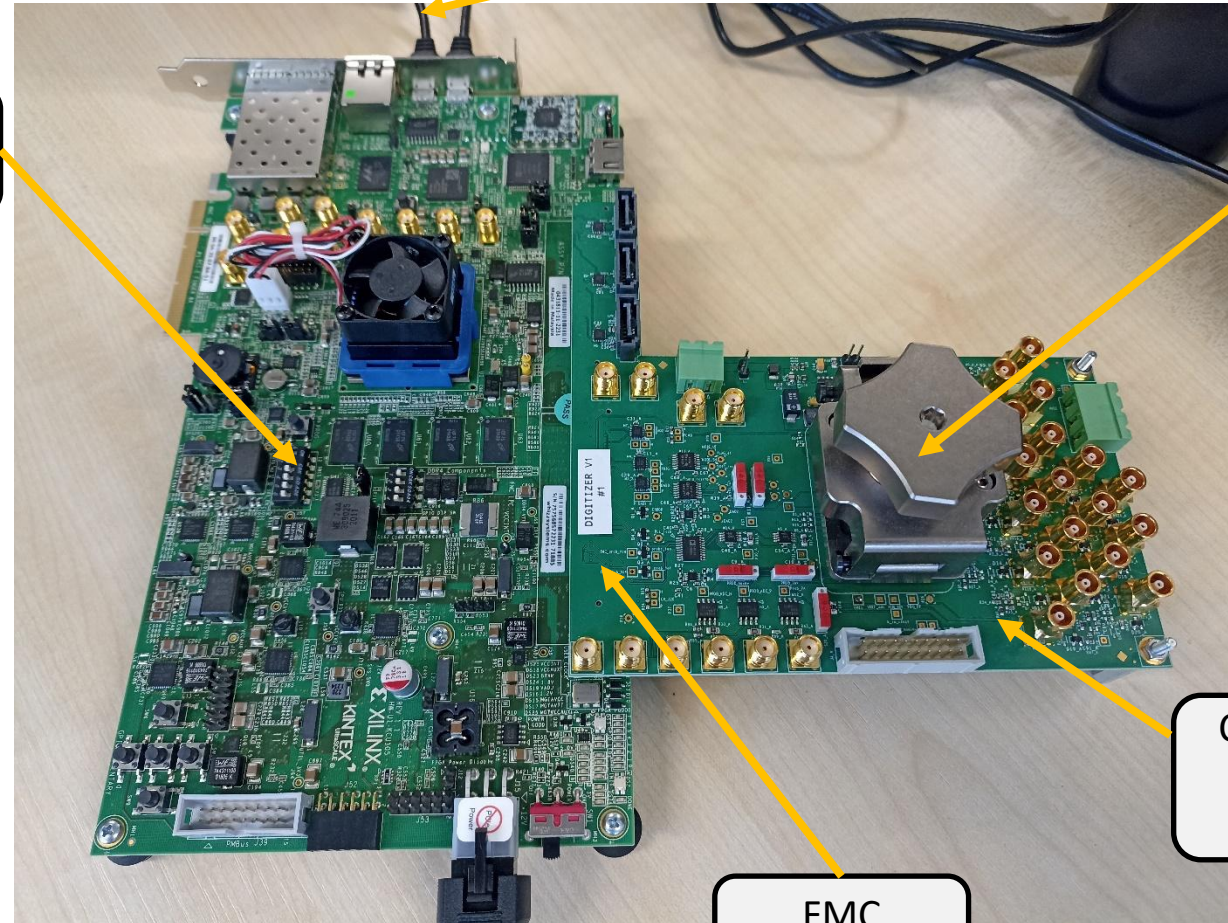


Custom HKROC for
CALOROC
motherboard

FMC
connector



CALOROC
motherboard –
received last week

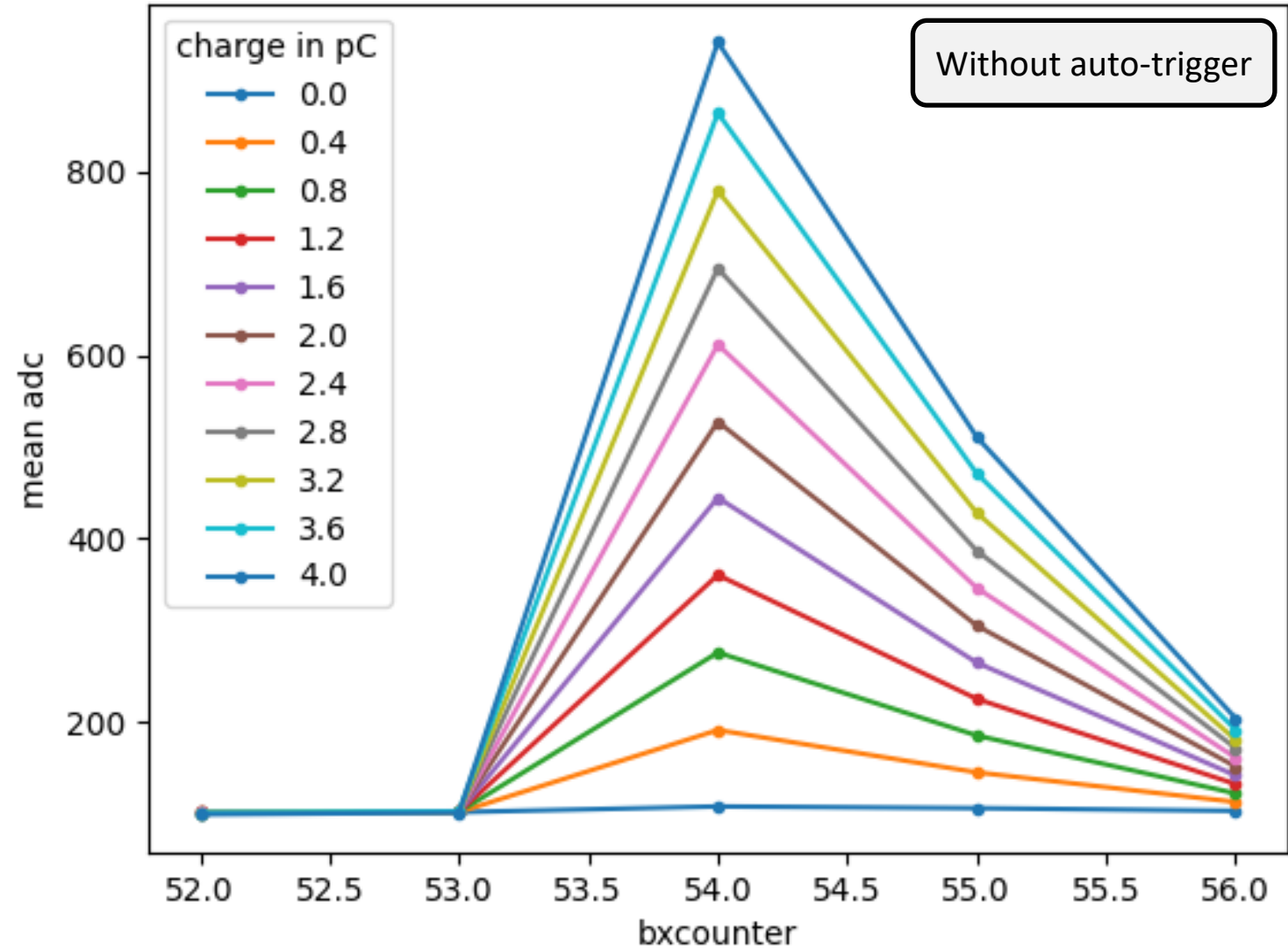


- Using internal injection of the ASIC:
 - High-gain channel
 - Without auto-trigger (using fast commands)
 - to force autotrigger

- Using 5 samples (1 baseline + 4 signals)

- Working as expected but see next slides for detailed analysis (gain / noise / uniformity)

ADC vs BX Counter per Charge for high gain



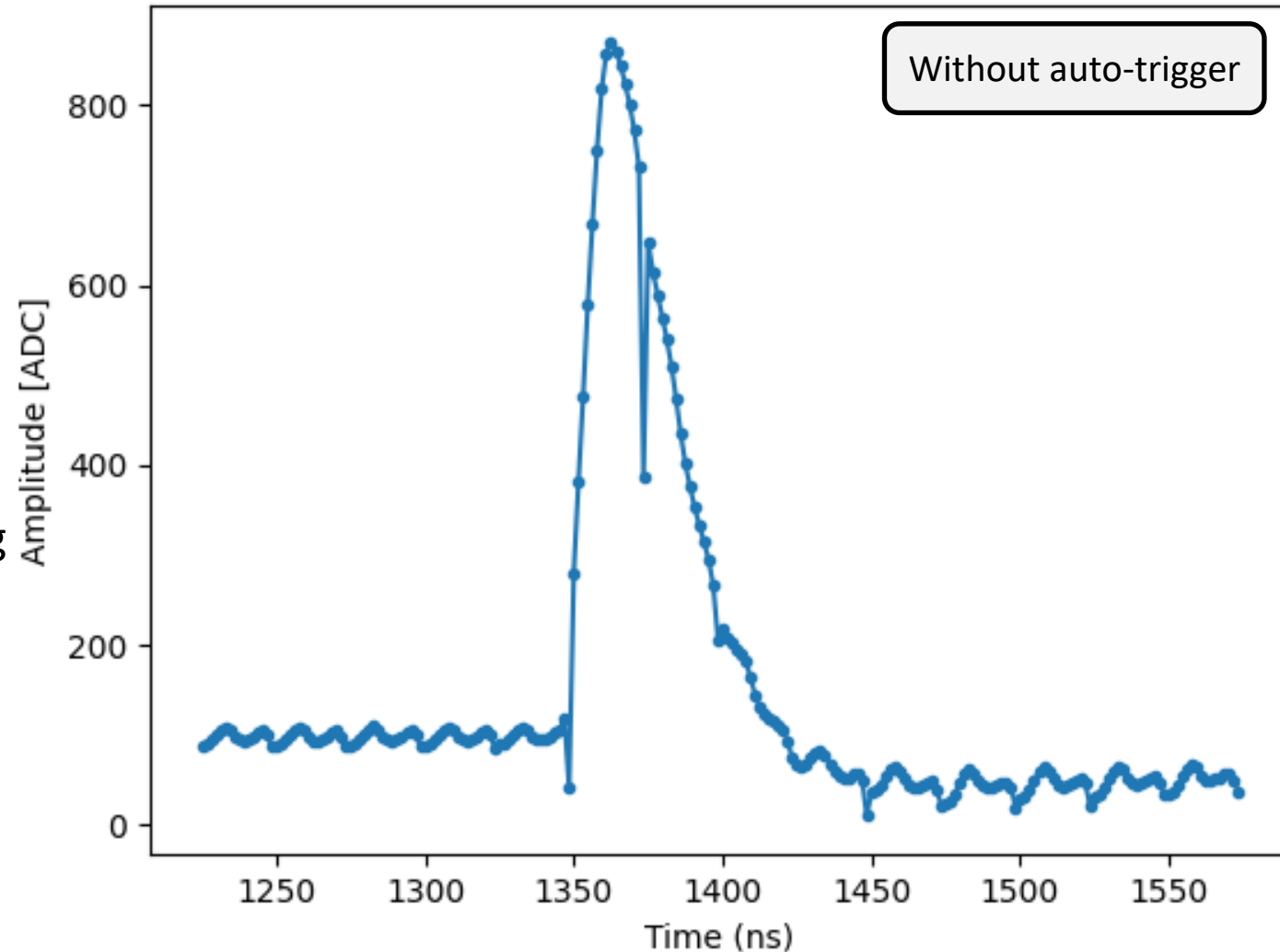
- ❑ Using internal injection of the ASIC:
 - ❑ Done by doing several runs and shifting the ADC **sampling**
 - ❑ Move to 1 sample every ~25 ns to 16 samples
 - ❑ Used only to reconstruct waveform like an oscilloscope

- ❑ Digital noise observed about 4.1 ADC counts
 - ❑ 2.2 counts expected in the simulations

- ❑ SNR for a 10 DAC injection (200fC) was 19 (using the pedestal noise) for channel
 - ❑ Expected but see next slide

- ❑ Investigation in progress
 - ❑ New PCB needed + perhaps dedicated one

Signal vs time for channel 26 with a phase offset of 10

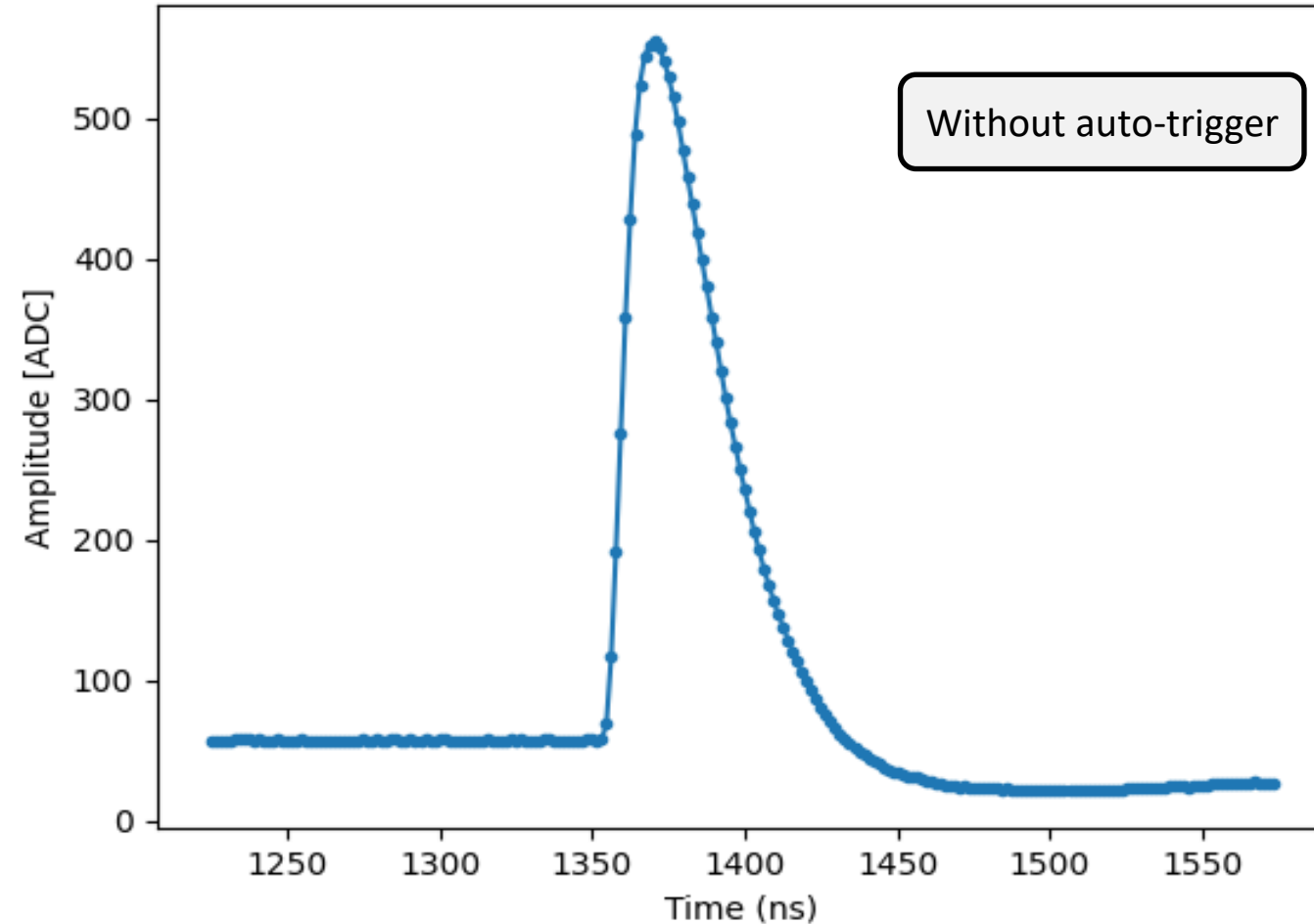


- Using internal injection of the ASIC:
 - Done by doing several runs and shifting the injection
 - Move to 1 sample every ~25 ns to 16 samples

- Injection synchronous to the sampling
 - Confirms the noise is due to digital coupling

- Investigation in progress
 - Noise correlated with preamp gain
 - Internal or PCB coupling ?

Signal vs time for channel 26 with a phase offset of 0



Main investigation for the coming months of measurements

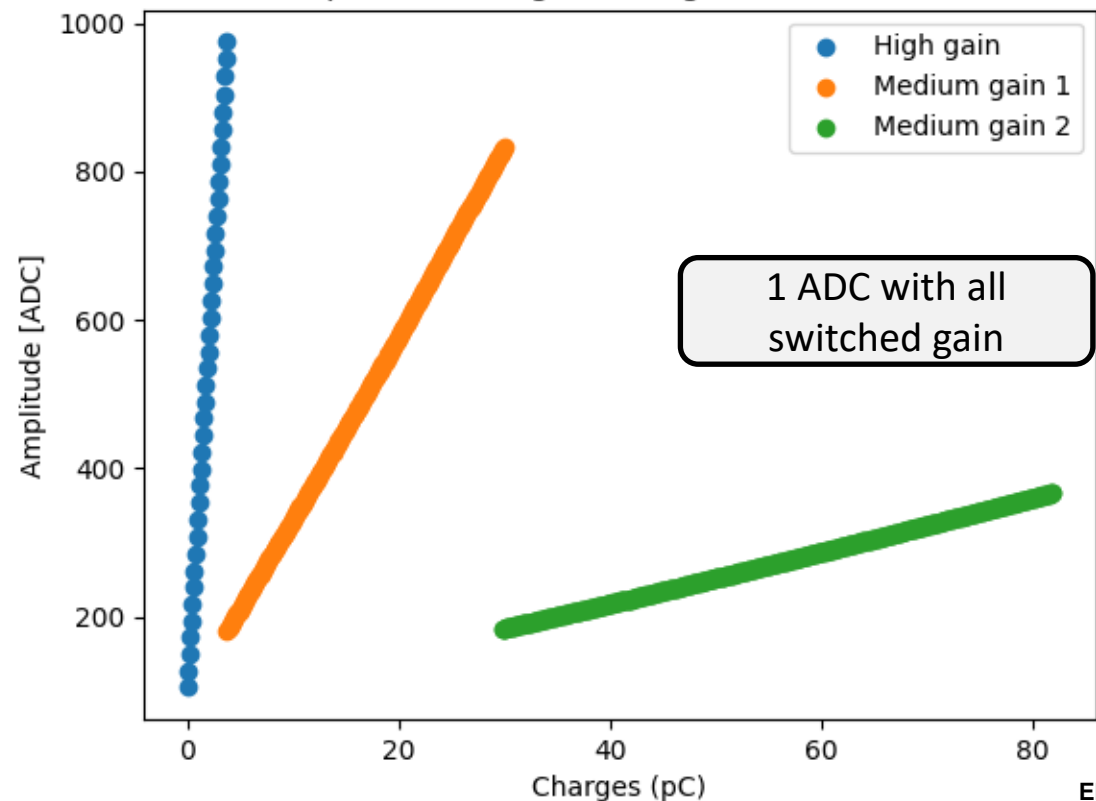
Full chain ASIC response for each mode

- ❑ Previous measurements done using the 1 ADC configuration with gain switching active
- ❑ 2 ADCs mode possibility (1 ADC forced to high-gain and second one linked to switched gain)

1 ADC mode

ADC peak vs charge for all gains in channel 26

Without auto-trigger

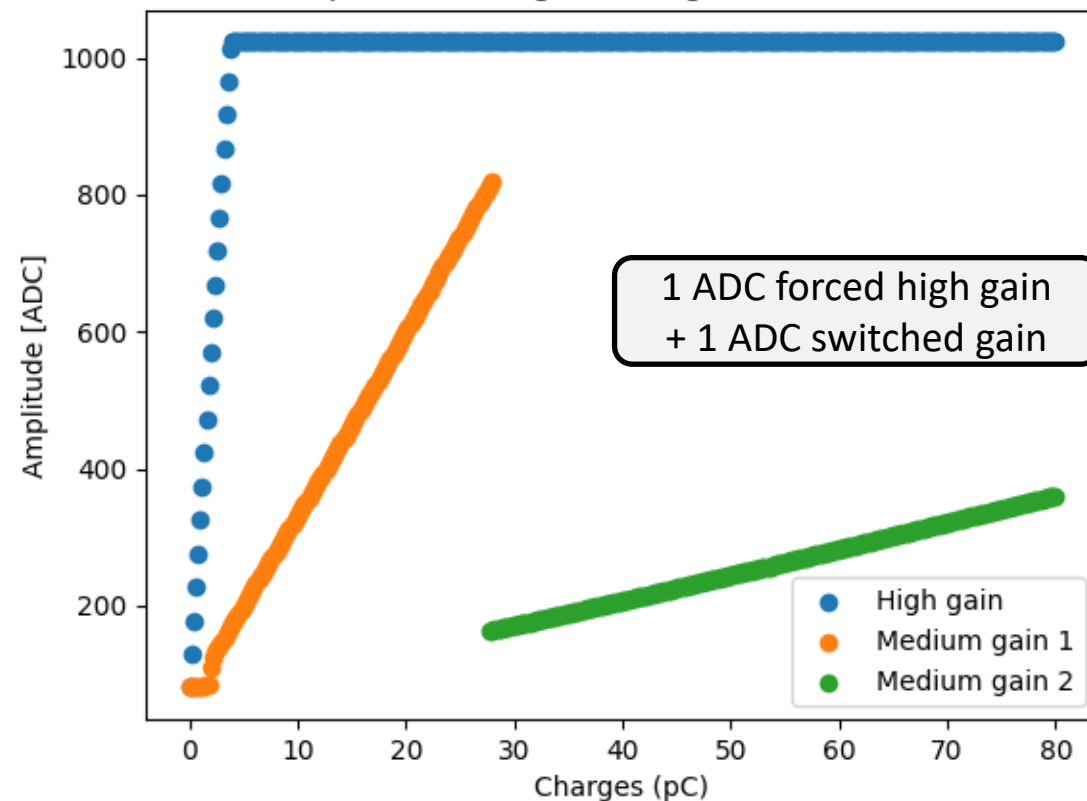


1 ADC with all switched gain

EIC 2026

2 ADCs mode

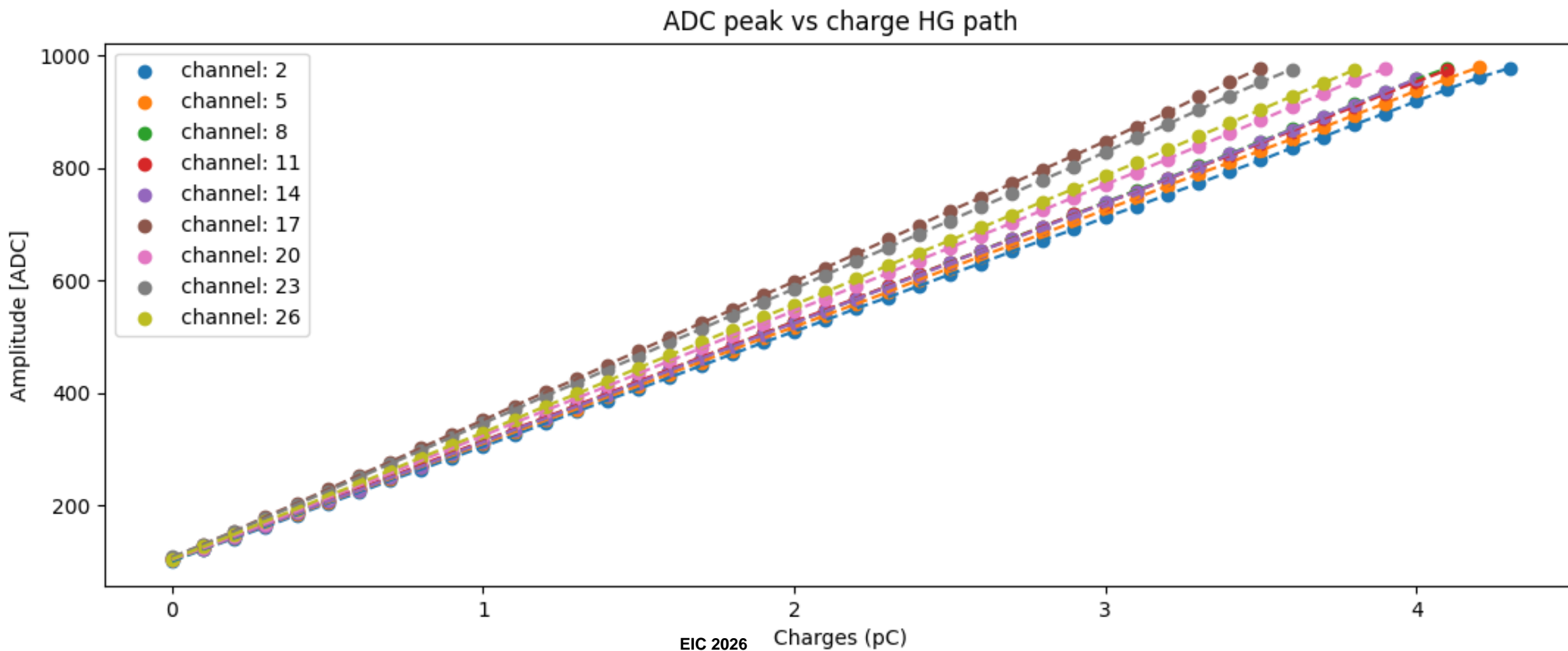
ADC peak vs charge for all gains in channel 26



1 ADC forced high gain + 1 ADC switched gain

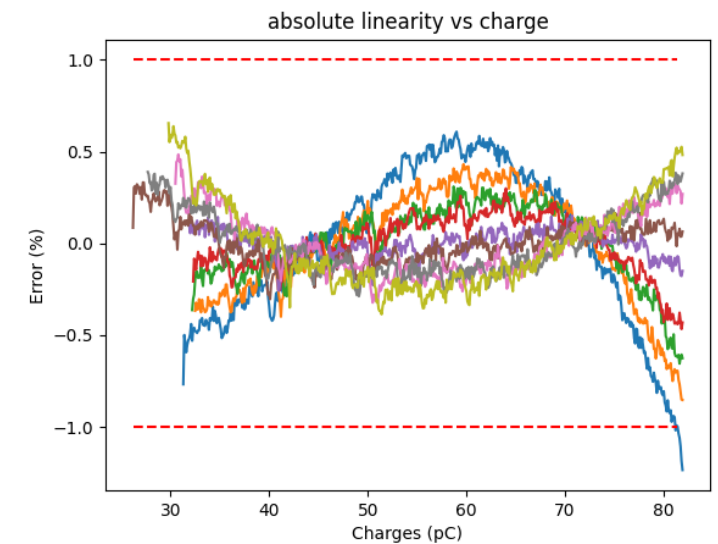
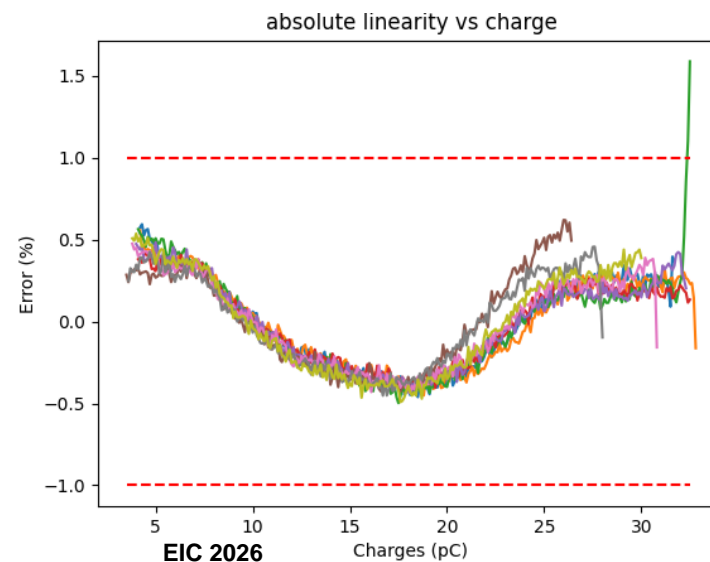
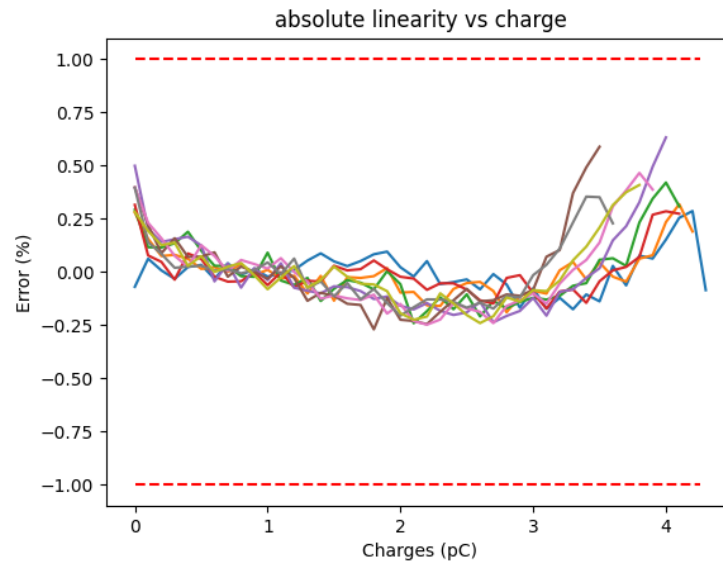
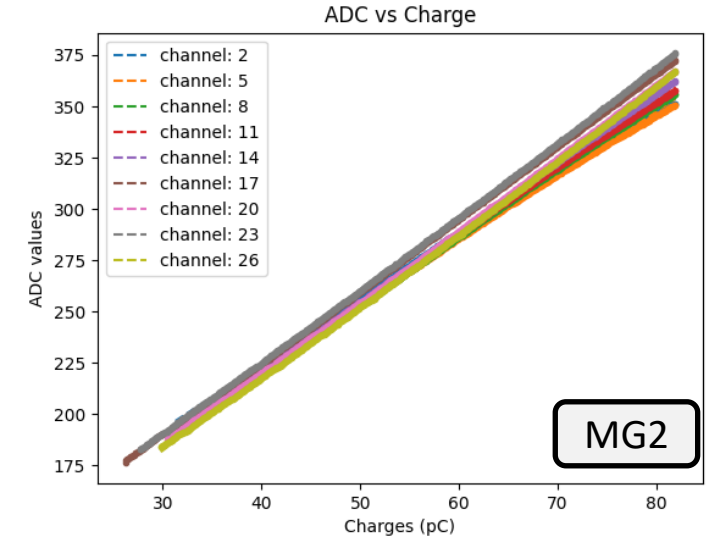
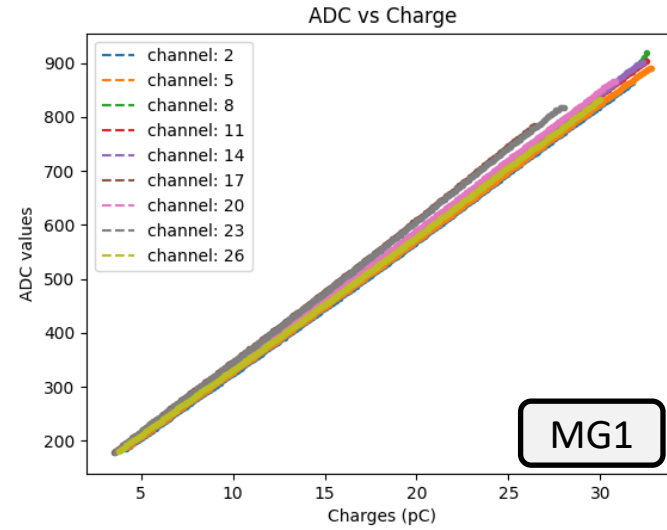
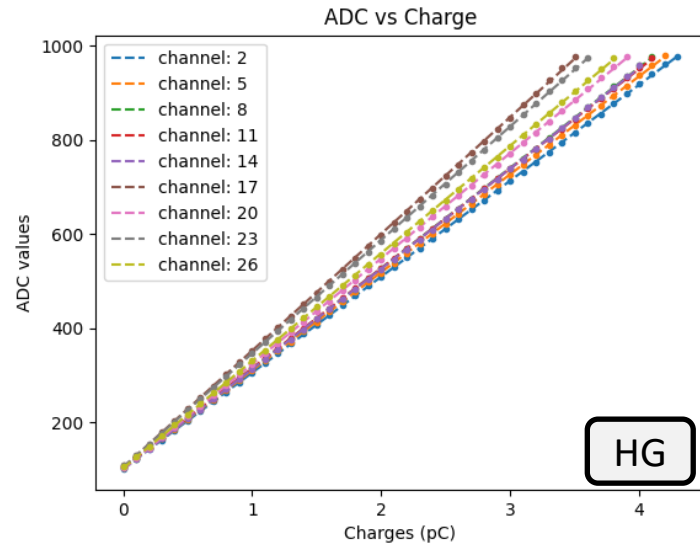
Gain uniformity over channels

- ❑ Gain disparity observed with a maximum difference of 13% less gain
- ❑ Mainly due to the parasitic resistance between the injection DAC and channels
- ❑ External injection (new PCB) is needed to measure the effective gain uniformity



□ Linearity measured at the peak of the signal

□ Using external trigger



CALOROC integration and power supply consideration (Sept 2025)

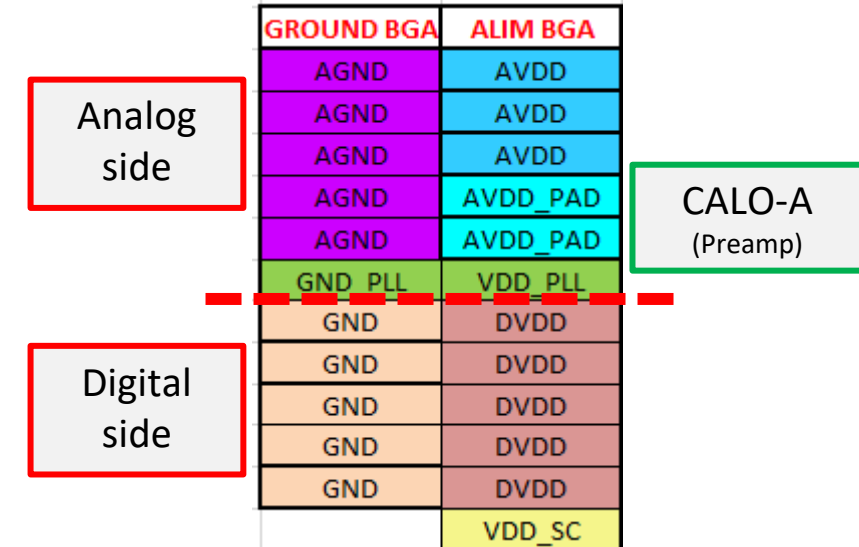


- On the board, CALOROC will need a maximum of 3 power supplies:
 - Analog / Digital + 1 dedicated for CALOROC-A (Preamp)
 - (Not shown here: LED power and HV)



JEDEC MO-216 – 17 x 17 mm BGA version

Digital side										Analog side									
MAPPING CALOROC_1 BGA 400 (TOP VIEW)																			
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SDA	RSTB_I2C	HARD_RSTB	SOFT_RSTB	ERROR	CK_320_N	CK_320_P	FCMD_P	FCMD_N	AD<4>	CHIP_R	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND
SCL	GND	GND	GND	GND	GND	VH110<0>	VH110<1>	FLAG_AF	AD<4>	VREF_ADC	AGND	AVDD	AGND	IN<0>	AGND	IN<1>	AGND	NC	VDDA_PAD
DAC_ALDO	GND	GND	GND	GND	GND	NC	NC	FLAG_AF	AD<4>	VCM_ADC	AGND	AVDD	AGND	IN<2>	AGND	IN<3>	AGND	NC	VDDA_PAD
NC	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	D<0>	AVDD	AVDD	AVDD	AGND	IN<4>	AGND	IN<5>	AGND	NC	VDDA_PAD
NC	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	D<0>	AVDD	AVDD	AVDD	AGND	IN<6>	AGND	IN<7>	AGND	NC	VDDA_PAD
OUT_TSPFF	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	D<0>	AVDD	AVDD	AVDD	AGND	IN<8>	AGND	IN<9>	AGND	AGND	AGND
SIPM_CALIB	NC	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	D<0>	AGND	AGND	AGND	AGND	IN<10>	AGND	IN<11>	AGND	NC	VREF_SK_LP
NC	NC	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AGND	AGND	AGND	AGND	AGND	IN<12>	AGND	IN<13>	AGND	AGND	AGND
STROBE_EXT	NC	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AGND	AGND	AGND	AGND	AGND	IN<14>	AGND	IN<15>	AGND	NC	VREF_NOINV_SK
EFUSE	NC	GND	DVDD	VDD_PLL	VDD_PLL	AGND_PLL	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<16>	AGND	IN<17>	AGND	NC	VREFINV_VBM3PA
TRIG_P	NC	GND	DVDD	VDD_SC	VDD_SC	AGND_PLL	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<18>	AGND	IN<19>	AGND	NC	VREFTOA_VBM3PA
TRIG_N	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<20>	AGND	IN<21>	AGND	NC	VREFTOA_VBMPA
DAQ2_P	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<22>	AGND	IN<23>	AGND	NC	VBG_IV
DAQ2_N	PLL_LOCK	GND	DVDD	VDD_SC	VDD_SC	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<24>	AGND	IN<25>	AGND	NC	PROBEPVA_VBOPA
DAQ3_P	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	D<0>	AVDD	AVDD	AVDD	AVDD	IN<26>	AGND	IN<27>	AGND	NC	INCTEST
DAQ3_N	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	D<0>	AVDD	AVDD	AVDD	AVDD	IN<28>	AGND	IN<29>	AGND	NC	VDDA_PAD
ADD<3>	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	D<0>	AVDD	AVDD	AVDD	AVDD	IN<30>	AGND	IN<31>	AGND	NC	VDDA_PAD
ADD<2>	GND	GND	GND	GND	GND	NC	NC	NC	VCM_ADC	AGND	AVDD	AGND	AGND	IN<32>	AGND	IN<33>	AGND	NC	VDDA_PAD
ADD<1>	GND	GND	GND	GND	GND	NC	NC	NC	VREF_ADC	AGND	AVDD	AGND	AGND	IN<34>	AGND	IN<35>	AGND	NC	VDDA_PAD
ADD<0>	PROBE_TOT_PA	PROBE_TOA	PROBE_DC2	PROBE_DC1	PROBE_INV	VNEG	VH110<2>	PROBE_NOINV	TRIG<EXT>	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND



Board power	Nominal value	ASIC power	Max ratings
Analog power	1.2 Volts	AVDD, VDD_PLL	8 mW / chn
Preamp power	2.5 or 1.2 Volts (CALO-A or CALO-B)	AVDD_PAD	2 mW / chn
Digital power	1.2 Volts	DVDD	3 mW / chn

April 2026 update:

- Measurement of 12 mW / channel
- Without auto-trigger and zero suppress

ASIC sanity checks

- Power consumption of each part
- Bias value versus simulation

CALOROC-A
50% done

CALOROC-B
80% done

Validating interfaces (could be done in parallel)

- Accessing the parameters (I2C only)
- Reading ASIC output (high speed serial links)

CALOROC-A
50% done

CALOROC-B
80% done

At this stage, more in-depth characterization tests could be performed

ASIC front-end characterization

- Linearity / Noise
- Analog to digital conversion
- Timing measurements**
- CALO-A: Reproduce H2GCROC performances
- CALO-B: Validation of switch-gain mechanism

CALOROC-A
Not started

CALOROC-B
Started

Results will drive CALOROC2 design → Q1 2027
Focus on noise / timing measurements

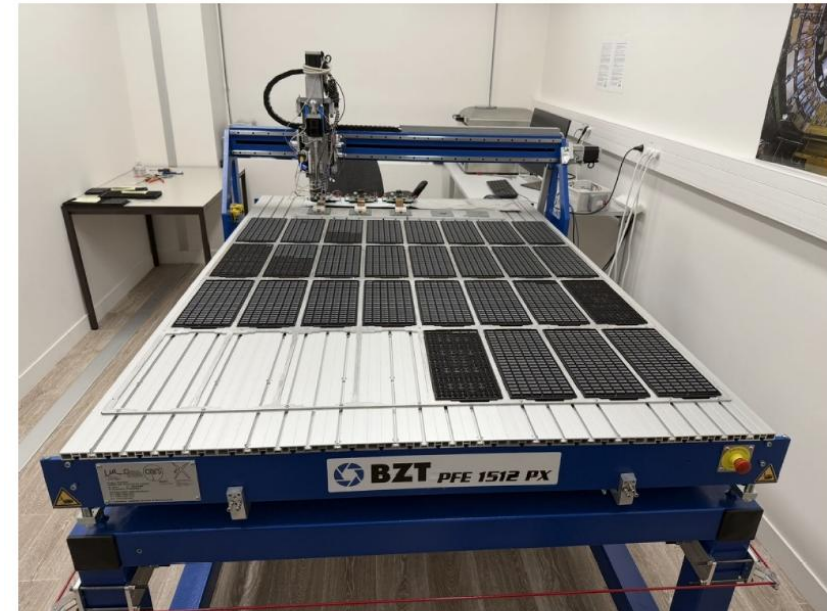
- ❑ Expertise in radiation-hardened front-end ASICs for HEP
 - ❑ HL-LHC ASICs: ATLAS HGTD and CMS HGCAL (10^5 ASICs)
- ❑ Expertise in irradiation testing (dose and displacement)
 - ❑ HL-LHC levels 200 Mrad and 10^{16} n_{eq} / cm^2 (1 MeV equivalent neutrons)
- ❑ Standard interfaces ensures a full compatibility with our robot
 - ❑ 2x 50 ASICs tested per hour (H2GCROC) with QR code scan

- Feedback from H2GCROC in 2026:
- 70% yield after testing (10k ASICs)
 - 250 chips / day / robot
 - Robots available in 2027

 - Database management, robot setup and mechanical structure done by LLR



LLR robot: processing of LD (Si and SiPM)



OMEGA robot: processing of HD (Si)

Documents history

VERSION	DATE	MODIFICATION
1.0	5 Sept, 2025	First release
1.1	3 Oct, 2025	Update with LLR comments + BGA/C4 mapping
1.2	12 Mar, 2026	Update operating modes, fast commands, I2C, CRC, 1 ADC mode
1.3	14 Apr, 2026	SC parameters update

MAPPING CALOROC_1 BGA 400 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	SDA	RSTB_I2C	HARD_RSTB	SOFT_RSTB	ERROR	CK_320_N	CK_320_P	FCMD_P	FCMD_N	ADD<4>	CHIP_R	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND
B	SCL	GND	GND	GND	GND	GND	VH10<0>	VH10<1>	FLAG_AF	ADD<4>	VREF_ADC	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND
C	DAQ1n_daq1n	GND	GND	GND	GND	GND	NC	NC	FLAG_AF	NC	VCM_ADC	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND
D	NC_daq1n	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
E	OUTF_daq1n	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
F	NC	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
G	SIPM_CALIB	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
H	NC	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
J	STROBE_EXT	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
K	EFLISE	NC	GND	DVDD	VDD_PLL	VDD_PLL	AGND_PLL	GND	GND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
L	TRIG_P	NC	GND	DVDD	VDD_SC	VDD_SC	AGND_PLL	GND	GND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
M	TRIG_N	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
N	DAQ2_P	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
P	DAQ2_N	PLL_LOCK	GND	DVDD	VDD_SC	VDD_SC	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
R	DAQ3_P	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
T	DAQ3_N	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
U	ADD<3>	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
V	ADD<2>	GND	GND	GND	GND	GND	NC	NC	NC	NC	VCM_ADC	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND
W	ADD<1>	GND	GND	GND	GND	GND	NC	NC	NC	NC	VREF_ADC	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND
Y	ADD<0>	PROBE_T0F_PA	PROBE_TOA	PROBE_DC2	PROBE_DC1	PROBE_INV	VNEG	VH10<2>	VH10<3>	PROBE_NONVW	TRIG2_EXT	TRIG1_EXT	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND

- ❑ Detailed datasheet for CALOROC1-B
 - ❑ Available in version 1.3 (**only distributed to first users**)
 - ❑ Includes interfaces – Parameters – EIC fast commands
 - ❑ HL-LHC ASICs: ATLAS HGTD and CMS HGCAL (10⁵ ASICs)

- ❑ Available ASIC pinout (also part of the datasheet)
 - ❑ Common to all CALOROCs

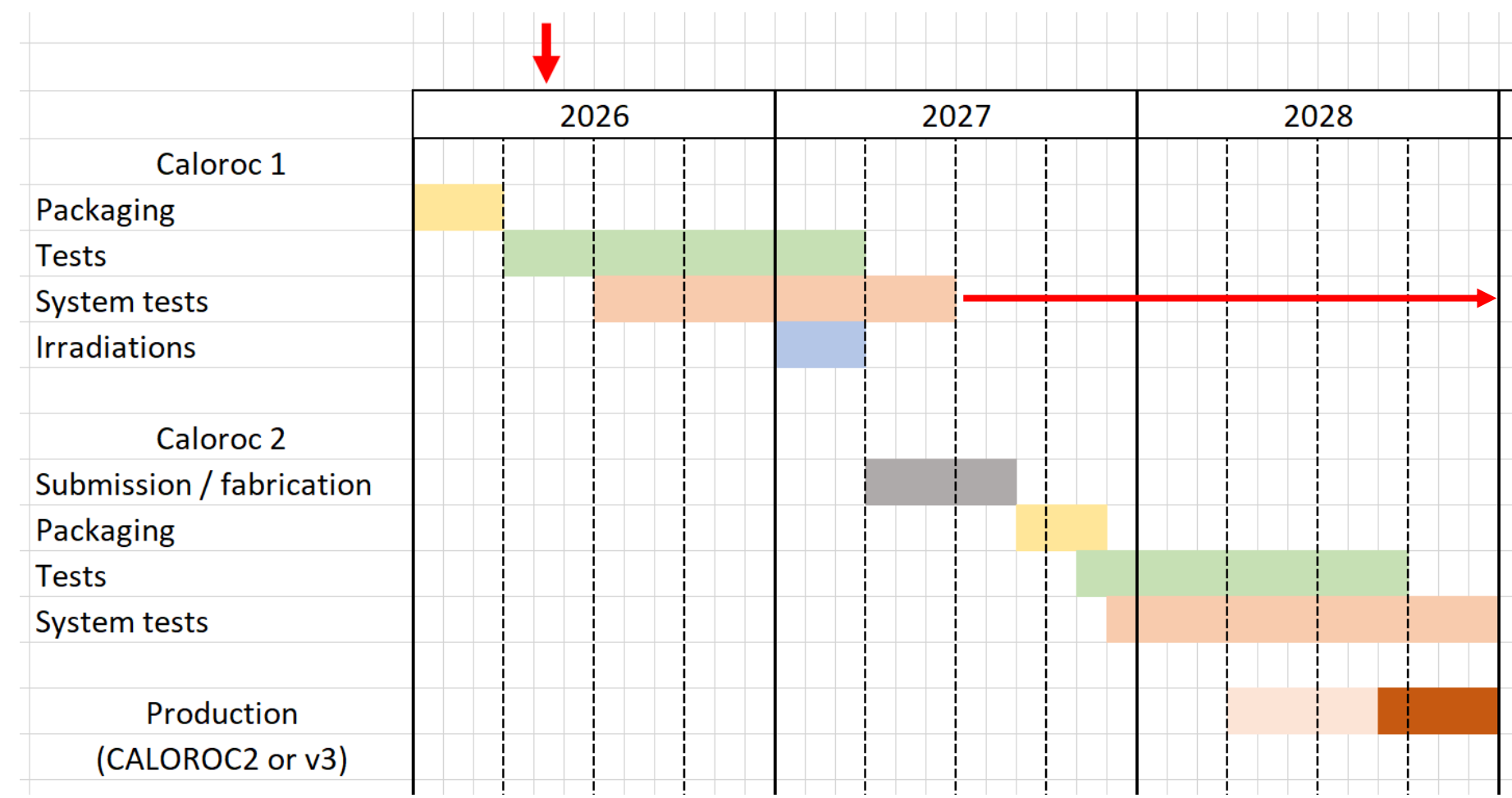
- ❑ Preliminary CALOROC “Tests and Acceptance Criteria”
 - ❑ Derived from H2GCROC robot serial tests

CALOROC Quality Control: Tests and Acceptance Criteria

Abstract: This document is based on the work carried out by the LLR and OMEGA groups on quality checks for the HGCROC and H2GCROC ASICs. Two robots were set up to automate the various tests, depending on whether the chosen package is High Density (HD) or Low Density (LD). Since CALOROC is largely derived from H2GCROC, a significant part of the quality checks will be equivalent and are described in this document.

Timeline / System tests

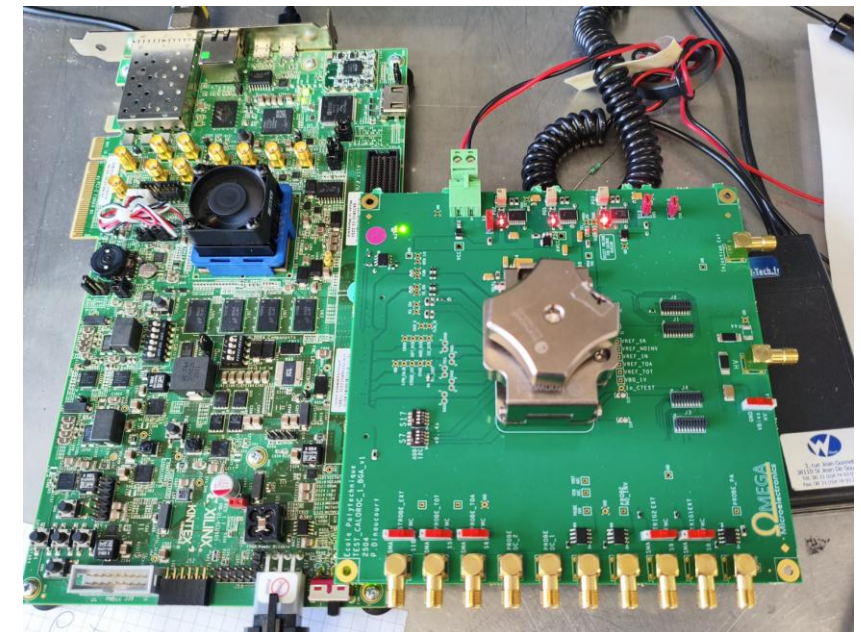
- ❑ CALOROC timeline – 2026 to 2028
 - ❑ First fabrication completed in Dec 2025 (Eng. Run)
 - ❑ Only 28 ASICs per variant of CALOROC1
 - ❑ Second fabrication foreseen in March 2027



CALOROCs provided (May 26):

- 12 ASICs for LLR FEB (A+B)
- 2 ASICs for ORNL (A)
- 3 for testboards (B)

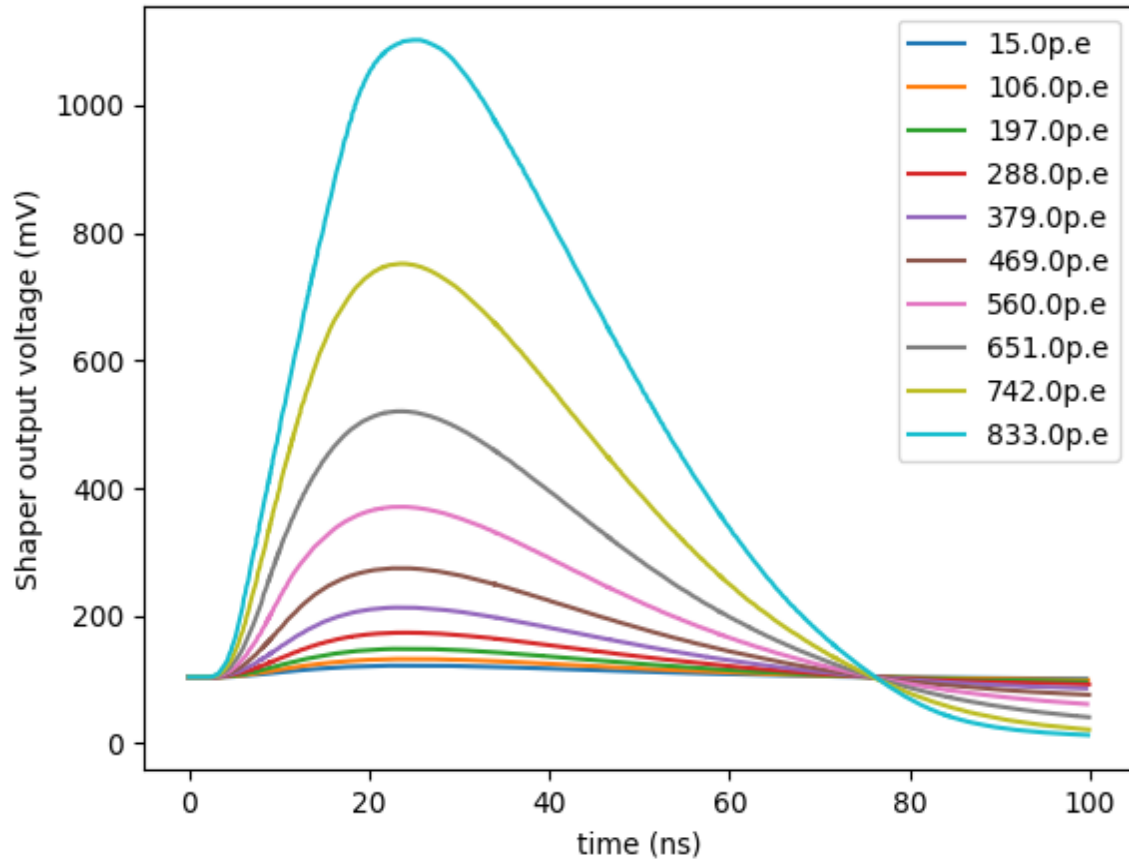
- ❑ CALOROCs received in April 26
 - ❑ Small quantities (28 x 2). Remaining one (100x2) in 4 months
- ❑ CALOROC-A analog measurements delayed
- ❑ CALOROC-B first measurements are encouraging and will focus on:
 - ❑ Noise investigation
 - ❑ Timing measurements
 - ❑ Crosschecks on our 2 different testboards
- ❑ Possible actions for investigation
 - ❑ “Noise analysis” testboard (3 months to fabricate)
 - ❑ New substrate (4 months to fabricate)
 - ❑ FEB crosschecks
- ❑ CALOROC2 in March 27
 - ❑ If noise understood + timing measurements OK



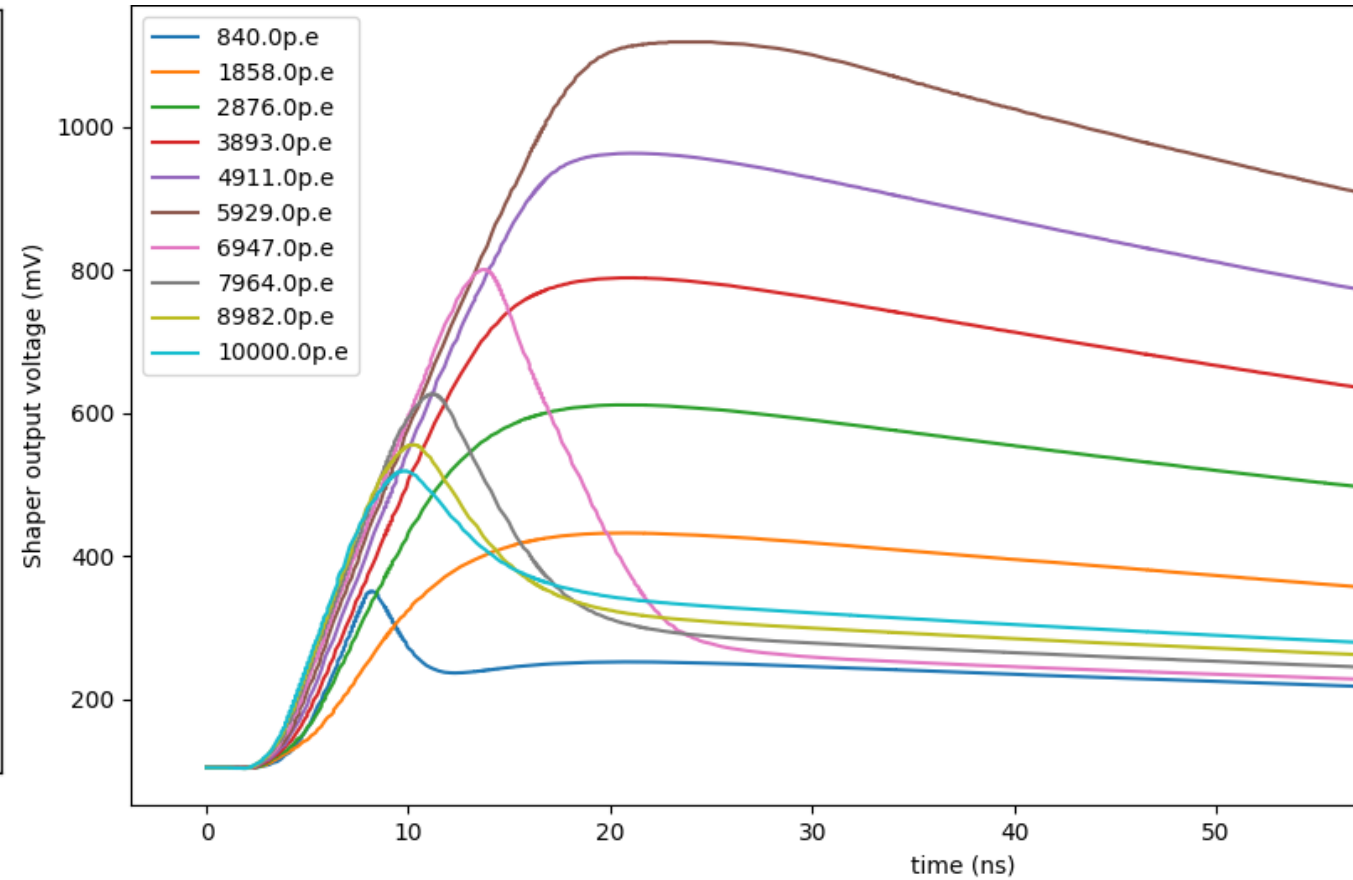
□ Waveform for HG on the left + gain switching on the right:

□ Example with Cd of 8.96 nF

Waveform for high gain shaper @8.96nf configuration



Waveform for medium gain shaper @8.96nf configuration

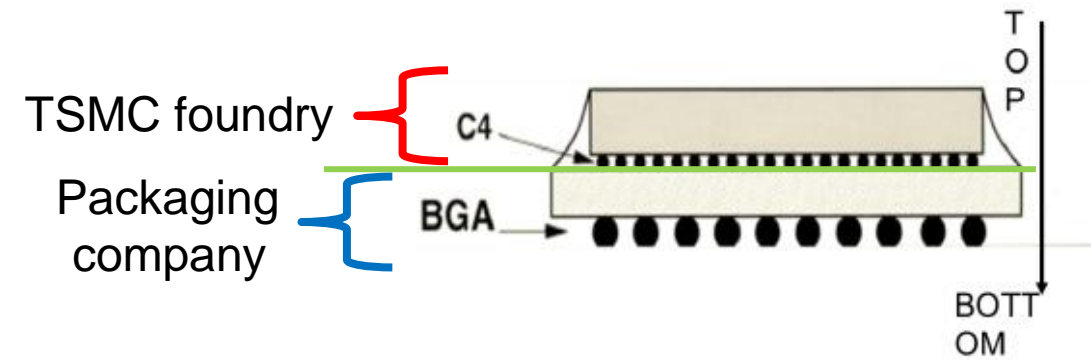


- ❑ The SiPM configuration has a direct impact on the SNR
 - ❑ SNR for 1p.e is proportional to Q/C (larger SiPM cap decrease SNR)
 - ❑ Gain of $1.8e5$ electrons per p.e (table below)
- ❑ CALOROC1b will be able to readout SiPM in the range ~ 560 pF to 8.96 nF
 - ❑ Timing measurements will focus on the MIP ($\sim 15pe$)

Operation modes	1 SiPM of 560pF Caloroc1B	4 SiPMs of 560pF Caloroc1B	16 SiPMs of 560pF Caloroc1B	1 SiPM of 560pF Caloroc1A
Cin	560pF	2.24nF	8.96nF	560pF
Dynamic range in charge (Noise - Max)	3.2fC-190pC	11fC-790pC	45fC-3.17nC	20fC-320pC
Input time constant (occupancy related)	112ns	450ns	450ns	10ns
Jitter @ MIP ($\approx 400fC$)	42ps	130ps	520ps	400ps
SNR @ 1p.e ($\approx 30fC@gain=1.8e5$)	9	2.6	0.64	1.44

❑ CALOROC will have the same package as the existing HKROC:

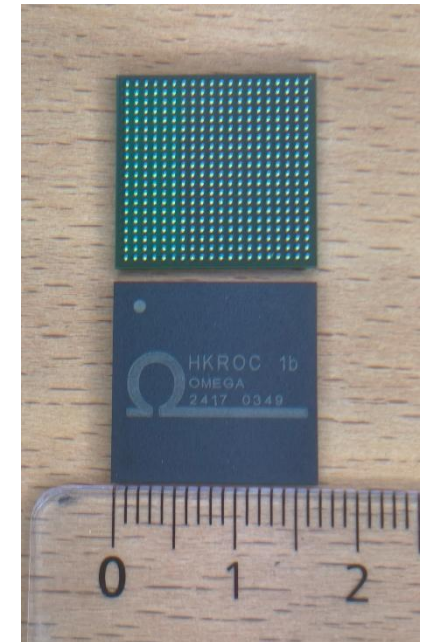
- ❑ JEDEC MO-216 – 17 x 17 mm BGA version
- ❑ 400 balls with 0.8 mm pitch
- ❑ Specific substrate (interposer) designed at OMEGA
- ❑ **QR code** like HGCROC3

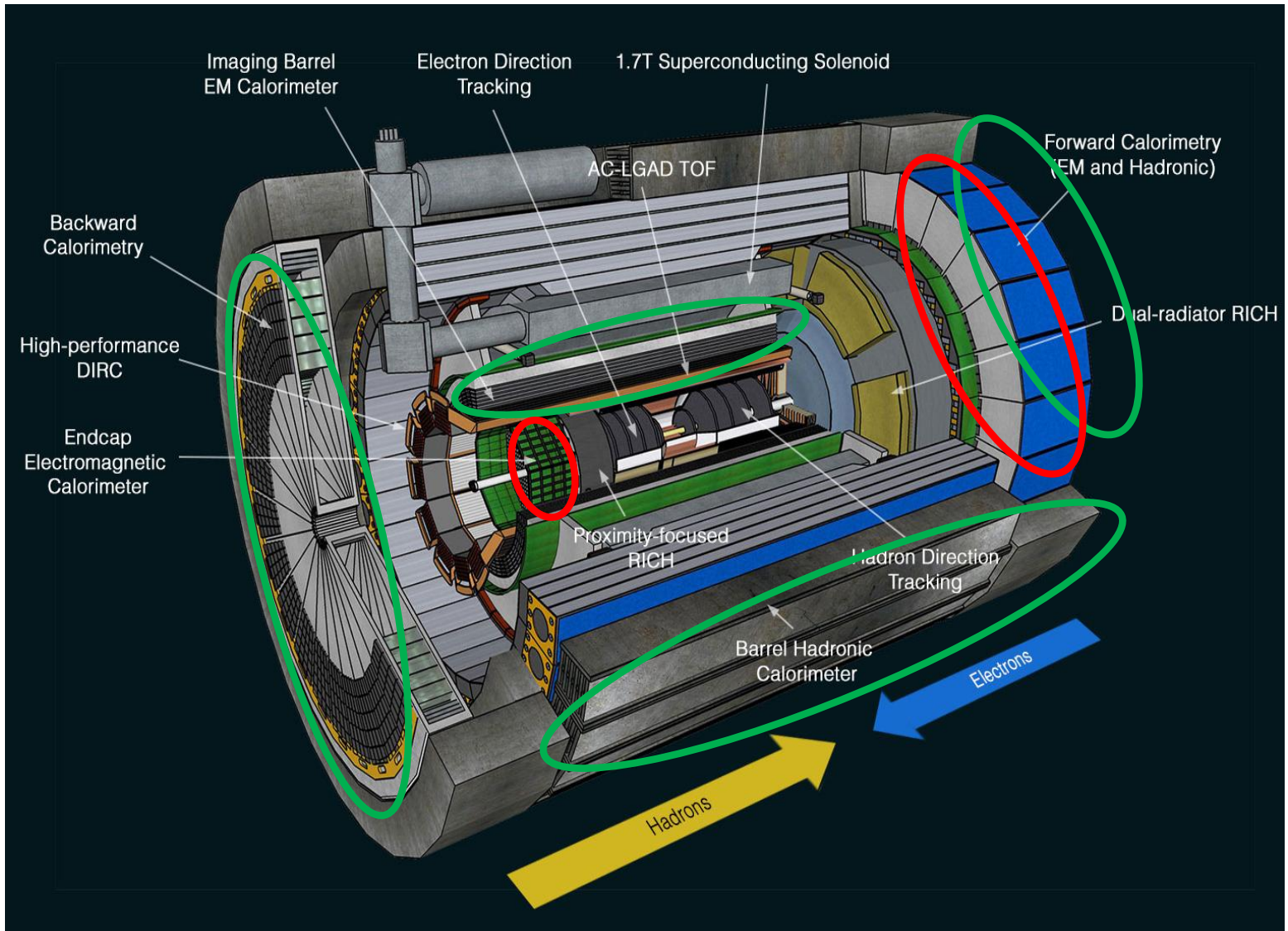


JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: THIN PROFILE, SQUARE AND RECTANGULAR, BALL GRID ARRAY FAMILY, 1.00 & 0.80 mm PITCHES	ISSUE: E	DATE: AUG 2003	MO-216
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TABLE 3: SQUARE VARIATIONS – 0.80 PITCH

D / E	e = 0.80							
	MD/ME	N	SD/SE	VARIATION	MD-1/ME-1	N	SD/SE	VARIATION
14.00	17	289	0.00	BAJ-1	16	256	0.40	BAJ-2
15.00	18	324	0.40	BAK-1	17	289	0.00	BAK-2
16.00	19	361	0.00	BAL-1	18	324	0.40	BAL-2
17.00	20	400	0.40	BAM-1	19	361	0.00	BAM-2





13 Calorimeters:

7 x SiPM – CALOROC

5 x SiPM – Discrete

1 x SiPM – Commercial fADC250

From J. Landgraf
(IDR review)

