Journal of
Instrumentation

CALOROC1B, an integrated front-end ASIC to readout SiPMs for the ePIC detector at EIC

To cite this article: P. Dumas *et al* 2025 *JINST* **20** P11024

Jinst

Published by IOP Publishing for Sissa Medialab

Received: *October 16, 2025*
Accepted: *November 15, 2025*
Published: *November 28, 2025*

CALOROC1B, an integrated front-end ASIC to readout SiPMs for the ePIC detector at EIC

P. Dumas,[a,*] F. Bouyjou,[b] P. Dinaucourt,[a] C. de La Taille,[a] F. Dulucq,[a] A. El Berni,[a] S. Extier,[a] M. Firlej,[c] T. Fiutowski,[c] F. Guilloux,[b] M. Idzik,[c] J. Moron,[c] K. Swientek[c] and D. Thienpont[a]

[a] *OMEGA, CNRS, École polytechnique, Institut Polytechnique de Paris,*
Route de Saclay, 91120 Palaiseau, France
[b] *IRFU, CEA, Université Paris-Saclay,*
GIF-SUR-YVETTE, France
[c] *AGH University of Krakow,*
Krakow, Poland

E-mail: `pedro.dumas-ziehlmann@omega.in2p3.fr`

Abstract: The CALOROC1B ASIC has been designed to read out the SiPMs for the ePIC detector at the EIC collider. Each of its 36-channels is composed of a high-gain preamplifier, two low-power preamplifiers, a dynamic gain switching mechanism, a shaper, and two ADCs to measure the energy, with a discriminator connected to a TDC for time-of-arrival measurements. This work presents the ASIC architecture and its simulation results. The ASIC has been designed to read large SiPMs (up to 10 nF), be resilient to radiation, and have a large dynamic range (up to 140k measured as Qmax/Noise) while keeping a good resolution.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; Radiation-hard electronics

2025 JINST 20 P11024

---

[*] Corresponding author.

https://doi.org/10.1088/1748-0221/20/11/P11024

Contents

1 Introduction 1

2 Architecture choice 1

3 Simulation results 2
  3.1 Time to baseline and occupancy 2
  3.2 Charge resolution for different SiPMs 3
  3.3 Time resolution simulations 4
  3.4 Linearity 4

4 Conclusion and next steps 5

1 Introduction

In the context of the electron-ion collider (EIC) at Brookhaven, which aims to increase our understanding of the properties of the nuclei [1]. The CALOROC1B chip was developed to read large-area SiPMs (from 320 pF up to 10 nF) at the calorimeter of the electron-proton/Ion collider (ePIC) detector.

This experiment not only requires a front-end circuit that is capable of reading these large SiPMs, but also demands this circuit to handle a large dynamic range (equivalent to a 16 bits ADC), have a power consumption of less than 15 mW per channel, comply with the resolution requirements, and have a time resolution of less than 1 ns. This should be achieved while maintaining a linearity error of less than 1%. To comply with these requirements, CALOROC1B was developed.

CALOROC1B is a 36-channel ASIC that employs a dynamic gain switching mechanism to increase its dynamic range without significantly increasing the power consumption while keeping a good resolution for low charges. This switching mechanism chooses the signal read by the ADC between three signal paths: a high gain path, a medium gain path and a low gain path. Also, the medium gain path incorporates an additional gain switching step, which allows us to have a total of four gains (2 bits) which are selected dynamically depending on the input charge.

2 Architecture choice

This gain switching mechanism is similar to that of AGIPD [2] or SITH [3]. Except that for CALOROC1B, we expect a signal may arrive every 10 ns. Which is too fast for doing a synchronous reset, and we want the baseline to stay constant until a signal arrives to prevent the dark noise from triggering the time of arrival (TOA) (This is important because CALOROC1B has a streaming readout). As a consequence, the architecture, gain switching and reset mechanism needs to be modified to take into account this constraints.

The architecture of CALOROC1B consists of 3 amplification paths per channel, which are connected to an analog multiplexer that chooses which path will be read by the ADC. A simplified schematic of the architecture of CALOROC1B can be seen in figure 1.

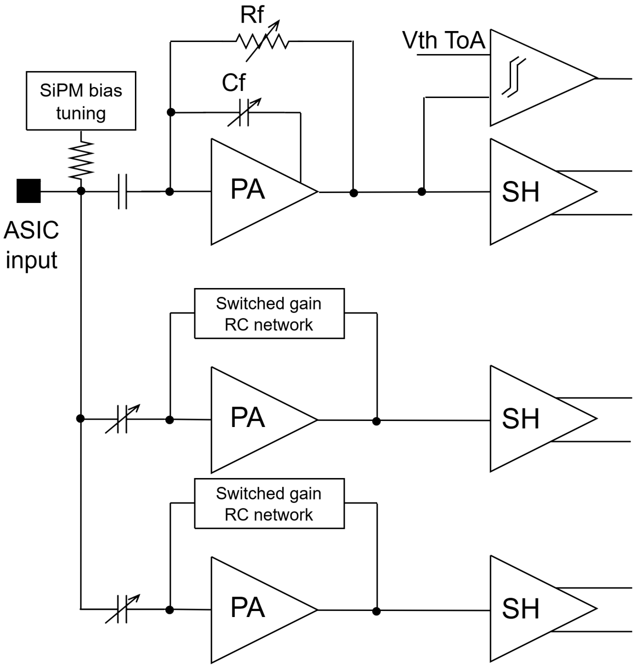


Figure 1. Schematic of the analog path of CALOROC1B composed of three preamplifier (PA) and three shapers (SH).

The gain paths were based on a previous circuit named HKROC [4], which uses a voltage amplifier configuration, which AC couples to the input. This configuration allows us to connect multiple amplification paths to the input without significantly altering the shape of the signal. Also, the AC coupling ensures a better signal-to-noise ratio than having a current conveyor as was done for H2GCROC [5], the downside of not using a current conveyor is lower occupancy, since it takes more time to return to the baseline after a signal arrives.

There are a total of 3 discriminators in the circuit used to trigger the gain switching mechanism, the first one, present in the high gain path, is used to switch from high gain to medium gain. Then the other two discriminators are on the medium gain path, one is used to switch the feedback resistance of the preamplifier (to reduce the nonlinearities) and the second one is used to switch from medium gain 1 to medium gain 2, and to switch from medium gain 2 to low gain if the pulse coming out of the discriminator is wide enough (which means that the preamplifier is saturated). Once triggered, the gain switching stays active for 75 ns to 100 ns before it resets to the default gain.

3 Simulation results

3.1 Time to baseline and occupancy

The time to baseline, which is the time it takes for a signal return to the DC value, depends on both the input RC constant, given by the SiPM capacitance and the value of R_{in} which can be chosen to be 50 Ω or 200 Ω. Using a 10 nF capacitance, our input time constant is $\tau = 500$ ns which gives us a time to baseline curve which can be seen in figure 2.

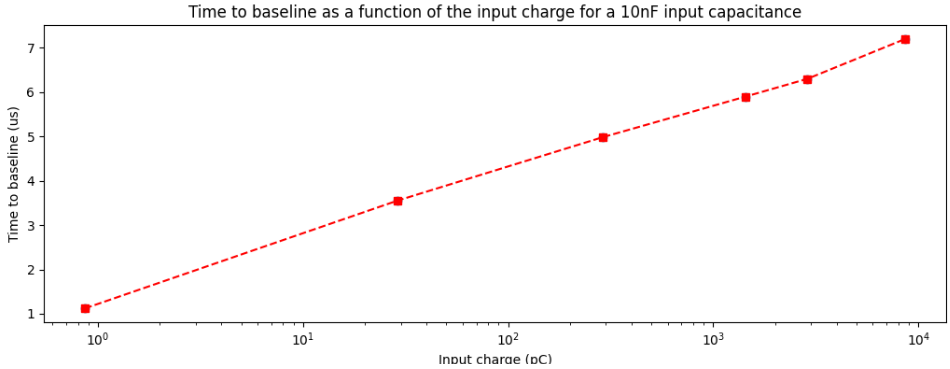


Figure 2. Simulated time to baseline.

This time constant could be reduced by using a smaller capacitance, although doing this could increase the electronic noise, therefore reducing the signal-to-noise ratio (SNR) assuming the same voltage amplitude for the input signal, if the charge is kept constant, then the SNR increases as the voltage $V = \frac{Q_{\text{in}}}{C}$ increases.

In the case of a time constant of $\tau = 100\,\text{ns}$ the electronic noise is doubled, although this increase in the noise could be fixed if the SiPM bias tuning is turned off. In this case the resistance is connected directly to ground and the noise stays near the value observed using the $\tau = 500\,\text{ns}$.

Since the hit rate per channel required by EIC (50 kHz) is lower than that required by Hyper-Kamiokande (1 MHz) [4], the time to baseline and occupancy requirements are lower than what was needed for HKROC [4]. Therefore we can accept the tradeoff of increasing the time to baseline and decreasing the occupancy in exchange for a higher SNR and lower jitter.

Although the time to baseline is in the order of the µs, the width of the signal at the time of arrival is less than 30 ns even for very large charges (1.44 nC using a 10 nF SiPM). This means that if we have two signals of similar magnitude, we should be able to measure them both if they arrive more than 30 ns apart from each other. This could be even lower (6 ns) for small signals (400 fC). If the second signal is an order of magnitude lower than the first one, then we won't be able to measure it since the signal's amplitude would be lower than the previous signal undershoot.

3.2 Charge resolution for different SiPMs

The following simulation results on table 1 show the dynamic range, input time constant, jitter and SNR simulated for different SiPMs for CALOROC1B. A column showing the measurement results for H2GCROC [5] was added to compare both circuits. The SiPM simulated had a gain of 1.8×10^5.

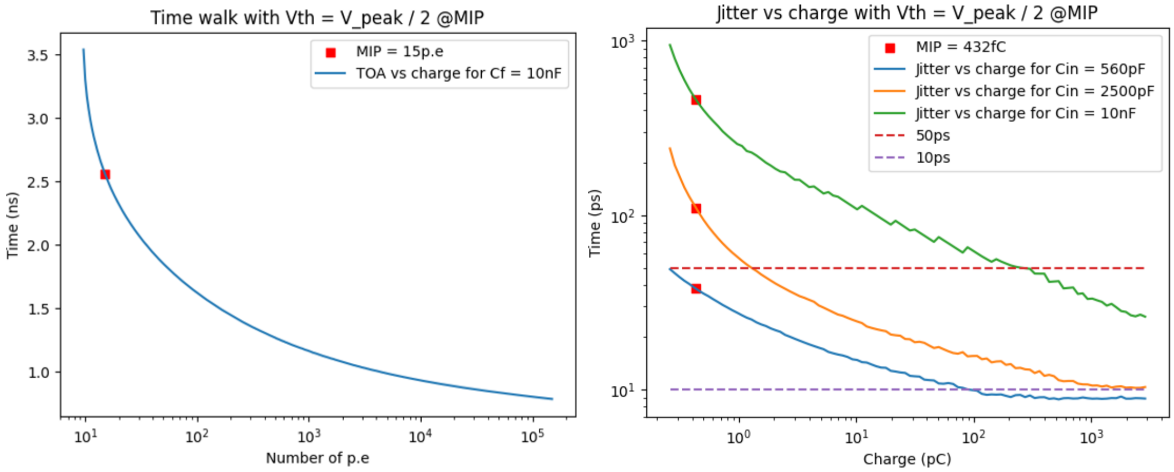
Table 1. Table of simulated results for multiple SiPM configurations.

Circuit	CALOROC1B	CALOROC1B	CALOROC1B	H2GCROC
SiPMs	1 SiPM of 560 pF	1 SiPM of 2.5 nF	4 SiPM of 2.5 nF	1 SiPM of 560 pF
C_{in}	560 pF	2.5 nF	10 nF	560 pF
Dynamic range (Noise — Q_{max})	2.6 fC — 190 pC	12 fC — 770 pC	48 fC — 3.1 nC	20 fC — 320 pC
Jitter @ MIP(432 fC)	35 ps	110 ps	470 ps	400 ps
SNR @ 1p.e (28.8 fC)	10	2.4	0.6	1.44
Q_{min}	43 fC	172 fC	690 fC	120 fC

We can observe that, as the SiPM capacitance, increases, the SNR decreases and the jitter increases (for a fixed charge). These simulations were made modifying the CALOROC1B parameters (controllable through slow control) to keep the electronic noise constant. The dynamic range shown in the table is the one achieved by using the default parameters for each capacitance, but the dynamic range can be doubled if needed in exchange for a reduced resolution for the low gain.

3.3 Time resolution simulations

The results for the time resolution simulations can be seen in figure 3(a) for the Time walk and figure 3(b) for the jitter, in which we can observe that the jitter is lower when the input capacitance is decreases.



(a) Time walk vs number of photons.

(b) Jitter vs number of photons.

Figure 3. Time resolution simulations.

It is worth mentioning that the time walk (3.5 ns) is considerably lower than that of H2GCROC (20 ns) [5]. This was achieved by using a high pass filter which allowed us to reduce the time walk in exchange for increasing the value of Q_{min} (The minimum charge measurable).

3.4 Linearity

When using the gain switching, a common cause for concern is the linearity of the measurement, especially close to the switching point. To decrease the nonlinearities, the time constant of the medium and low gain paths is increased to virtually infinite, while the gain switching is active. When measuring the linearity we consider the first point of the ADC (@25 ns) for the high gain and the second point of the ADC (@50 ns) when the gain switching was active. We can do this as CALOROC1B measures by default 4 points for each signal it detects (pedestal plus 3 points every 25 ns). Doing this, we can see in figure 4 a graph of voltage as a function of the input photons where each line corresponds to each different gain.

If we measure the absolute linearity error for each line individually, we obtain that the absolute nonlinearity error is less than 1% for each line.

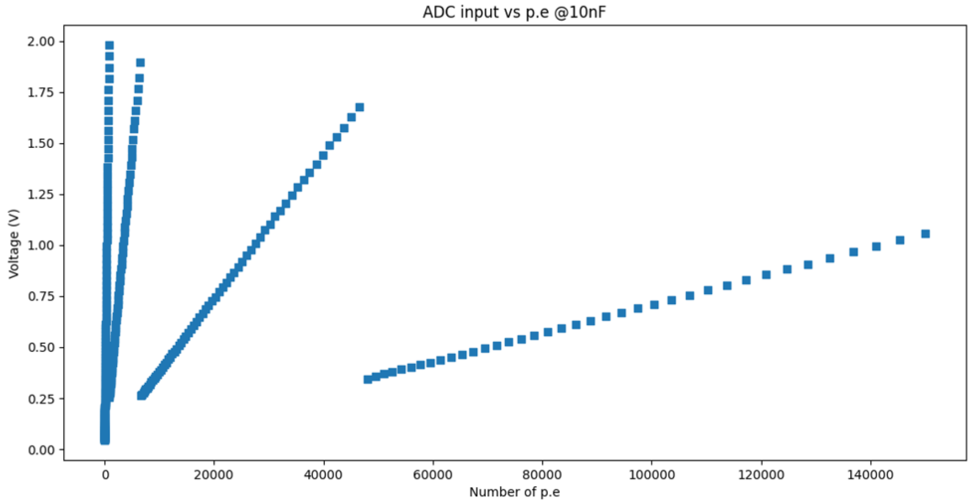


Figure 4. Voltage at the input of the ADC vs number of photons supposing a gain of 1.8×10^5 for the SiPM

4 Conclusion and next steps

As shown, CALOROC1B is a promising new circuit designed at Omega which is able to read large SiPMs (10 nF) while significantly improving the dynamic range and the resolution of both charge and time measurements compared to previous ASICs [4, 5] in exchange for a reduced hit rate and time to baseline. This particular implementation of the gain switching mechanism showed nonlinearity errors of less than 1% on simulations which is within the requirements for the ePIC detector. The next steps will be to characterize the ASIC through measurements once it is manufactured to confirm its simulated performance and find any errors we may have missed during the simulation phase.

References

[1] F. Willeke, *Electron Ion Collider Conceptual Design Report 2021*, BNL-221006-2021-FORE (2021) [`DOI:10.2172/1765663`].

[2] A. Allahgholi et al., *Megapixels @ Megahertz — The AGIPD high-speed cameras for the European XFEL*, *Nucl. Instrum. Meth. A* **942** (2019) 62324 [`arXiv:1908.02103`].

[3] I. D'Adda et al., *SITH: An SiPM Readout ASIC for Prompt Gamma-Ray Detection in Hadrontherapy Applications*, *IEEE Trans. Nucl. Sci.* **71** (2024) 2140.

[4] S. Conforti Di Lorenzo et al., *HKROC: an integrated readout chip designed to facilitate the readout of a large number of photomultiplier tubes for the next generation of neutrino experiments*, 2025 *JINST* **20** C02039.

[5] J. González Martínez, *Design and characterization of readout ASICs for SiPM detectors in pico-second timing measurements for the CMS HGCAL experiment*, Ph.D. thesis, Institut Polytechnique de Paris, Palaiseau, France (2024).