NUCLÉAIRE & PARTICULES

Omega

ÉCOLE POLYTECHNIQUE

IP PARIS

CALOROC for SiPM Readout at EIC

Internal ASIC Review

May 13 2026

OMEGA Microelectronics

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Organization for Micro-Electronics desiGn and Applications

ASIC & Discrete Readout Internal Reviews

Goals of the reviews:

- Provide a comprehensive assessment of the ASICs and Discrete Readout from design to production

    1. Specifications & Requirements - frontend, processing, interfaces, power and packaging (including form factors where applicable).
    2. Digital Interfaces - commands & controls
    3. Status & Steps to Completion - with schedule and to include testing/validation with detectors
    4. Production Outlook - to include final production review, production timeline and QA/QC testing
    5. Documentation - Functionality (e.g. User's Manual/Spec sheets) and QA/QC Plans, and with planned availability for FEB final designs and Engineering Articles, bump/wire bonding.

Review Schedule:

- EICROC - 1 April 2026
- ALCOR - 22 April 2026
- SALSA - 6 May 2026
- CALOROC - 13 May 2026
- FCFD - 20 May 2026
- Discrete - 27 May 2026

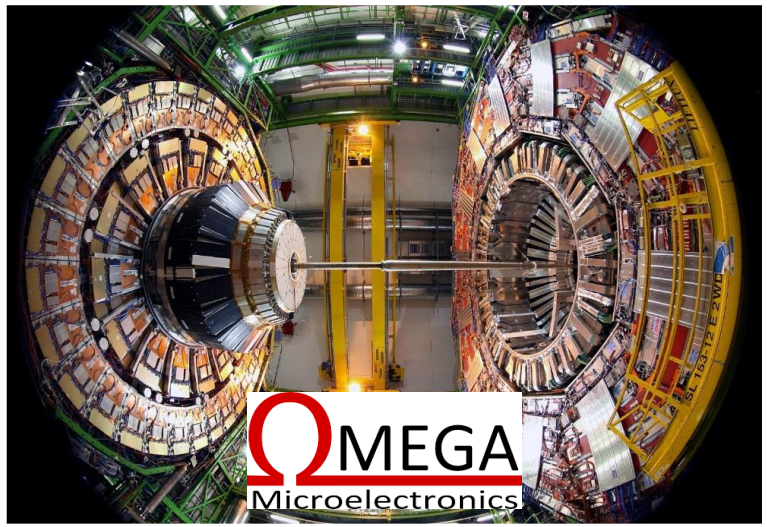
From H2GCROC to CALOROC

H2GCROC for the endcap calorimeter – Phase II

6M of Silicon channels
(+ 240k of SiPM)

Radhard (200 Mrad)
Low Power (15 mW per chn)
Precise timing (25 ps)

Total of 150k ASICs needed
Pre-prod this year



CALOROC for EIC

Same ASIC structure (floorplan)
Same ADC and TDC
Same readout

Common interfaces

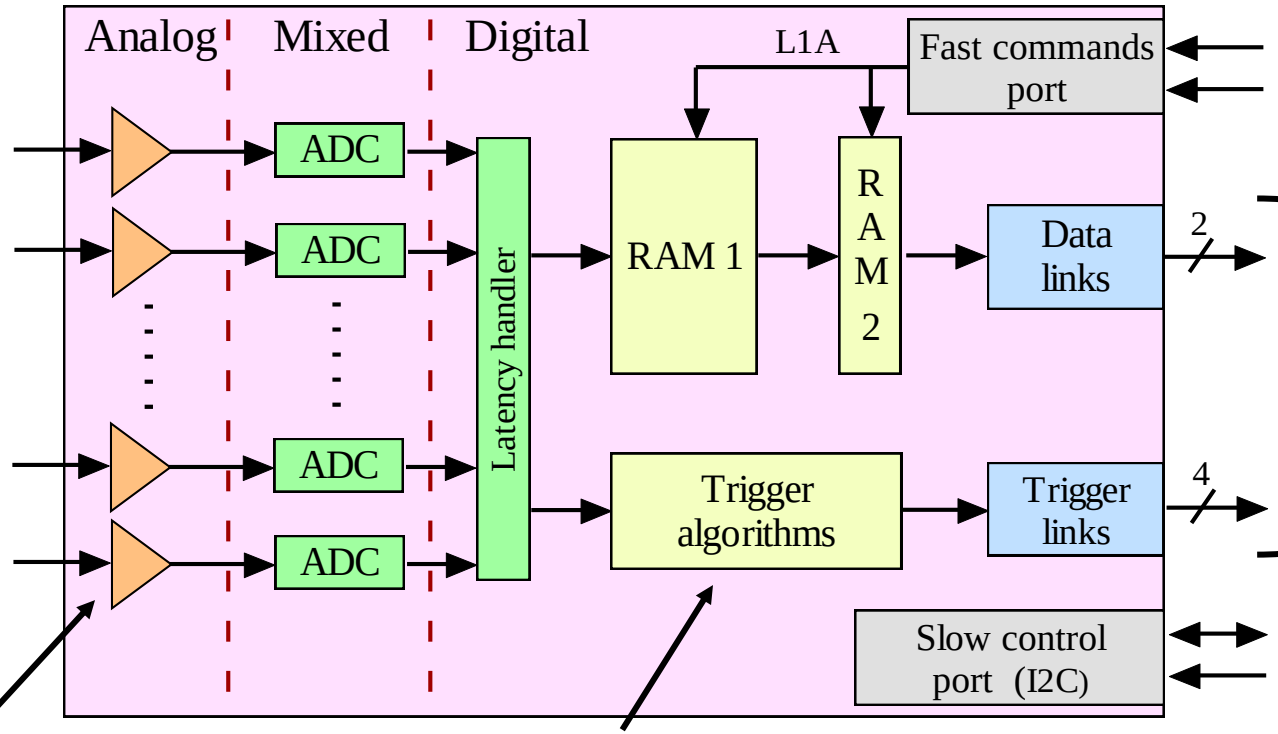
HEP trend => imaging calorimetry

- ❑ High number of channels
- ❑ Charge and precise timing (<100 ps)
- ❑ Low power + System-On-Chip

Based on H2GCROC, CALOROC will provide a versatile and low-power solution for SiPM readout

ROC chips standard structure

- H2GCROC (for SiPM readout) is an HL-LHC colored ASICs (external L1 trigger)
  - Below is an calorimetry structure (but interfaces for CALOROC will similar)



Dedicated fast command interface : calibration pulses, external L1 trigger.

Data and trigger serial links with CLPS signaling (LpGBT @ 1,26 Gbps)

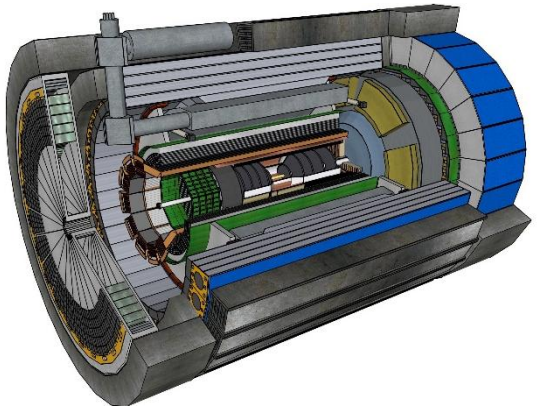
Analog front-end specific to sensor

LHC-like structure :
Ram1 for data storage
Ram2 for L1 accepted events

I2C interface to load the ASIC parameters (slow control interface)

What is CALOROC ?

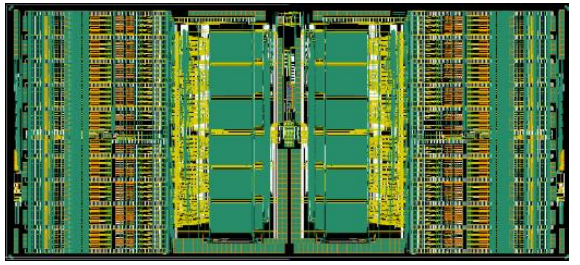
- CALOROC will be available in 2 versions for SiPM readout:
  - SiPM range capacitance from 560 pF to 8.96 nF
  - ~ 10-15 mW / channel
  - Radiation hardening (HL-LHC levels)
    - 200 Mrad and 10^{16} n_{eq} / cm^2 (1 MeV equivalent neutrons)
    - SEE hardening on control logic
  - Charge and time measurement



- Streaming readout (no external trigger required)
- Conservative CALOROC1A based on CMS H2GCROC:
  - H2GCROC (ADC, TOT) analog/mixed reuse
  - Back-end compatible with EIC + zero-suppress

- New CALOROC1B based on gain switching:
  - New analog part without TOT (dynamic gain switching)
  - Backend « à la HKROC »: auto-trigger, zero-suppress – EIC compatible

HGCROC



HKROC

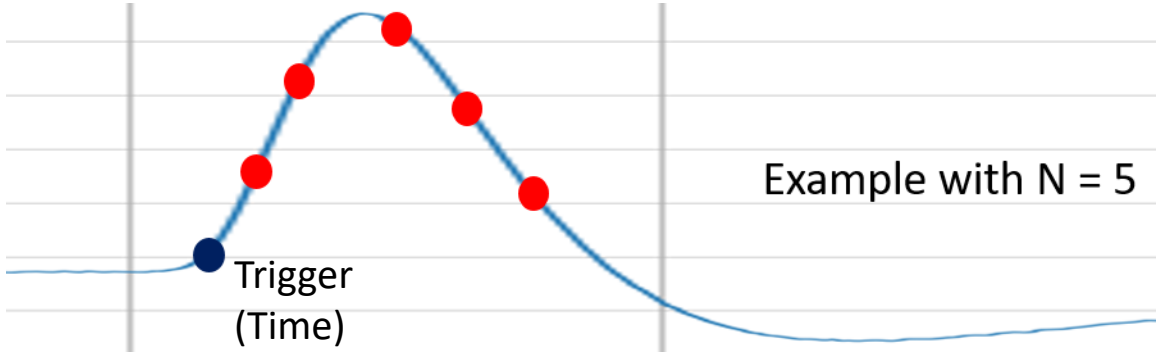
CALOROC 1A
CMS front end
EIC readout

CALOROC 1B
New front end
EIC readout

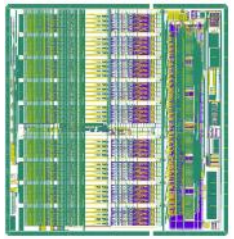
CALOROC1 received beginning of April 2026

CALOROC: Waveform Digitizer for SiPM Readout

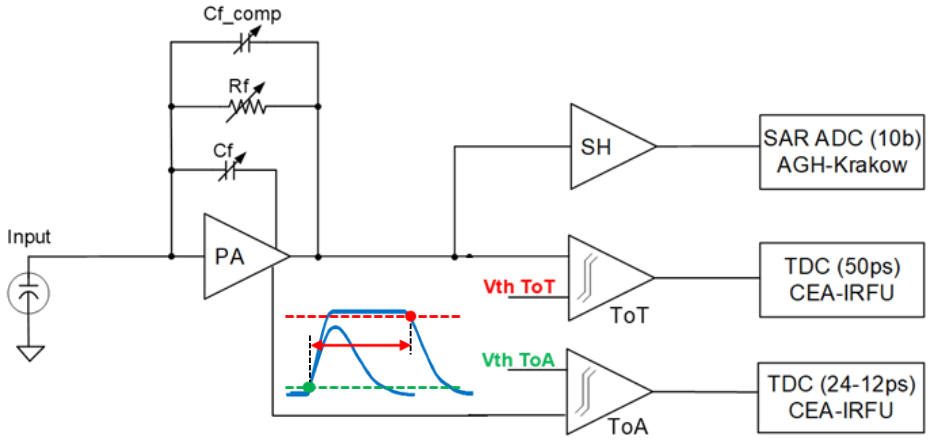
- CALOROC main changes:
  - Released in 2 versions: CALOROC-A and CALOROC-B
  - New 6-layer substrate – BGA (common)
  - New EIC digital processing (common)
  - New testboards (common)



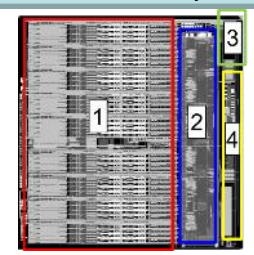
CALOROC 1A
CMS front-end
100-600pF SiPM capacitance



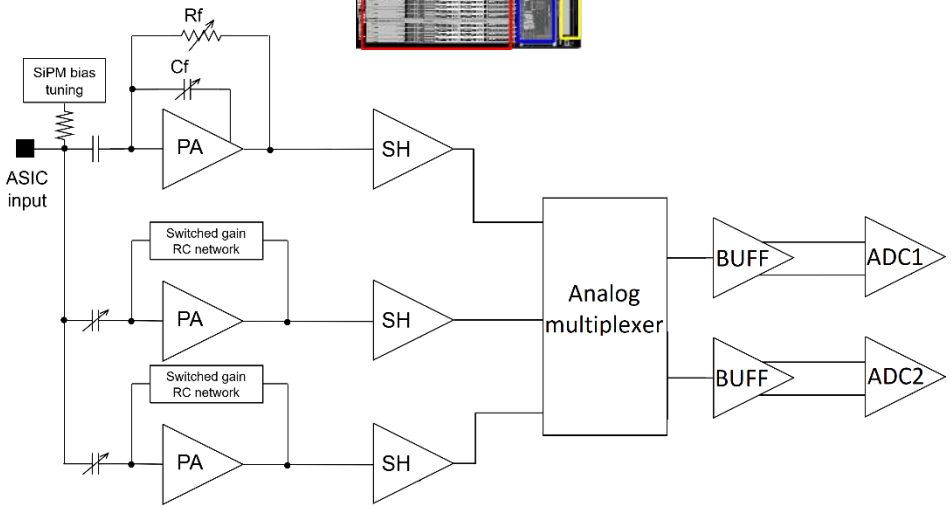
Measurements not started



CALOROC 1B
New switched-gain front-end
600p-10nF SiPM capacitance

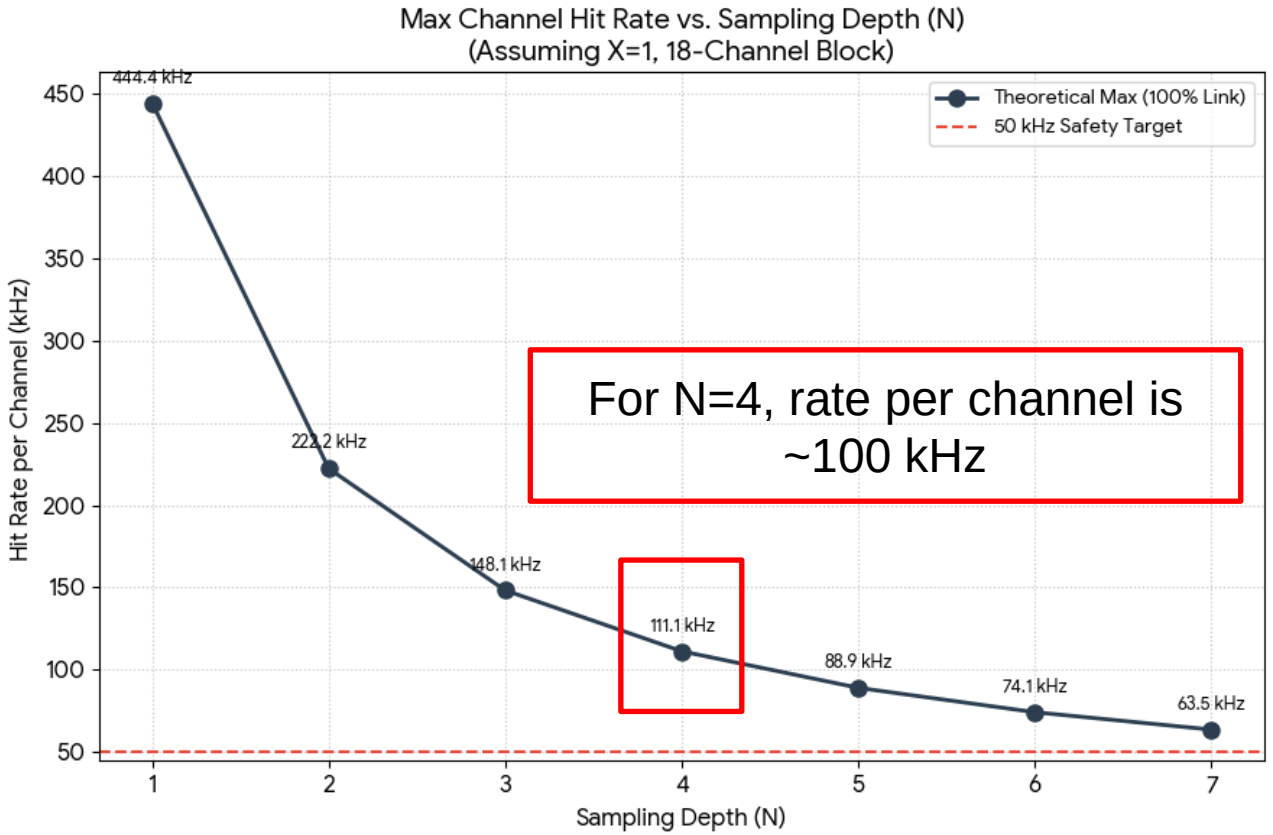


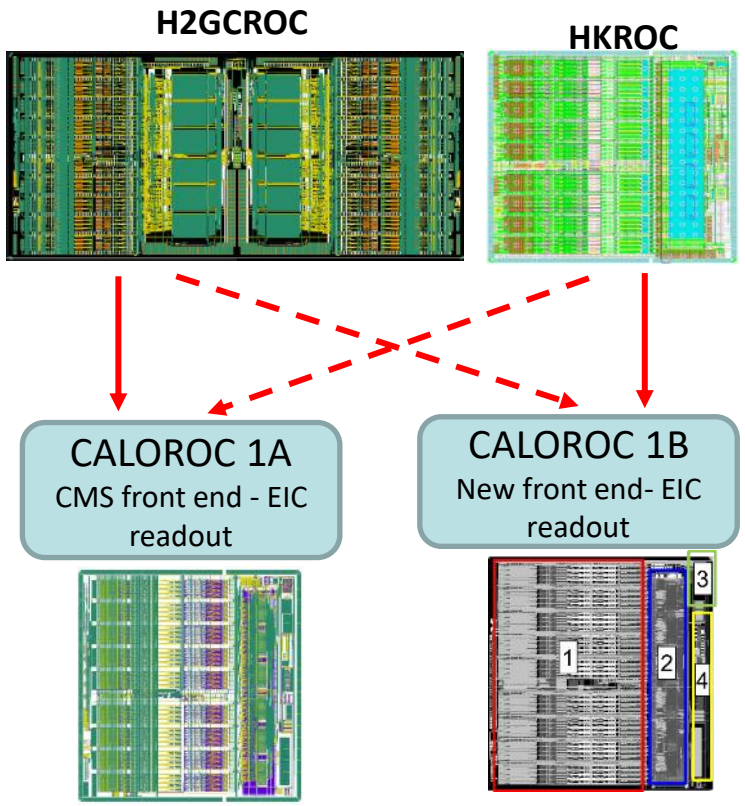
Measurements in progress



Follow-up of BNL CALOROC1 workfest (preliminary)

- Channel rate calculated with:
  - Uniform distribution
  - Worst case = always 1 channel readout over 18
    - Example with N=4 and
      - 2 separated in time hit ➔ 40 words read out
      - 2 in-time hits ➔ 24 words read out



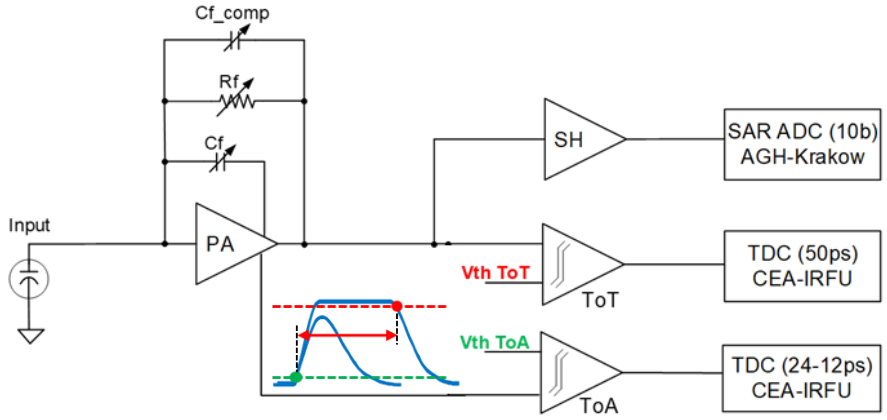


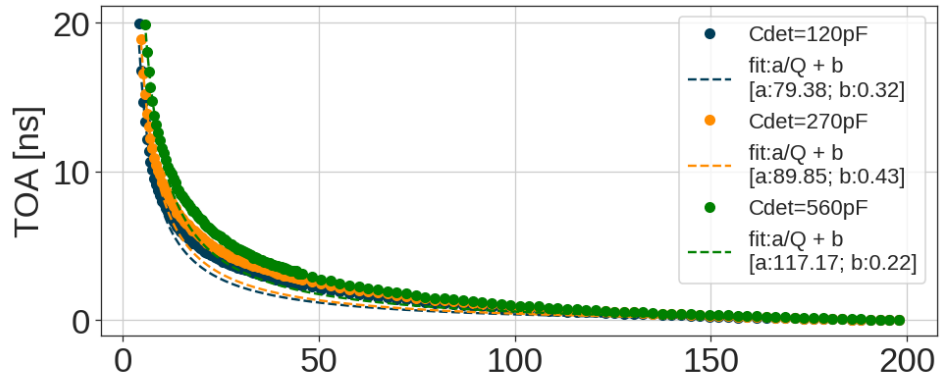
1. The Readout Model

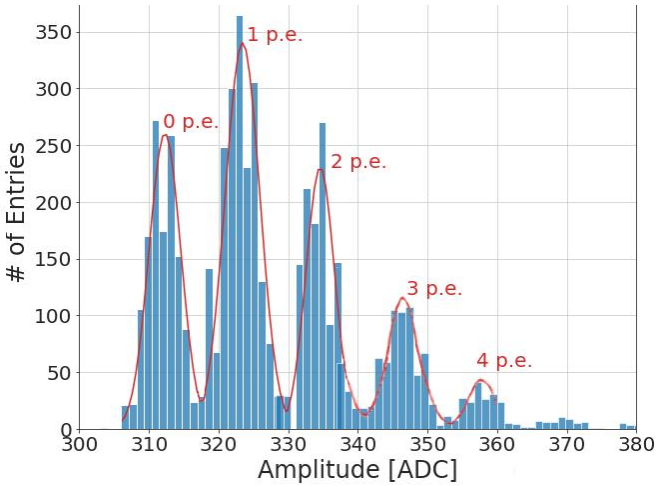
$$T_{readout} = N \times (X + 4) \times 25\ ns$$

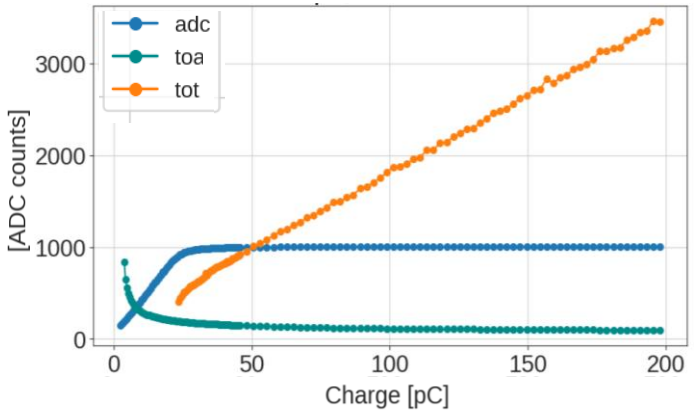
CALOROC1A (measurements of H2GCROC)

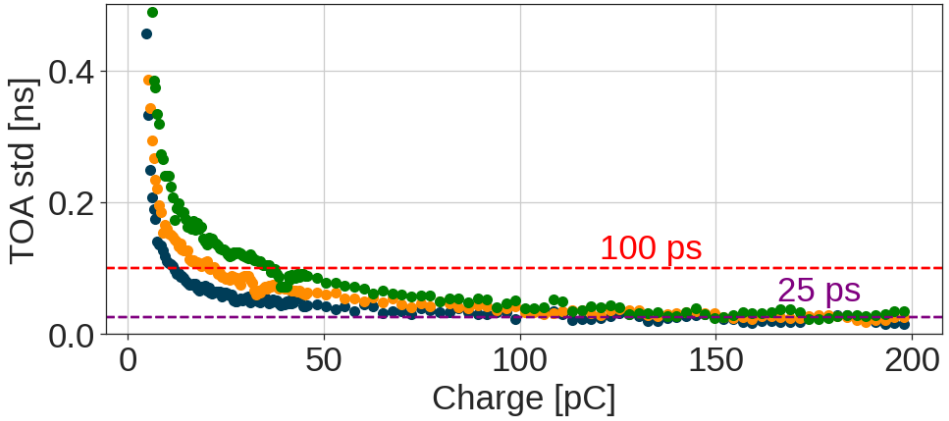
- Reuse of analog front-end based on ADC/TOT and TOA: fully characterized *
  - 15 mW per channel / Radiation performance / SiPM range 100-600 pF

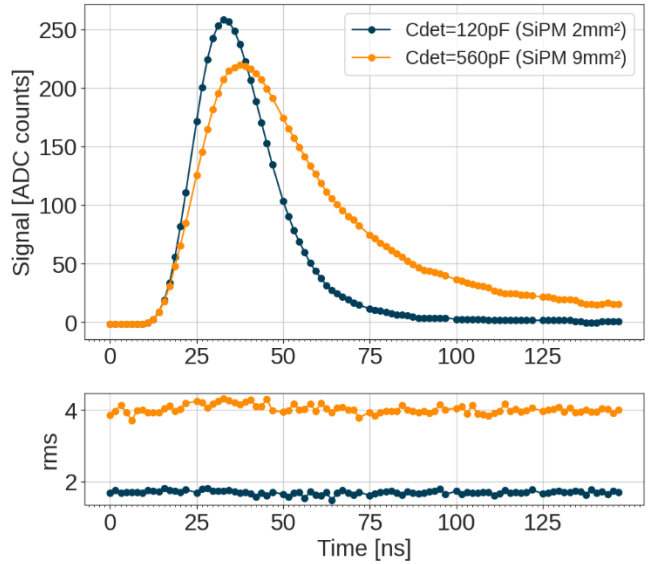










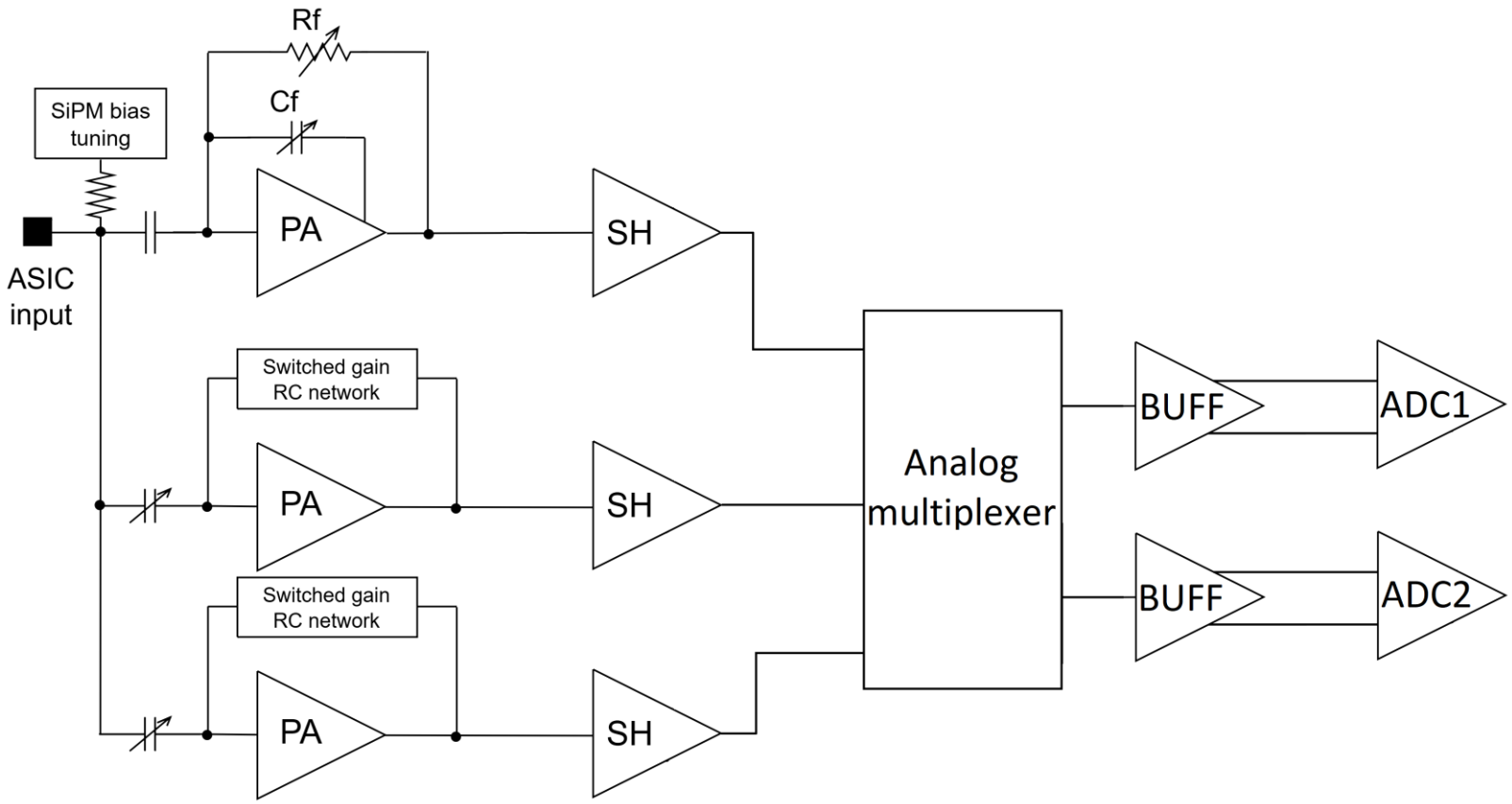


- CALOROC1A only update its back-end to be EIC compatible

* TWEPP 2023 ➔ https://doi.org/10.1088/1748-0221/19/04/C04005

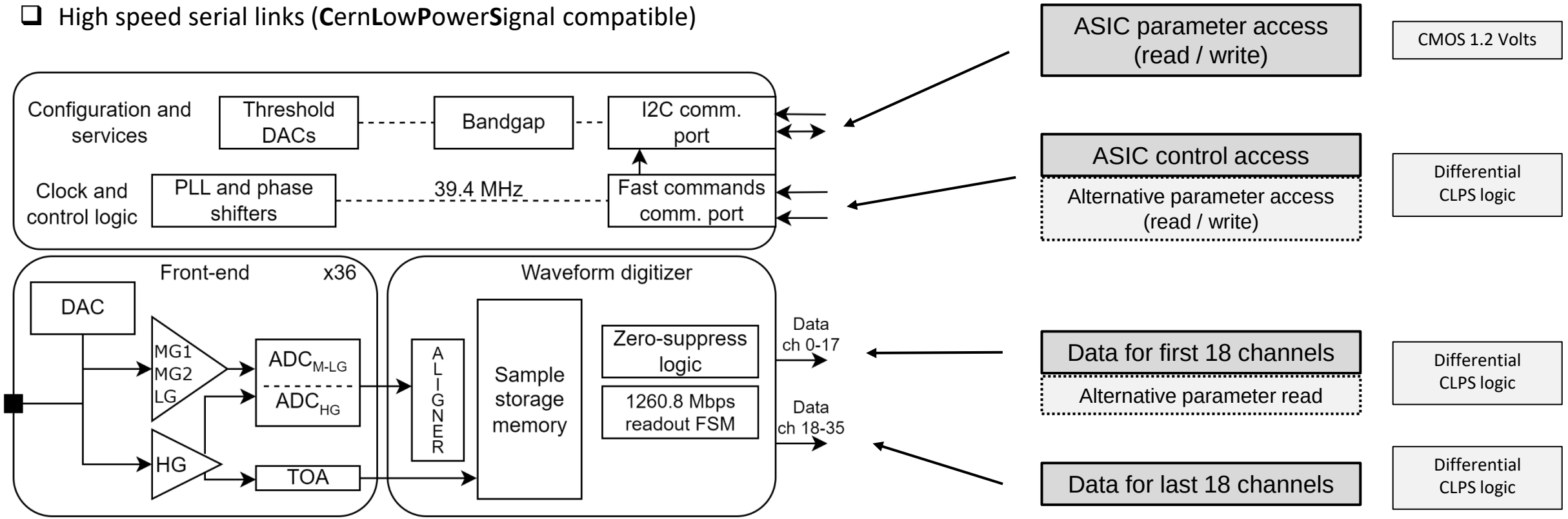
CALOROC1B: Channel Architecture

- New dynamic frontend with switched gain:
  - 1 high gain preamplifier
  - 2x low power preamplifier
  - 1 analog multiplexer
- Reuse CMS-H2GCROC ADCs and TDCs:
  - 10-bit 40 MHz ADC (Krakow)
  - 25 ps TDC (Saclay)
- Shared CALOROCs backend
- Common specifications:
  - SiPM from 560 pF to 2.24 – 8.96 nF
  - ~ 10-15 mW/channel
  - CMS HL-LHC Radiation level 200 Mrad



CALOROC-B: Block Diagram – Interfaces [F. Dulucq]

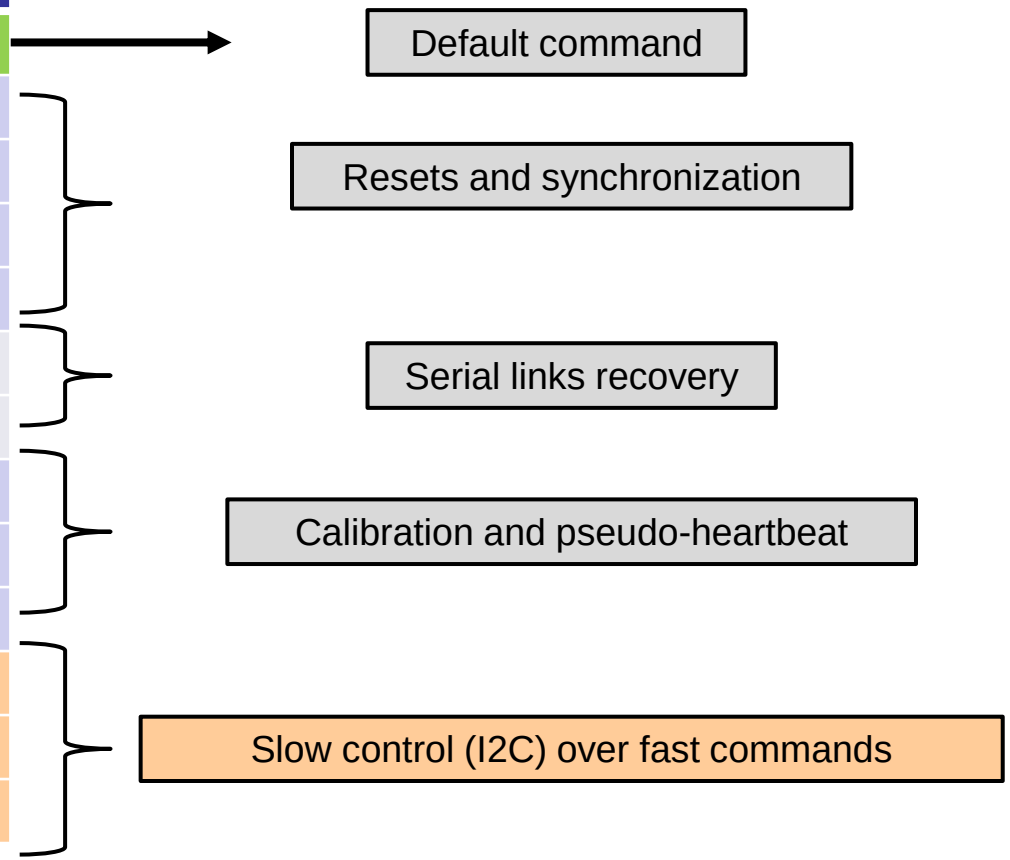
- CALOROCs will have the same interfaces (comparable to CMS ones):
  - 1 clock @ 315.2 MHz + 2 resets (hard + soft)
  - Fast command to dynamically control the ASIC (differential)
  - I2C to set the parameters
  - High speed serial links (**C**ern**L**ow**P**ower**S**ignal compatible)



CALOROC: Fast Commands

- Commands to interact dynamically with the ASIC
  - 8 bits commands synchronized with incoming 315.2 MHz clock – MSB first
  - Only idle needed – others have a known latency
  - Detailed in the datasheet

Fast commands	Value	Description
Idle	00110110	Default command inside
ChipSync	11010010	Reset FSM, buffers and counters
BCR	00011101	Reset timestamp counter to a default value
EBR	11010001	Empty readout buffers
PING	10011001	Ping status and counters
LinkResetROCD	10011010	Transmission of synchronization patterns
ROC-Serializer-Reset	10011100	Reset serializer link module only
L1A	01001011	External trigger (all channels)
CalPulseInt	00101101	800 ns internal calibration pulse
CalPulseExt	01111000	100 ns external calibration pulse
SC_0	01011010	I2C over fast command - send ‘0’
SC_1	01011100	I2C over fast command - send ‘1’
SC_Valid_Reset	10001011	Valid or reset (2 consecutives) current transaction



CALOROC: Readout Frames

- For charge measurements, CALOROC-A based on ADC/TOT, CALOROC-B only ADCs

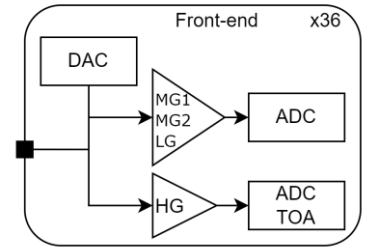
CALOROCA (CMS-like)

4b-data Header	2b Mode	Dh Ts	1 - 6b evt counter - 0 - 16b Timestamp	1
4b-hit Header	8b 0	Dh Hm	Dh Ch	18 channels Hit map
Tc	Tp	10b ADC-1	10b ADC or TOT (Tc = 1)	10b TOA
Tc	Tp	10b ADC-1	10b ADC or TOT	10b TOA
⋮				
Tc	Tp	10b ADC-1	10b ADC or TOT	10b TOA
CRC				
Idle/Sync Header	28b default IDLE Pattern			

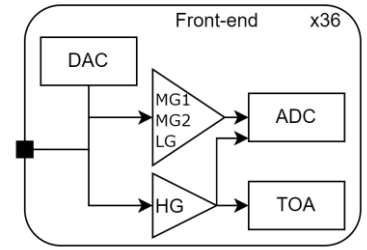
CALOROCB – 2 ADCs or 1 ADC (4 gains)

4b-data Header	2b Mode	Dh Ts	1 - 6b evt counter - 0 - 16b Timestamp	1
4b-hit Header	8b 0	Dh Hm	Dh Ch	18 channels Hit map
2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
⋮				
2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
CRC				
Idle/Sync Header	28b default IDLE Pattern			

CALOROCB (2 ADCs)

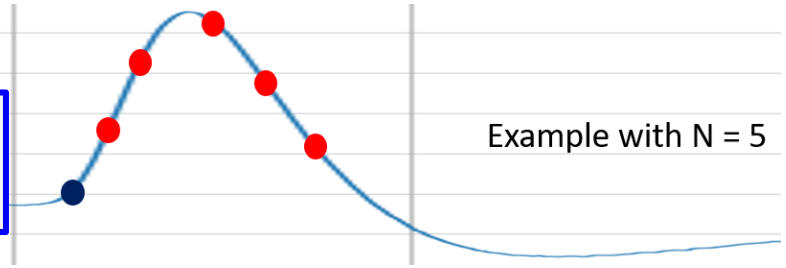


CALOROCB (1 ADCs)



In ZS mode, for **X** (1-18) hit channels and **N** samples, number of 32-bit words is:

N x (2Headers + **X** + 2Trailers)



Measurement Setup

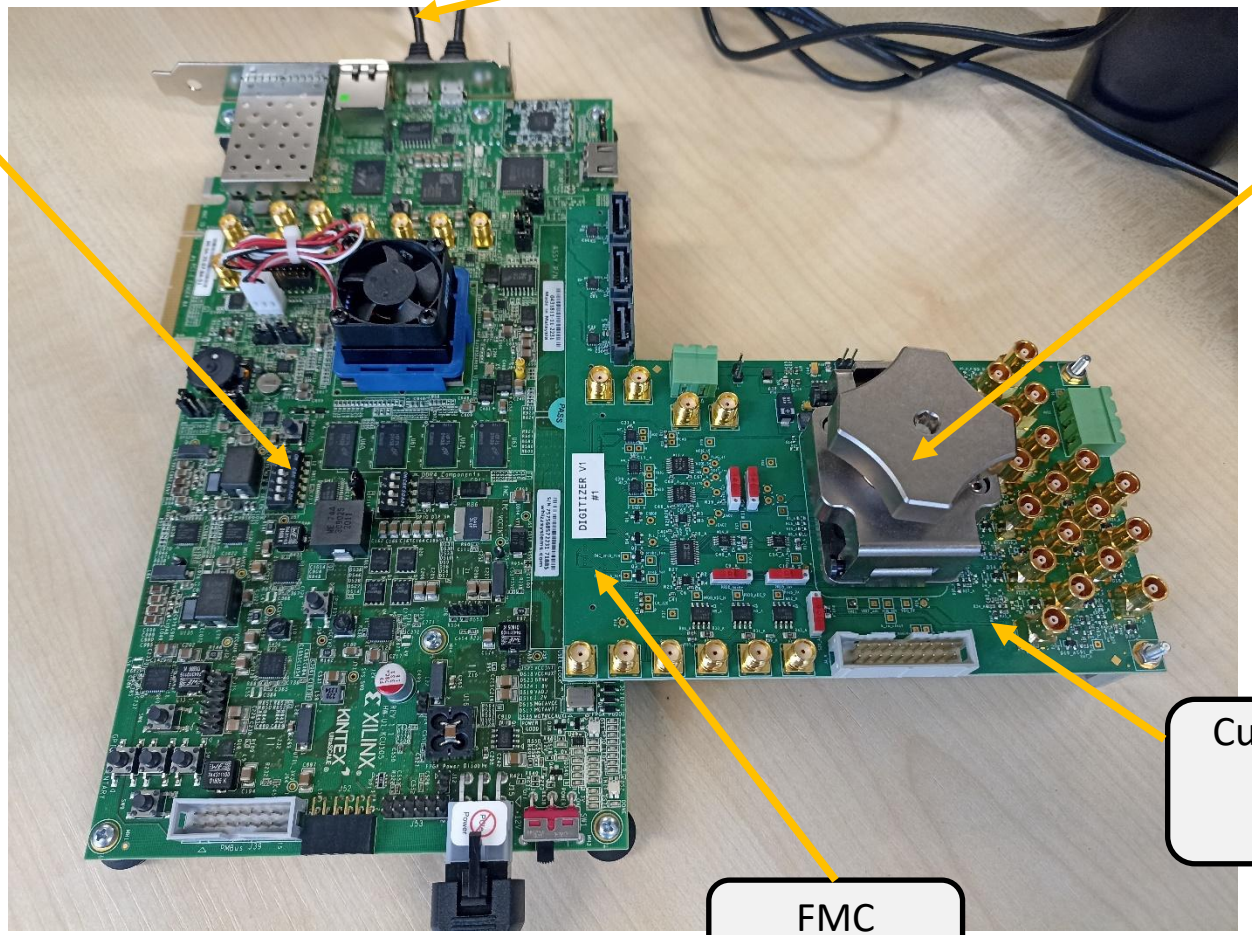
- Measurements done on HKROC modified motherboard:
  - Part of the channels accessible with detector capacitance of 2.2 nF
  - Measurements using internal injection DAC (20fC / DAC , maximum of 82pC)
  - Firmware + software (LLR – OMEGA)

Python scripts

Monitor
Program
Test

Commercial
KCU105 board

CALOROC
BGA socket



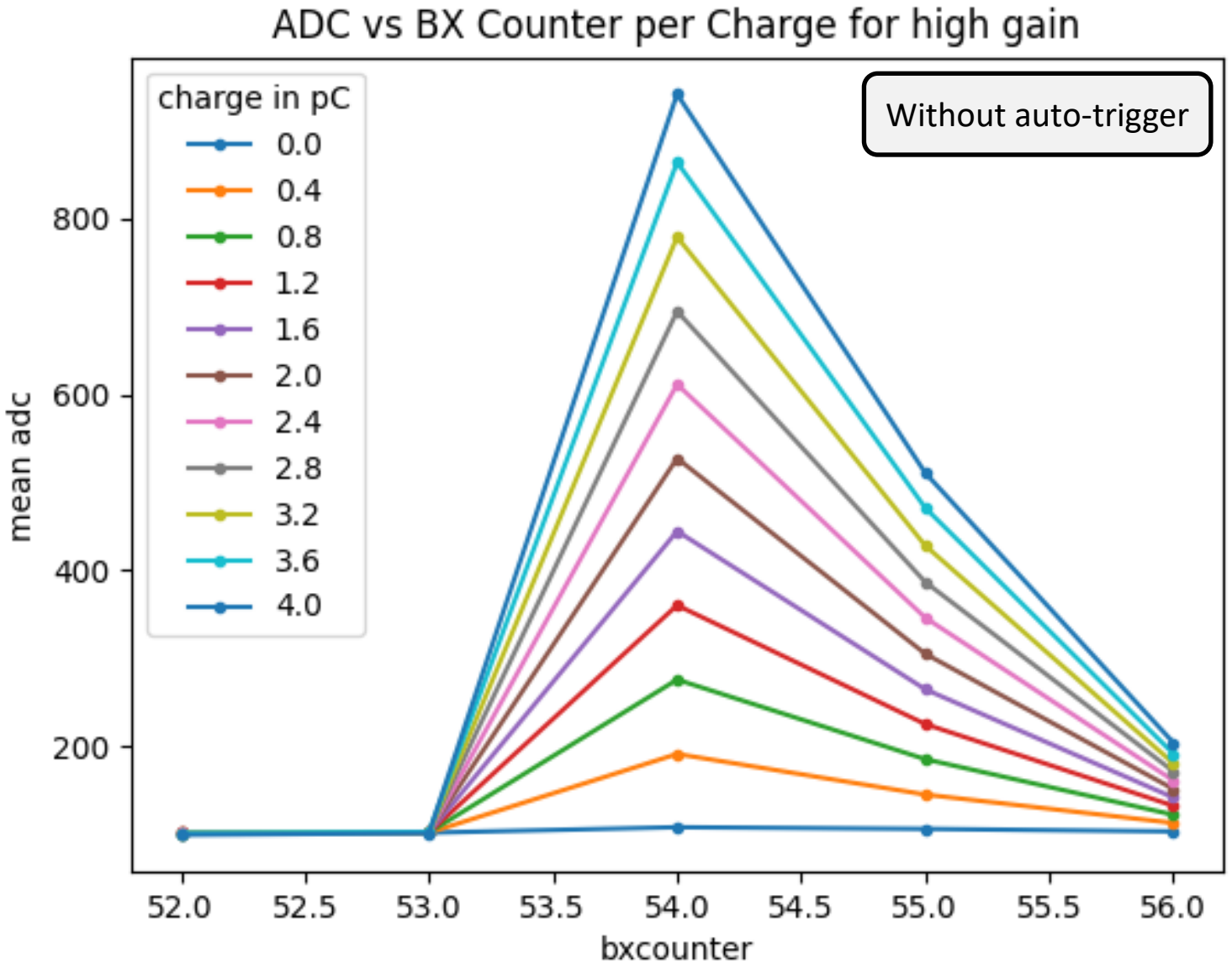
CALOROC
motherboard –
received last week

Custom HKROC for
CALOROC
motherboard

FMC
connector

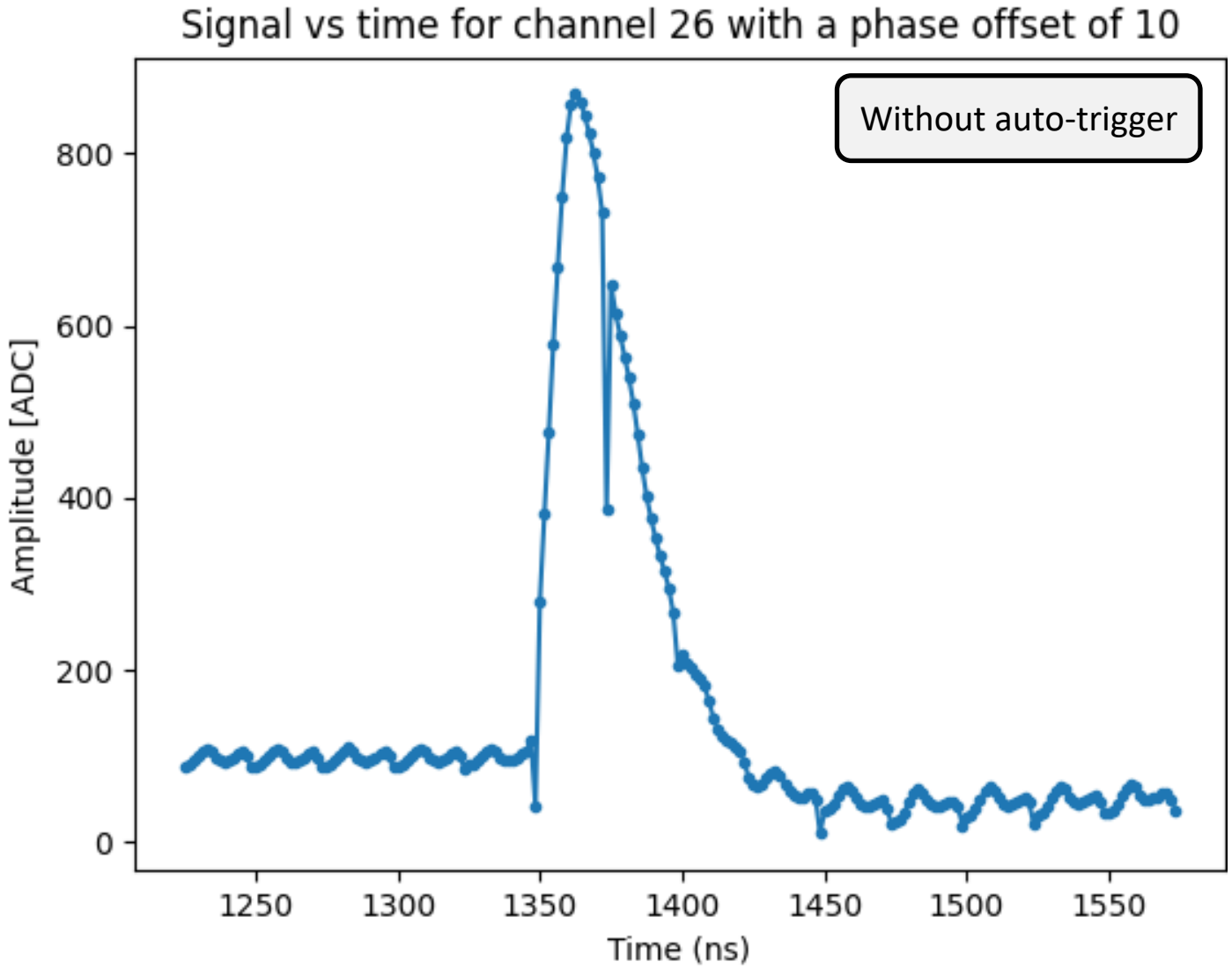
High Gain Waveform Measurements

- Using internal injection of the ASIC:
  - High-gain channel
  - Without auto-trigger (using fast commands)
  - to force autotrigger
- Using 5 samples (1 baseline + 4 signals)
- Working as expected but see next slides for detailed analysis (gain / noise / uniformity)



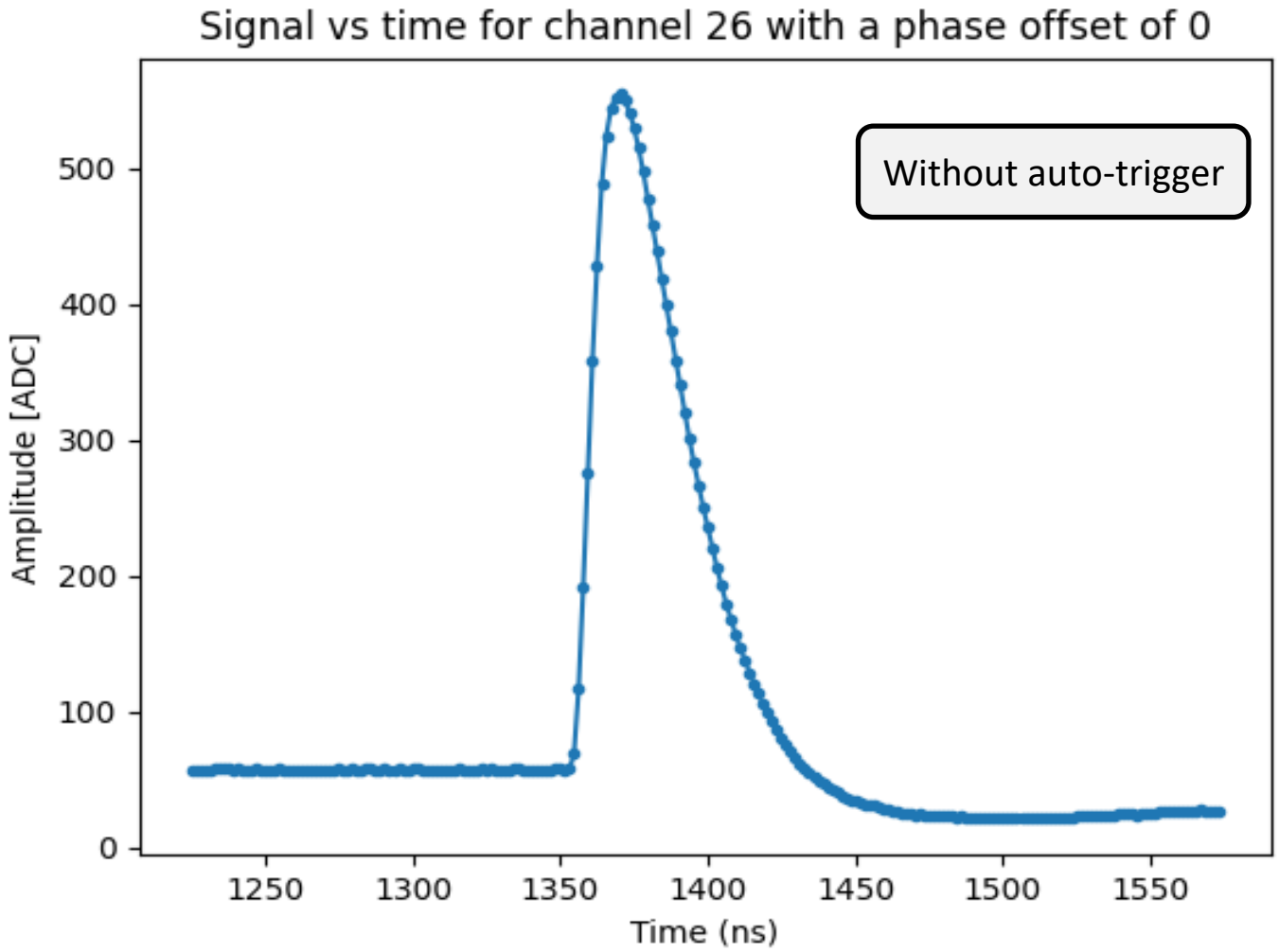
CALOROC-B Waveform Measurements

- Using internal injection of the ASIC:
  - Done by doing several runs and shifting the ADC **sampling**
  - Move to 1 sample every ~25 ns to 16 samples
  - Used only to reconstruct waveform like an oscilloscope
- Digital noise observed about 4.1 ADC counts
  - 2.2 counts expected in the simulations
- SNR for a 10 DAC injection (200fC) was 19 (using the pedestal noise) for channel
  - Expected buy see next slide
- Investigation in progress
  - New PCB needed + perhaps dedicated one



CALOROC-B Waveform Measurements

- Using internal injection of the ASIC:
  - Done by doing several runs and shifting the **injection**
  - Move to 1 sample every ~25 ns to 16 samples
- Injection synchronous to the sampling
  - Confirms the noise is due to digital coupling
- Investigation in progress
  - Noise correlated with preamp gain
  - Internal or PCB coupling ?



Main investigation for the coming months of measurements

Full chain ASIC response for each mode

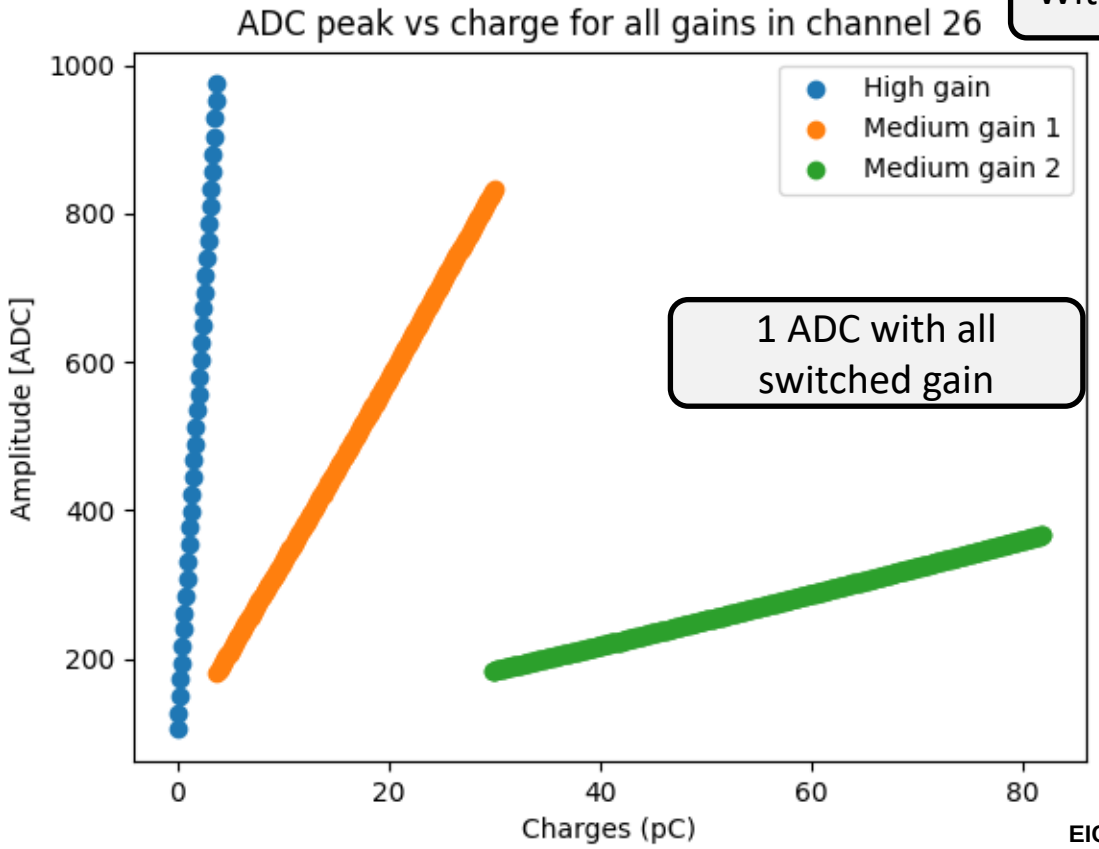
- Previous measurements done using the 1 ADC configuration with gain switching active

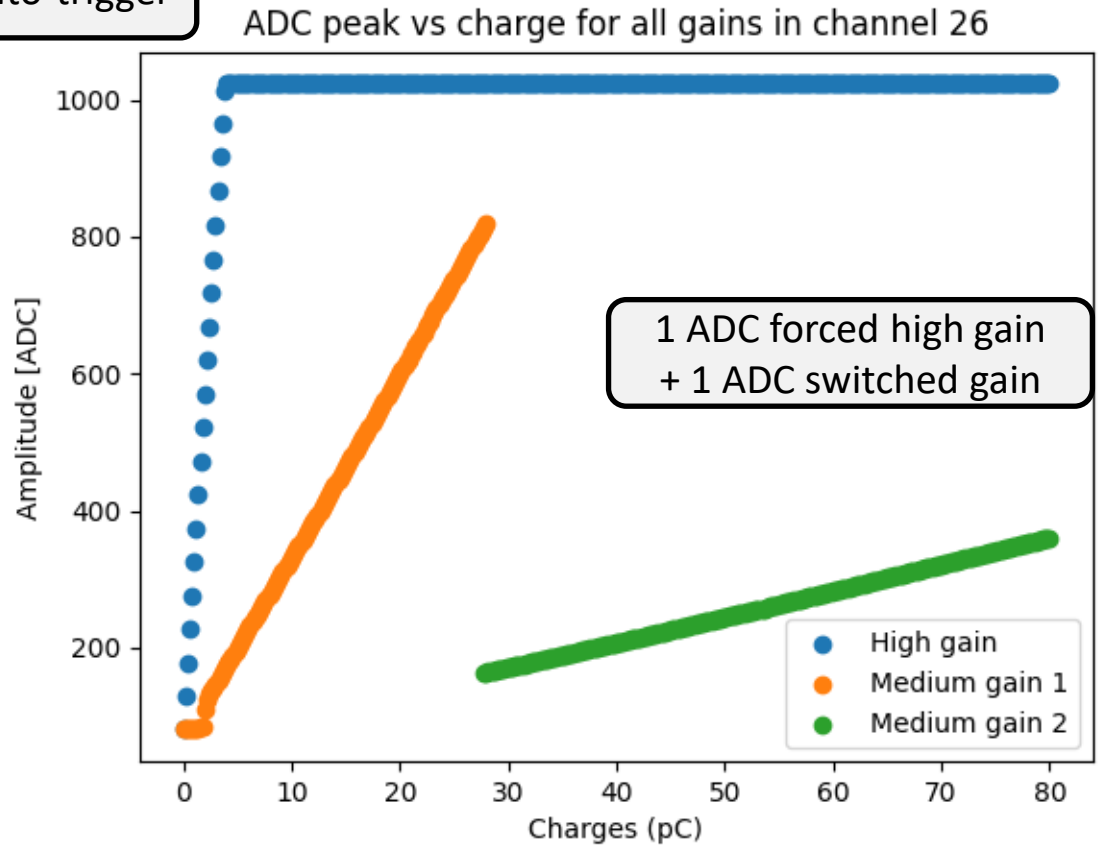
- 2 ADCs mode possibility (1 ADC forced to high-gain and second one linked to switched gain)

1 ADC mode

Without auto-trigger

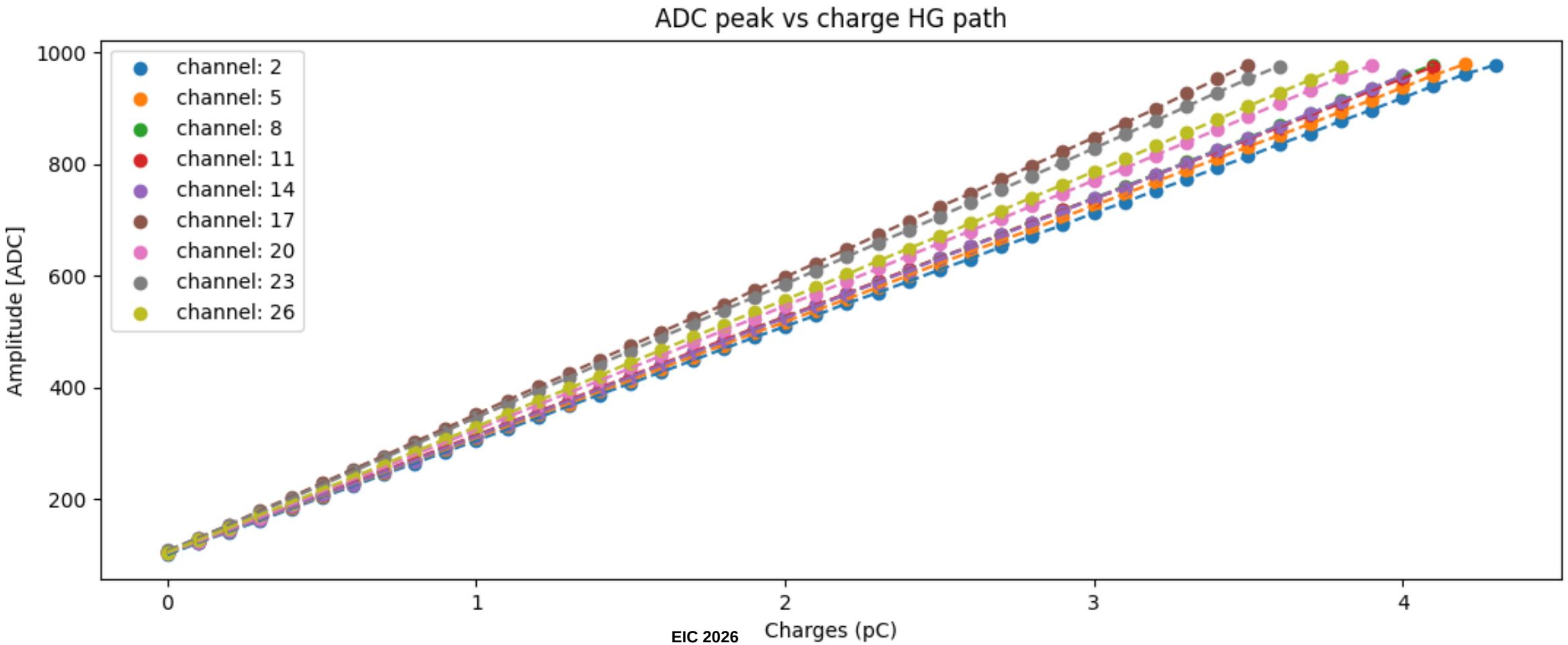
2 ADCs mode





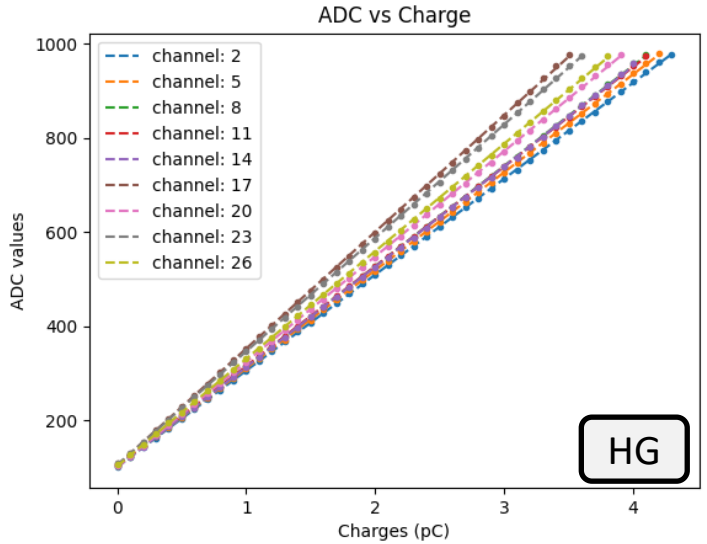
Gain uniformity over channels

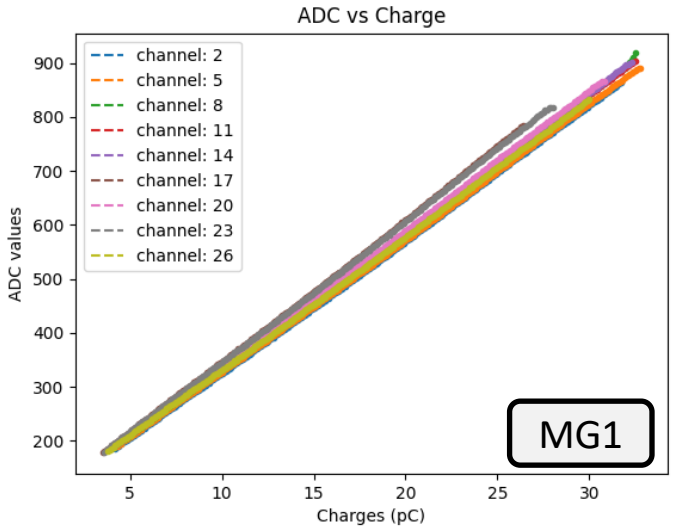
- Gain disparity observed with a maximum difference of 13% less gain
- Mainly due to the parasitic resistance between the injection DAC and channels
- External injection (new PCB) is needed to measured the effective gain uniformity

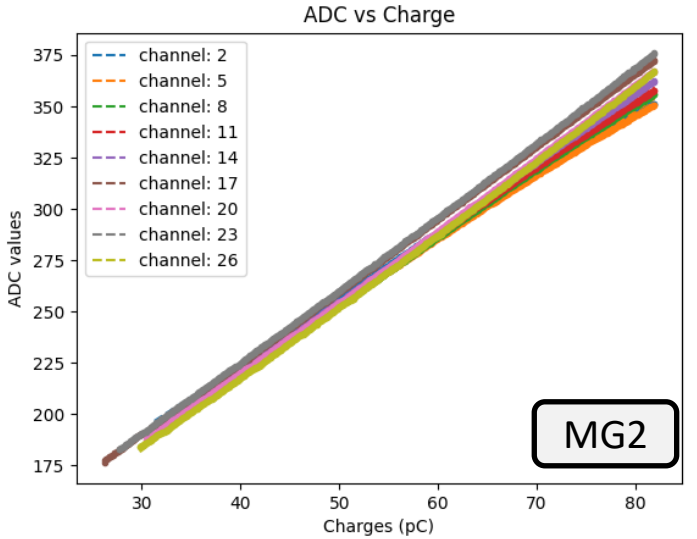


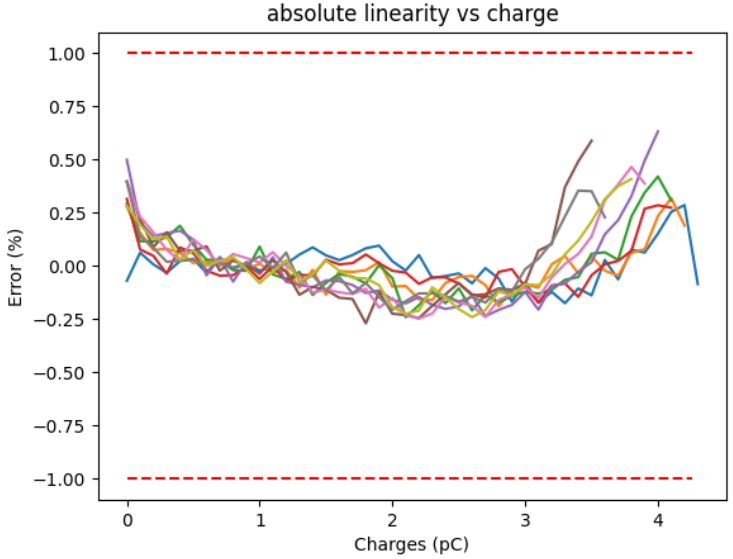
Gain Linearity

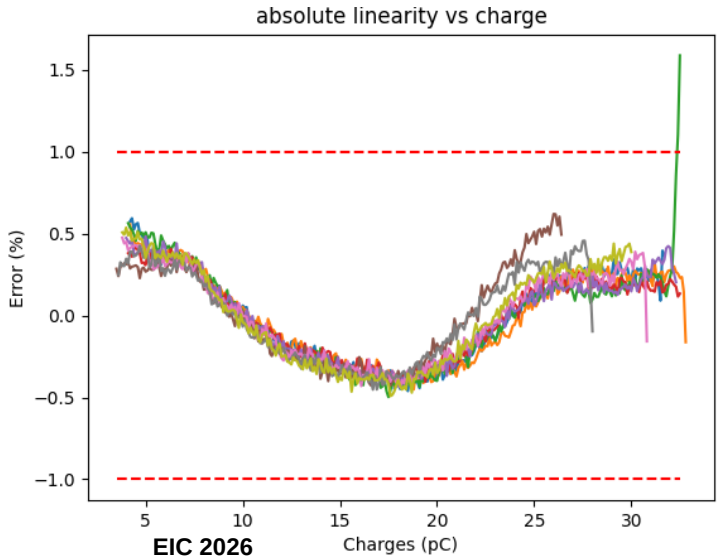
- Linearity measured at the peak of the signal
  - Using external trigger

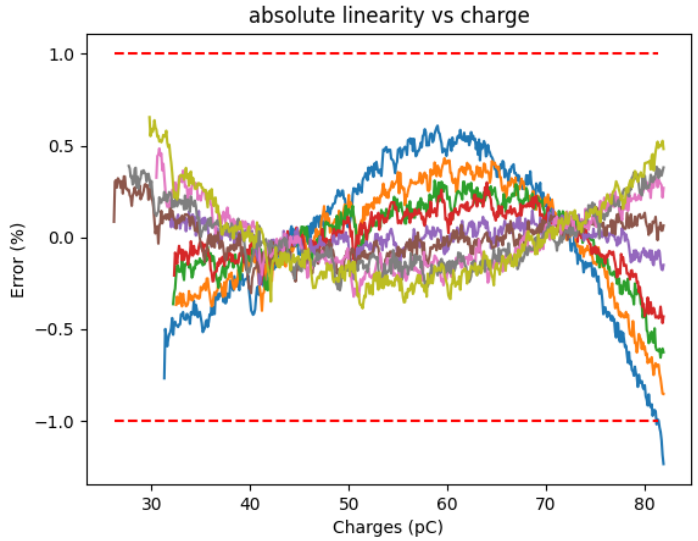












CALOROC integration and power supply consideration (Sept 2025)

- On the board, CALOROC will need a maximum of 3 power supplies:
  - Analog / Digital + 1 dedicated for CALOROC-A (Preamp)
  - (Not shown here: LED power and HV)

JEDEC MO-216 – 17 x 17 mm BGA version

Digital side

Analog side

MAPPING CALOROC_1 BGA 400 (TOP VIEW)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SDA	RSTB_I2C	HARD_RSTB	SOFT_RSTB	ERROR	CK_320_N	CK_320_P	FCMD_P	FCMD_N	ADD<4>	CHIP_R	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND
SCL	GND	GND	GND	GND	GND	VHI10<0>	VHI10<1>	FLAG_AF	ADD<4>	VREF_ADC	AGND	AVDD	AGND	IN<0>	AGND	IN<1>	AGND	NC	VDDA_PAD
DAC_ALDO	GND	GND	GND	GND	GND	NC	NC	FLAG_AF		VCM_ADC	AGND	AVDD	AGND	IN<2>	AGND	IN<3>	AGND	NC	VDDA_PAD
NC	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<4>	AGND	IN<5>	AGND	NC	VDDA_PAD
NC	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<6>	AGND	IN<7>	AGND	NC	VDDA_PAD
OUT_TSPFF	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<8>	AGND	IN<9>	AGND	AGND	AGND
SIPM_CALIB	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<10>	AGND	IN<11>	AGND	NC	VREF_SK_LP
NC	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<12>	AGND	IN<13>	AGND	AGND	AGND
STROBE_EXT	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<14>	AGND	IN<15>	AGND	NC	VREF_NOINV_SK
EFUSE	NC	GND	DVDD	VDD_PLL	VDD_PLL	AGND_PLL	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<16>	AGND	IN<17>	AGND	NC	VREFINV_VBM3PA
TRIG_P	NC	GND	DVDD	VDD_SC	VDD_SC	AGND_PLL	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<18>	AGND	IN<19>	AGND	NC	VREFTOA_VBIPA
TRIG_N	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<20>	AGND	IN<21>	AGND	NC	VREFTOT_VBMPA
DAQ2_P	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<22>	AGND	IN<23>	AGND	NC	VBG_1V
DAQ2_N	PLL_LOCK	GND	DVDD	VDD_SC	VDD_SC	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<24>	AGND	IN<25>	AGND	NC	PROBEPA_VBOPA
DAQ3_P	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<26>	AGND	IN<27>	AGND	NC	INCTEST
DAQ3_N	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<28>	AGND	IN<29>	AGND	NC	VDDA_PAD
ADD<3>	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<30>	AGND	IN<31>	AGND	NC	VDDA_PAD
ADD<2>	GND	GND	GND	GND	GND	NC	NC	NC		VCM_ADC	AGND	AVDD	AGND	IN<32>	AGND	IN<33>	AGND	NC	VDDA_PAD
ADD<1>	GND	GND	GND	GND	GND	NC	VHI10<2>	NC	NC	VREF_ADC	AGND	AVDD	AGND	IN<34>	AGND	IN<35>	AGND	NC	VDDA_PAD
ADD<0>	PROBE_TOT_PA	PROBE_TOA	PROBE_DC2	PROBE_DC1	PROBE_INV	VNEG	VHI10<3>	PROBE_NOINV	TRIG_EXT	TRIG1_EXT	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND

GROUND BGA	ALIM BGA
AGND	AVDD
AGND	AVDD
AGND	AVDD
AGND	AVDD_PAD
AGND	AVDD_PAD
GND_PLL	VDD_PLL
GND	DVDD
GND	DVDD
GND	DVDD
GND	DVDD
GND	DVDD
	VDD_SC

Analog side

Digital side

CALO-A (Preamp)

Board power	Nominal value	ASIC power	Max ratings
Analog power	1.2 Volts	AVDD, VDD_PLL	8 mW / chn
Preamp power	2.5 or 1.2 Volts (CALO-A or CALO-B)	AVDD_PAD	2 mW / chn
Digital power	1.2 Volts	DVDD	3 mW / chn

April 2026 update:

- Measurement of 12 mW / channel
- Without auto-trigger and zero suppress

First Measurements Plan (BNL January Meeting)

- ASIC sanity checks
  - Power consumption of each part
  - Bias value versus simulation

CALOROC-A	CALOROC-B
50% done	80% done

- Validating interfaces (could be done in parallel)
  - Accessing the parameters (I2C only)
  - Reading ASIC output (high speed serial links)

CALOROC-A	CALOROC-B
50% done	80% done

At this stage, more in-depth characterization tests could be performed

- ASIC front-end characterization
  - Linearity / Noise
  - Analog to digital conversion
  - Timing measurements
  - CALO-A: Reproduce H2GCROC performances
  - CALO-B: Validation of switch-gain mechanism

CALOROC-A	CALOROC-B
Not started	Started

Results will drive CALOROC2 design ➔ Q1 2027
Focus on noise / timing measurements

Quality Assurance / Quality checks

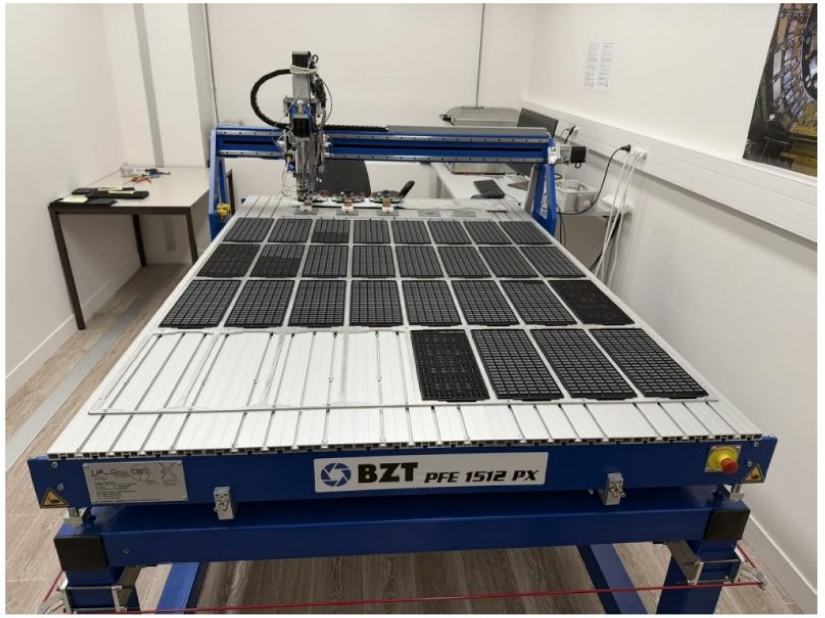
- Expertise in radiation-hardened front-end ASICs for HEP
  - HL-LHC ASICs: ATLAS HGTD and CMS HGCAL (10^5 ASICs)
- Expertise in irradiation testing (dose and displacement)
  - HL-LHC levels 200 Mrad and 10^{16} n_{eq} / cm^2 (1 MeV equivalent neutrons)
- Standard interfaces ensures a full compatibility with our robot
  - 2x 50 ASICs tested per hour (H2GCROC) with QR code scan

Feedback from H2GCROC in 2026:

- 70% yield after testing (10k ASICs)
- 250 chips / day / robot
- Robots available in 2027

- Database management, robot setup and mechanical structure done by LLR

LLR robot: processing of LD (Si and SiPM)



OMEGA robot: processing of HD (Si)

Documentation

- Detailed datasheet for CALOROC1-B
  - Available in version 1.3 (**only distributed to first users**)
  - Includes interfaces – Parameters – EIC fast commands
  - HL-LHC ASICs: ATLAS HGTD and CMS HGCAL (10^5 ASICs)

AGH Irfu OMEGA Microelectronics

Documents history

VERSION	DATE	MODIFICATION
1.0	5 Sept, 2025	First release
1.1	3 Oct, 2025	Update with LLR comments + BGA/C4 mapping
1.2	12 Mar, 2026	Update operating modes, fast commands, I2C, CRC, 1 ADC mode
1.3	14 Apr, 2026	SC parameters update

- Available ASIC pinout (also part of the datasheet)
  - Common to all CALOROCs

MAPPING CALOROC_1 BGA 400 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	SDA	RSTB_I2C	HARD_RSTB	SOFT_RSTB	ERROR	CK_320_N	CK_320_P	FCMD_P	FCMD_N	ADD<4>	CHIP_R	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND
B	SCL	GND	GND	GND	GND	GND	VHI10<0>	VHI10<1>	FLAG_AF	ADD<4>	VREF_ADC	AGND	AVDD	AGND	IN<0>	AGND	IN<1>	AGND	NC	VDDA_PAD
C	DACaldo_daq0p	GND	GND	GND	GND	GND	NC	NC	FLAG_AF	NC	VCM_ADC	AGND	AVDD	AGND	IN<2>	AGND	IN<3>	AGND	NC	VDDA_PAD
D	NC_daq0n	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<4>	AGND	IN<5>	AGND	NC	VDDA_PAD
E	NC_daq1p	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<6>	AGND	IN<7>	AGND	NC	VDDA_PAD
F	OUTff_daq1n	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<8>	AGND	IN<9>	AGND	AGND	AGND
G	SIPM_CALIB	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<10>	AGND	IN<11>	AGND	NC	VREF_5K_LP
H	NC	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<12>	AGND	IN<13>	AGND	AGND	AGND
J	STROBE_EXT	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<14>	AGND	IN<15>	AGND	NC	VREF_NOINV_5K
K	EFUSE	NC	GND	DVDD	VDD_PLL	VDD_PLL	AGND_PLL	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<16>	AGND	IN<17>	AGND	NC	VREFINV_VBM3PA
L	TRIG_P	NC	GND	DVDD	VDD_SC	VDD_SC	AGND_PLL	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<18>	AGND	IN<19>	AGND	NC	VREFTOA_VBIPA
M	TRIG_N	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<20>	AGND	IN<21>	AGND	NC	VREFTOT_VBMPA
N	DAQ2_P	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<22>	AGND	IN<23>	AGND	NC	VBG_1V
P	DAQ2_N	PLL_LOCK	GND	DVDD	VDD_SC	VDD_SC	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<24>	AGND	IN<25>	AGND	NC	PROBEPA_VBOPA
R	DAQ3_P	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<26>	AGND	IN<27>	AGND	NC	INCTEST
T	DAQ3_N	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<28>	AGND	IN<29>	AGND	NC	VDDA_PAD
U	ADD<3>	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<30>	AGND	IN<31>	AGND	NC	VDDA_PAD
V	ADD<2>	GND	GND	GND	GND	GND	NC	NC	NC	NC	VCM_ADC	AGND	AVDD	AGND	IN<32>	AGND	IN<33>	AGND	NC	VDDA_PAD
W	ADD<1>	GND	GND	GND	GND	GND	NC	VHI10<2>	NC	NC	VREF_ADC	AGND	AVDD	AGND	IN<34>	AGND	IN<35>	AGND	NC	VDDA_PAD
Y	ADD<0>	PROBE_TOT_PA	PROBE_TOA	PROBE_DC2	PROBE_DC1	PROBE_INV	VNEG	VHI10<3>	PROBE_NOINV	TRIG2_EXT	TRIG1_EXT	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND

- Preliminary CALOROC "Tests and Acceptance Criteria"
  - Derived from H2GCROC robot serial tests

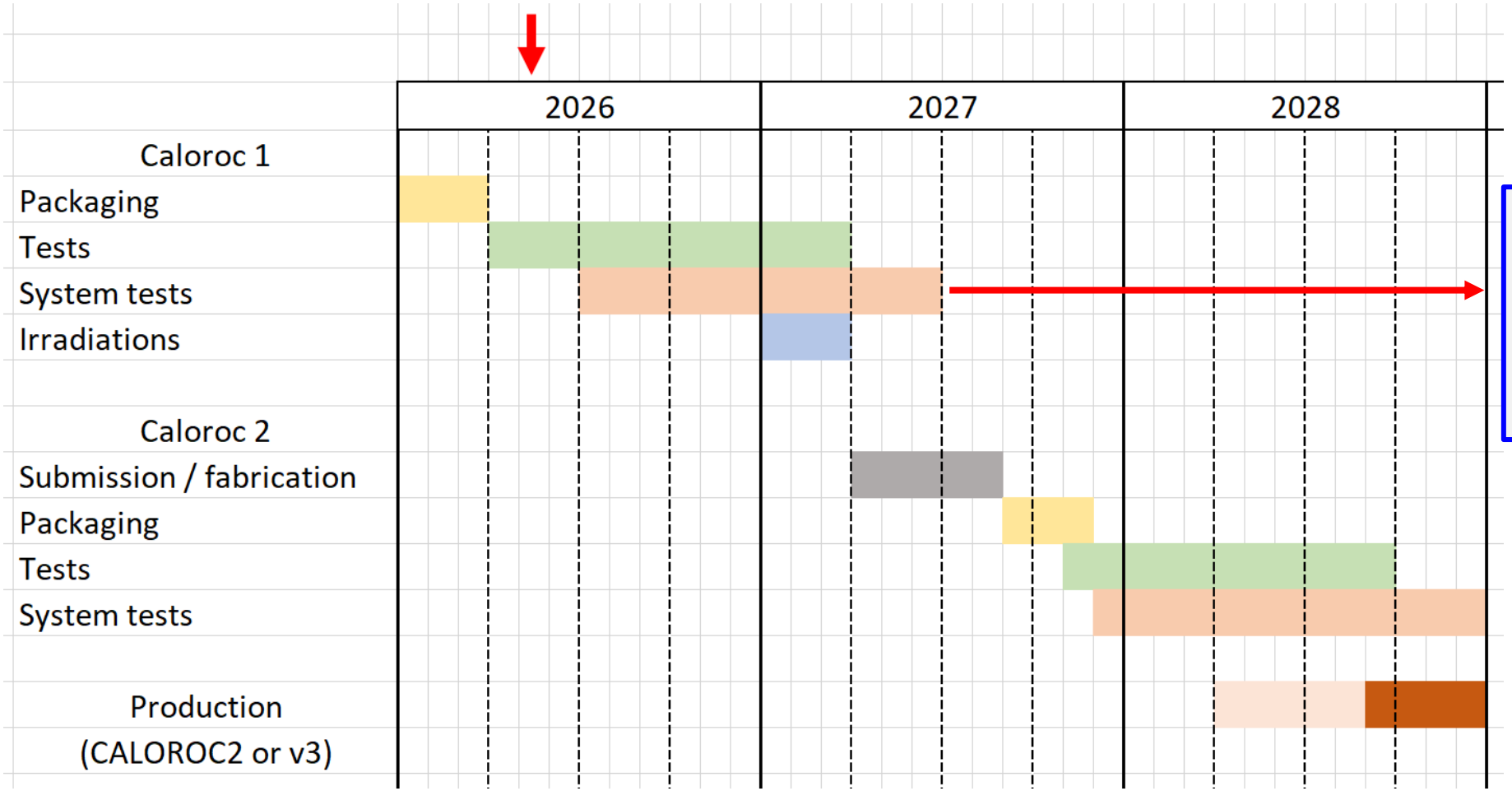
LLR OMEGA Microelectronics

CALOROC Quality Control: Tests and Acceptance Criteria

Abstract: This document is based on the work carried out by the LLR and OMEGA groups on quality checks for the HGCROC and H2GCROC ASICs. Two robots were set up to automate the various tests, depending on whether the chosen package is High Density (HD) or Low Density (LD). Since CALOROC is largely derived from H2GCROC, a significant part of the quality checks will be equivalent and are described in this document.

Timeline / System tests

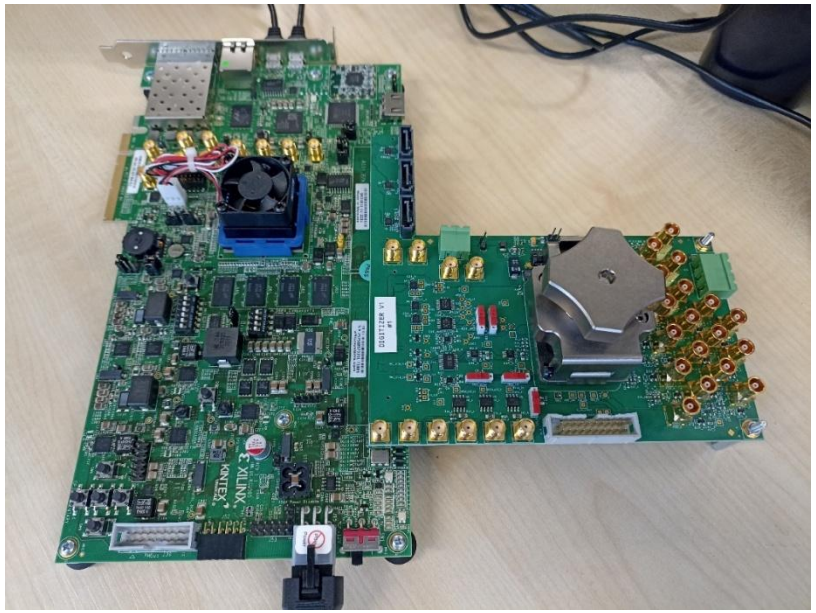
- CALOROC timeline – 2026 to 2028
  - First fabrication completed in Dec 2025 (Eng. Run)
    - Only 28 ASICs per variant of CALOROC1
  - Second fabrication foreseen in March 2027

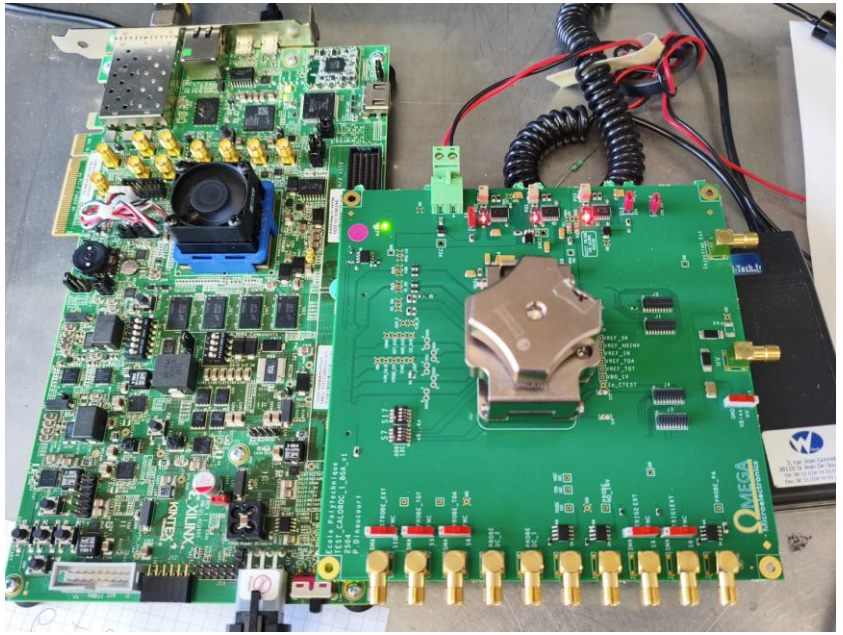


CALOROCs provided (May 26):
- 12 ASICs for LLR FEB (A+B)
- 2 ASICs for ORNL (A)
- 3 for testboards (B)

Summary and next steps

- CALOROCs received in April 26
  - Small quantities (28 x 2). Remaining one (100x2) in 4 months
- CALOROC-A analog measurements delayed
- CALOROC-B first measurements are encouraging and will focus on:
  - Noise investigation
  - Timing measurements
  - Crosschecks on our 2 different testboards
- Possible actions for investigation
  - “Noise analysis” testboard (3 months to fabricate)
  - New substrate (4 months to fabricate)
  - FEB crosschecks
- CALOROC2 in March 27
  - If noise understood + timing measurements OK





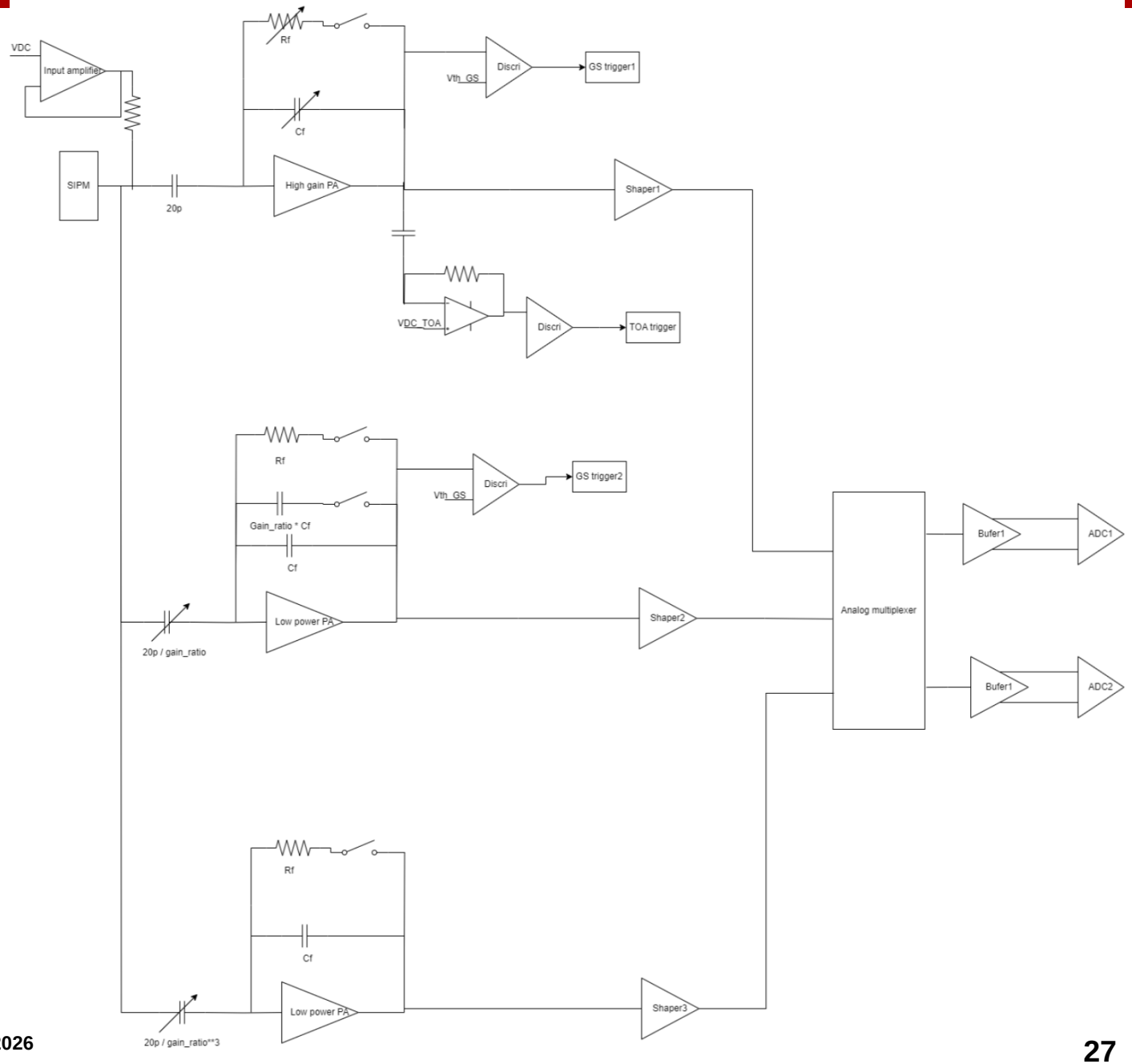
Backups

CALOROC1B: Detailed Channel Architecture

- Switched gain mechanism based on:
  - 1 High-gain preamp also connected to timing path (top)
  - 2 sitched-gain preamp (middle)
  - 1 low-gain preamp (bottom)

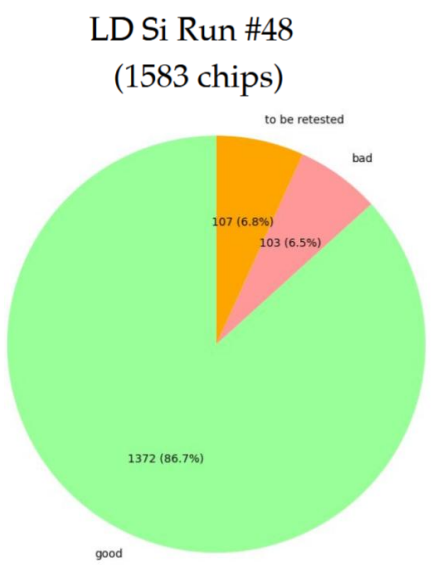
- Switching is based on 2 discriminators:
  - Latched outputs gives the overall gain active
    - 00 high gain
    - 01 medium gain 1 (before switching)
    - 10 medium gain 2 (after switching)
    - 11 low gain

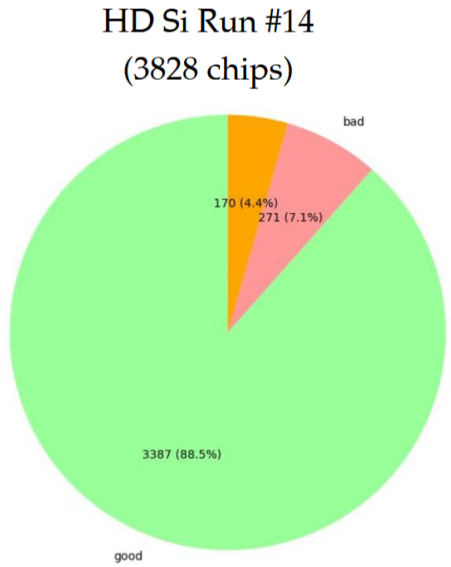
- Automatic reset is done after 75-100 ns after first comparator fired

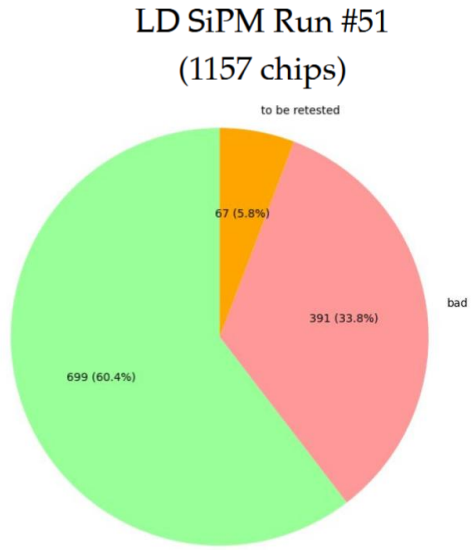


H2GCROC Robot Testing

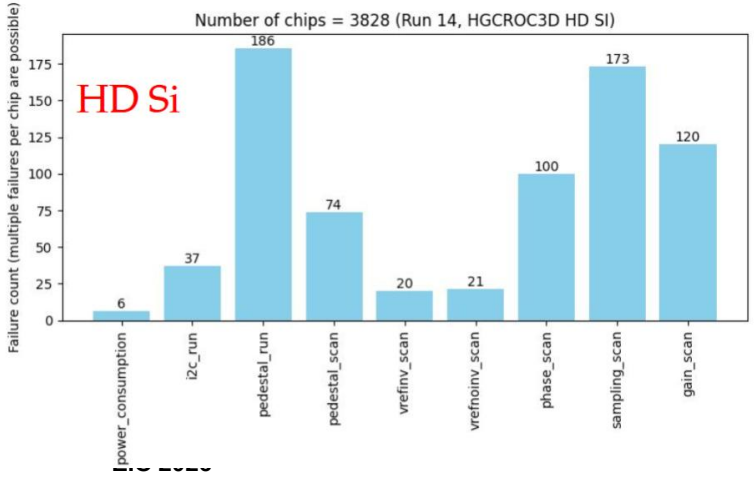
- Statistical analysis (LLR):
  - HGCROC yield > 85%
  - H2GCROC yield > 60%
    - Expected value for CALOROC-A

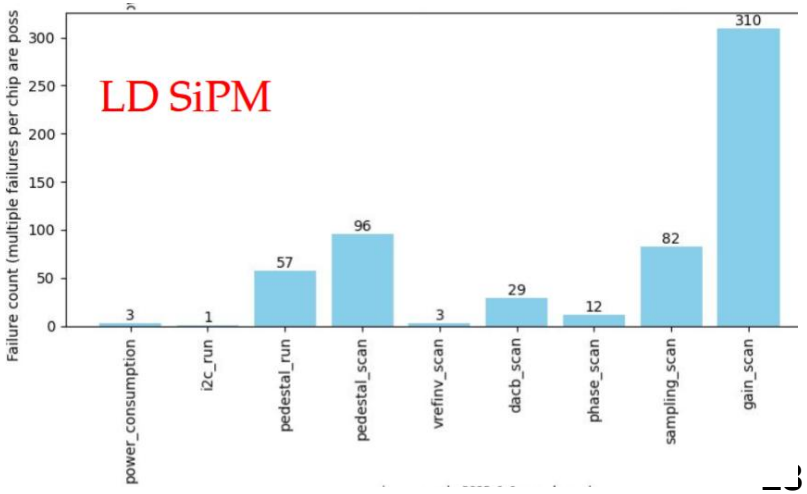






- Nature of failing tests (LLR):
  - Pedestal run (check ADC pedestal and noise)
  - Sampling scan (check ADC and TDC shapes)
  - Gain scan (check dynamic range / linearity)
  - SiPM fails mostly due to the gain scan
    - threshold tuning ?

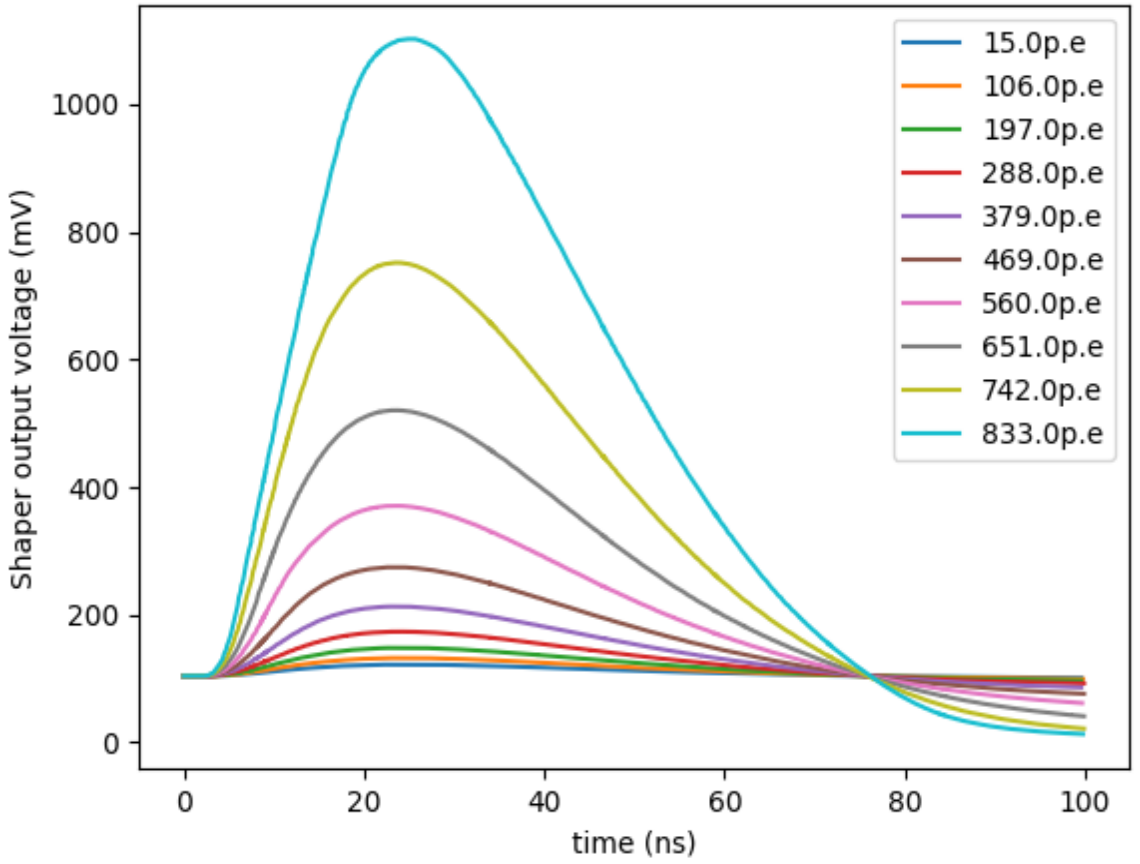




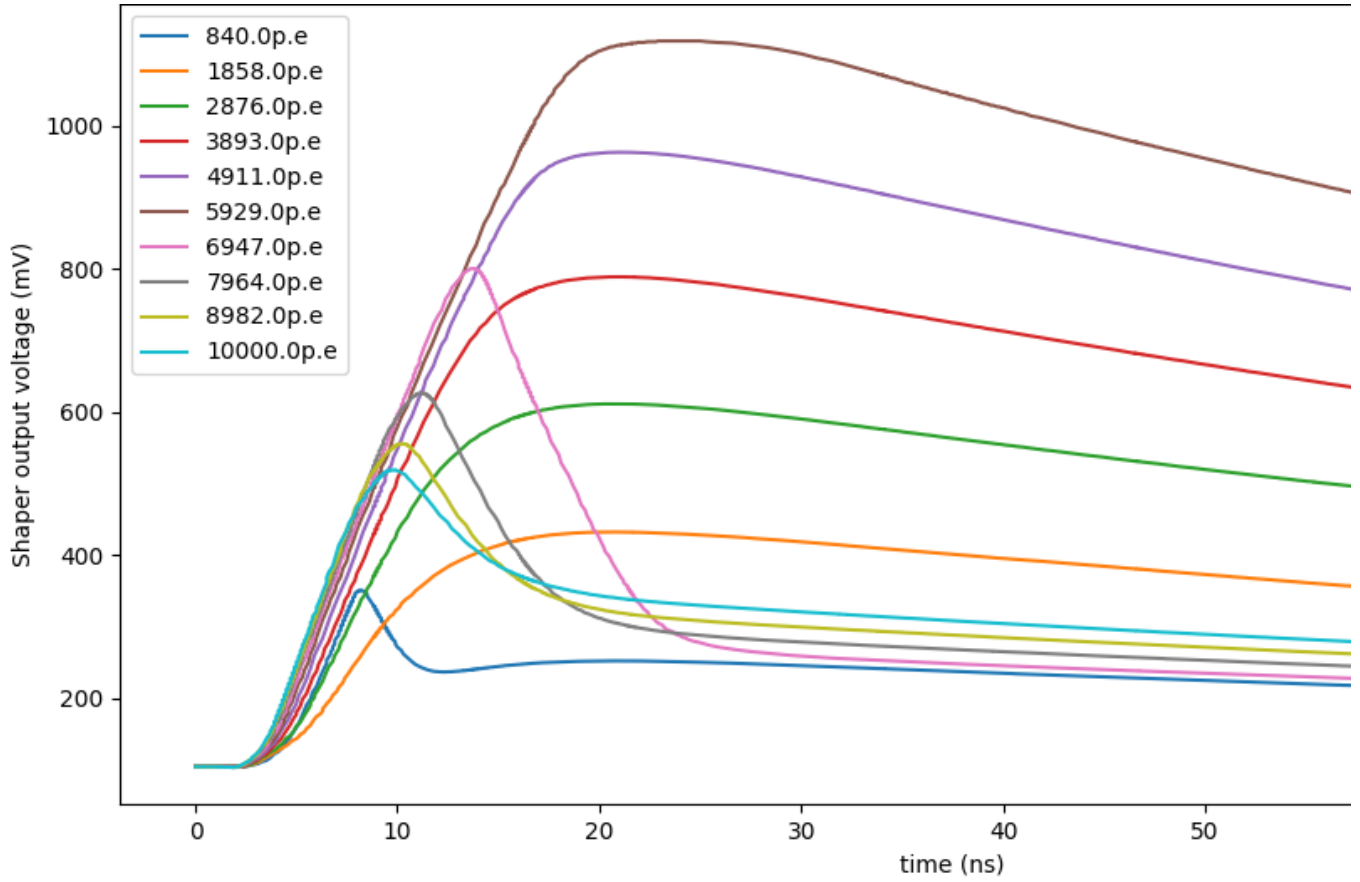
CALOROC1B: Charge and time simulations

- Waveform for HG on the left + gain switching on the right:
  - Example with Cd of 8.96 nF

Waveform for high gain shaper @8.96nf configuration



Waveform for medium gain shaper @8.96nf configuration



CALOROC1B: SiPM vs SNR

- The SiPM configuration has a direct impact on the SNR
  - SNR for 1p.e is proportional to Q/C (larger SiPM cap decrease SNR)
  - Gain of 1.8e5 electrons per p.e (table below)

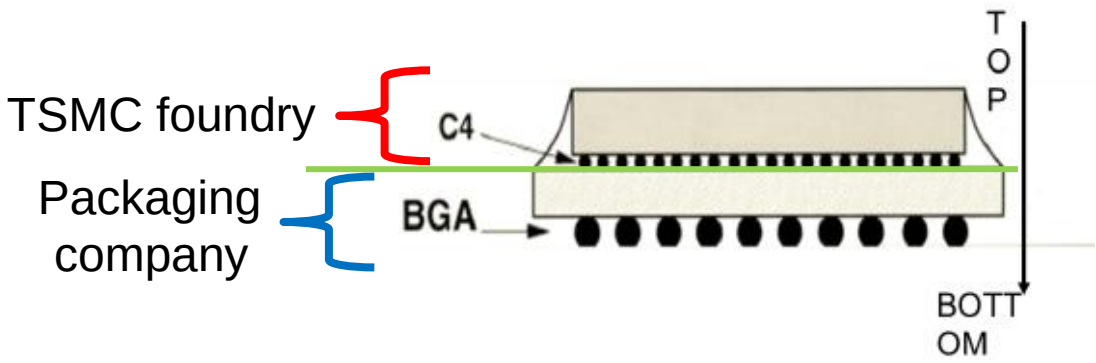
- CALOROC1b will be able to readout SiPM in the range ~ 560 pF to 8.96 nF
  - Timing measurements will focus on the MIP (~15pe)

Operation modes	1 SiPM of 560pF Caloroc1B	4 SiPMs of 560pF Caloroc1B	16 SiPMs of 560pF Caloroc1B	1 SiPM of 560pF Caloroc1A
Cin	560pF	2.24nF	8.96nF	560pF
Dynamic range in charge (Noise - Max)	3.2fC-190pC	11fC-790pC	45fC-3.17nC	20fC-320pC
Input time constant (occupancy related)	112ns	450ns	450ns	10ns
Jitter @ MIP (≈400fC)	42ps	130ps	520ps	400ps
SNR @ 1p.e (≈30fC@gain=1.8e5)	9	2.6	0.64	1.44

SiPM: S14160-3010PS 3x3mm (560pF)

CALOROC Packaging

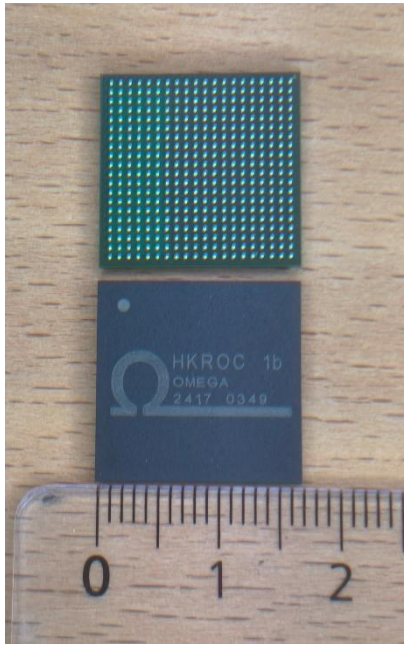
- CALOROC will have the same package as the existing HKROC:
  - JEDEC MO-216 – 17 x 17 mm BGA version
  - 400 balls with 0.8 mm pitch
  - Specific substrate (interposer) designed at OMEGA
  - **QR code** like HGCROC3



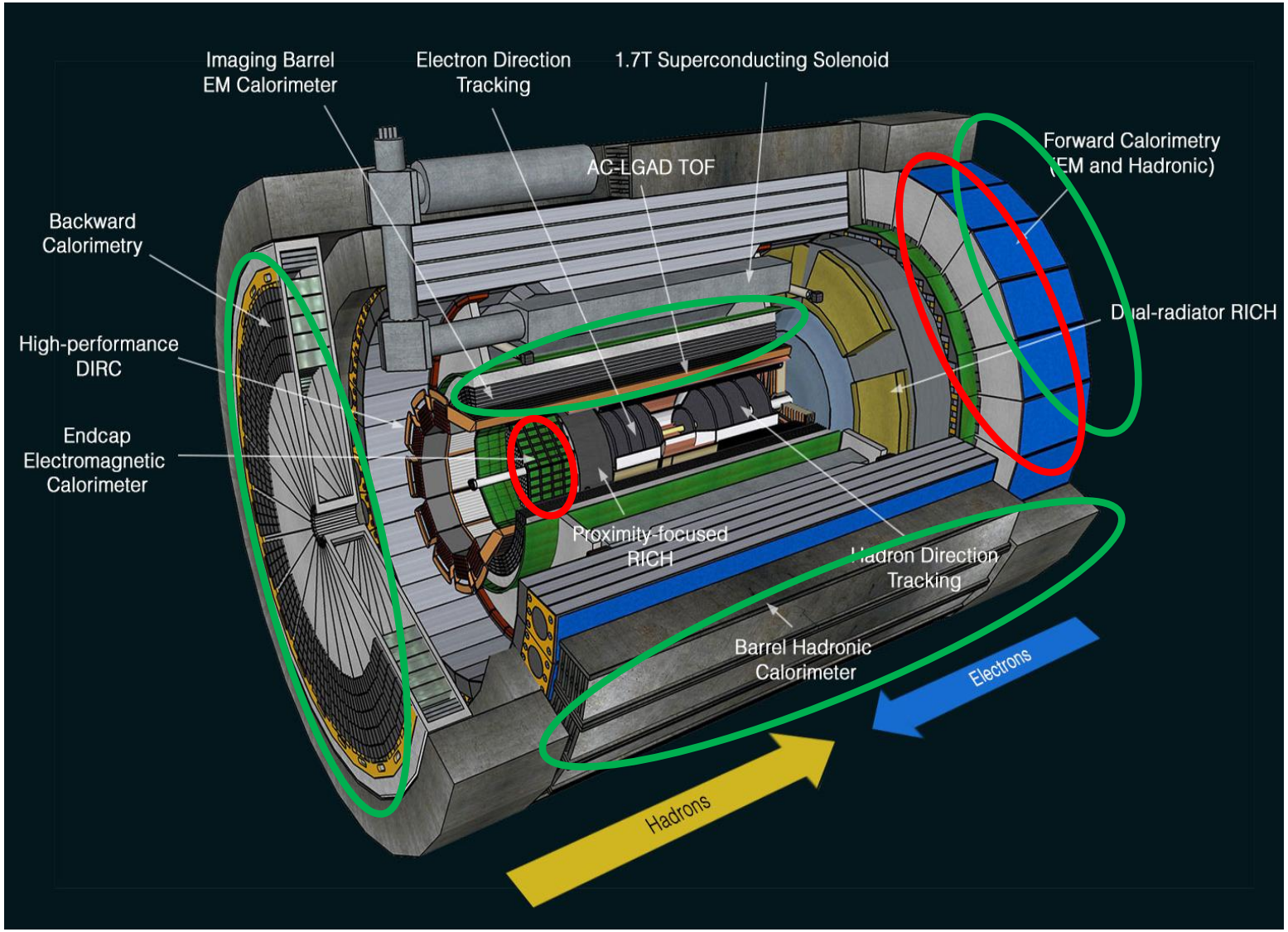
JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: THIN PROFILE, SQUARE AND RECTANGULAR, BALL GRID ARRAY FAMILY, 1.00 & 0.80 mm PITCHES	ISSUE: E	DATE: AUG 2003	MO-216

TABLE 3: SQUARE VARIATIONS – 0.80 PITCH

D / E	e = 0.80							
	MD/ME	N	SD/SE	VARIATION	MD-1/ME-1	N	SD/SE	VARIATION
14.00	17	289	0.00	BAJ-1	16	256	0.40	BAJ-2
15.00	18	324	0.40	BAK-1	17	289	0.00	BAK-2
16.00	19	361	0.00	BAL-1	18	324	0.40	BAL-2
17.00	20	400	0.40	BAM-1	19	361	0.00	BAM-2



Calorimetry at ePIC



13 Calorimeters:

- 7 x SiPM – CALOROC
- 5 x SiPM – Discrete
- 1 x SiPM – Commercial fADC250

From J. Landgraf
(IDR review)