OAK RIDGE National Laboratory

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H2GCROC readout update

PRESENTED BY

Norbert, Miklos, Gabor

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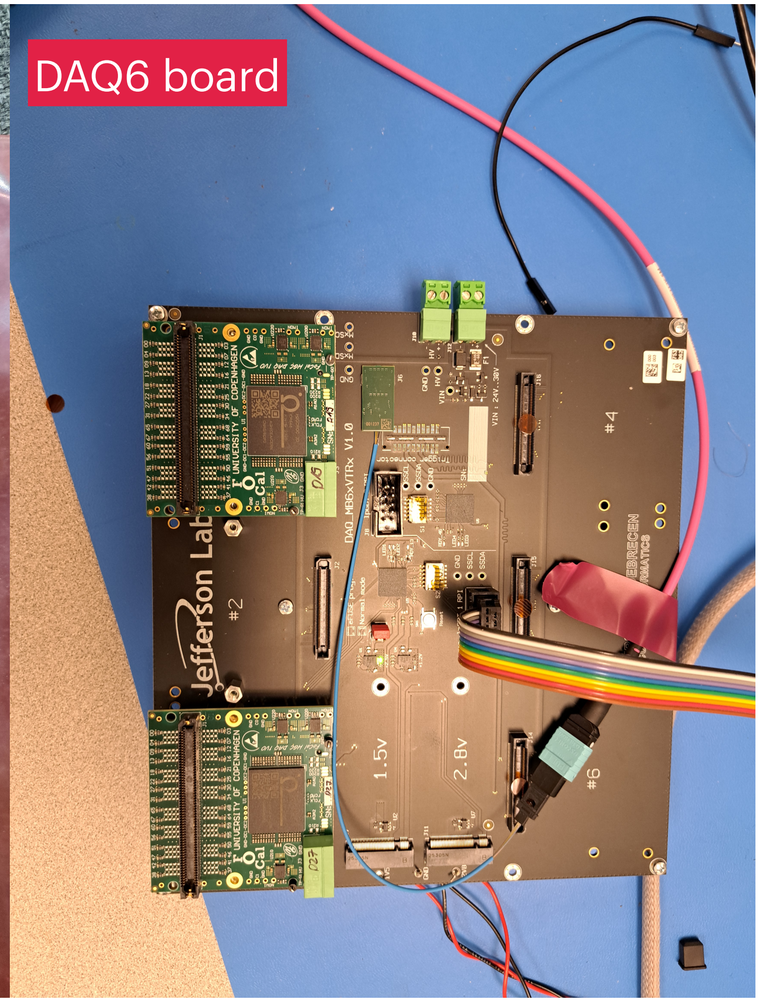
Hardware update



Produced 2 boards:

- DAQ3 board:
  - Accepts 3 H2GCROC mezzanines
  - SFP+ output, 10Gbps
- DAQ6 board:
  - 6 H2GCROC mezzanines
  - 2 LpGBT in master-slave configuration
  - VTRX+ for output, 2x10Gbps uplink

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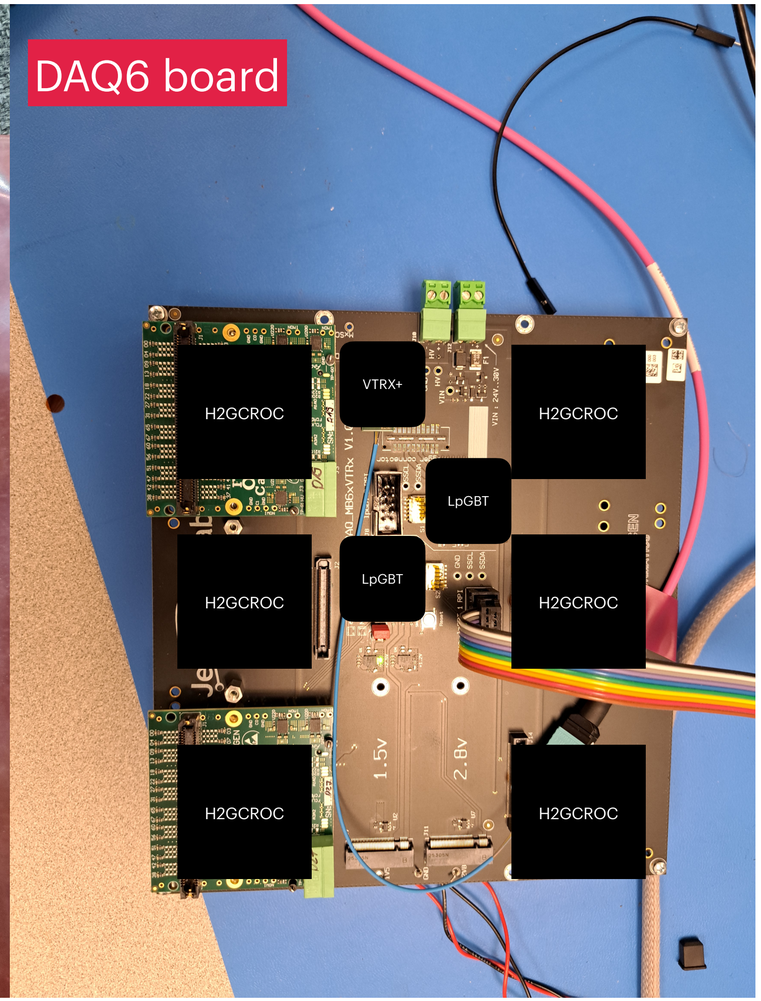

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Hardware issues:

- DAQ3, the SFP needs to be initialized from LpGBT (not ideal)
- DAQ6 has the VTRX+ flipped (collided with the trigger connector, that was solved)

Progress

- Connect to Zinq board with LpGBT firmware (borrowed from Jo Schambach)
  - When left alone it is stable
- Connect to Raspberry Pi to configure LpGBT
  - Has to pull up the I2C for the H2GCROC, might be on hardware in next iteration
- Send clock and FCMD to the H2GCROC in order to see the IDLE words coming
  - Saw it in Zinq board, looks good for all lines (need to do phase-adjustment, but so far very good sign)
- I2C setting from LpGBT to H2GCROC:
  - The LpGBT does not see yet the acknowledgment, scope we (maybe) see it
  - When touching the I2C lines, the lock with Zinq-LpGBT is sometimes lost (not good)