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Status report of the eRD109 project on SALSA chip development

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EPIC DAQ/electronics WG meeting

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STATUS OF THE PROTOTYPES

- **PRISMEv1 prototype** (PLL test chip)
  - Used to do tests of high-speed links and CDR decoding (implemented in PLL)
  - Radiation tests postponed again by CERN → May-June but not confirmed, facility still monopolized for BPOL problem
  - Facility found close to Saclay, able to irradiate ~20 Mrad X-ray per day, but not calibrated. Probes irradiated for test and calibration, not yet measured

- **SALSA1 prototype**
  - Radiation tests: same plans as PRISMEv1
  - No activity this month

CURRENT STATUS: SALSA2

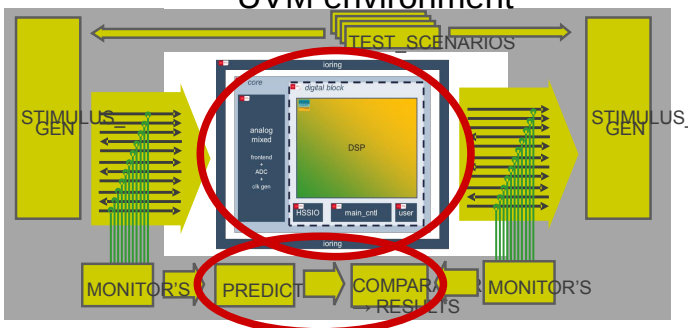
SALSA2 development status

- Front-end:
  - whole schematic done, including 2 x 16-channel blocks + service block (bandgap, biases, probes)
  - layout of 16-channel block done, including matrix of bumps + protections. Layout simulations done
  - layout of service central block including bumps ongoing, 1st version done (DRC + LVS ok)
- DSP
  - more modules finished (calibrations, fast command reception, readout state), some are done but are still being integrated (pattern generation)
  - First trials of synthesis, lead to size of around 23mm², smaller than expected; power consumption still being evaluated
- I/O: monitoring registers and fast command handling done, PLL integration ongoing, as well as adaptation of golden model timings. Tests of synthesis to be done to evaluate size and power consumption (delayed due to problems with Cadence license)
- Control core, ongoing: fast command decoding, state machine, monitor packets, monitoring reg.
- Floor plan: analog part almost done, DSP integr. started; evolution ongoing on pin-out definition
- UVM environment: workspaces created for each block, 1st version done for each, updates ongoing, alignments of golden models with RTL code ongoing, advanced scenarios to be done

Timeline

- Still a lot of works ahead: code validation, integration, layout generation, block assembly, simulation of whole chip
- Chip submission foreseen Q3 2026, MPW submission slots before summer already full
- Tests from beginning 2027
- Distribution to users in 2027

UVM environment



PROJECT MILESTONES AND NEXT STEPS

eRD109 FY24 project milestones

- SALSA2 specifications → July 2024
- SALSA2 submission → at least Q3 2026
- Beginning of SALSA2 tests → beginning of 2027

eRD109 FY25 project milestones

- SALSA3 design specifications → aiming 2nd semester 2026 (after SALSA2 submission)
- SALSA3 submission → 1st semester 2027
- Performance evaluation → 2nd semester 2027 - 1st semester 2028

Very next steps

- SALSA1 tests → TID tests in May or June hopefully...
- PRISMEv1 chip → TID tests in May or June
- SALSA2 development → in progress