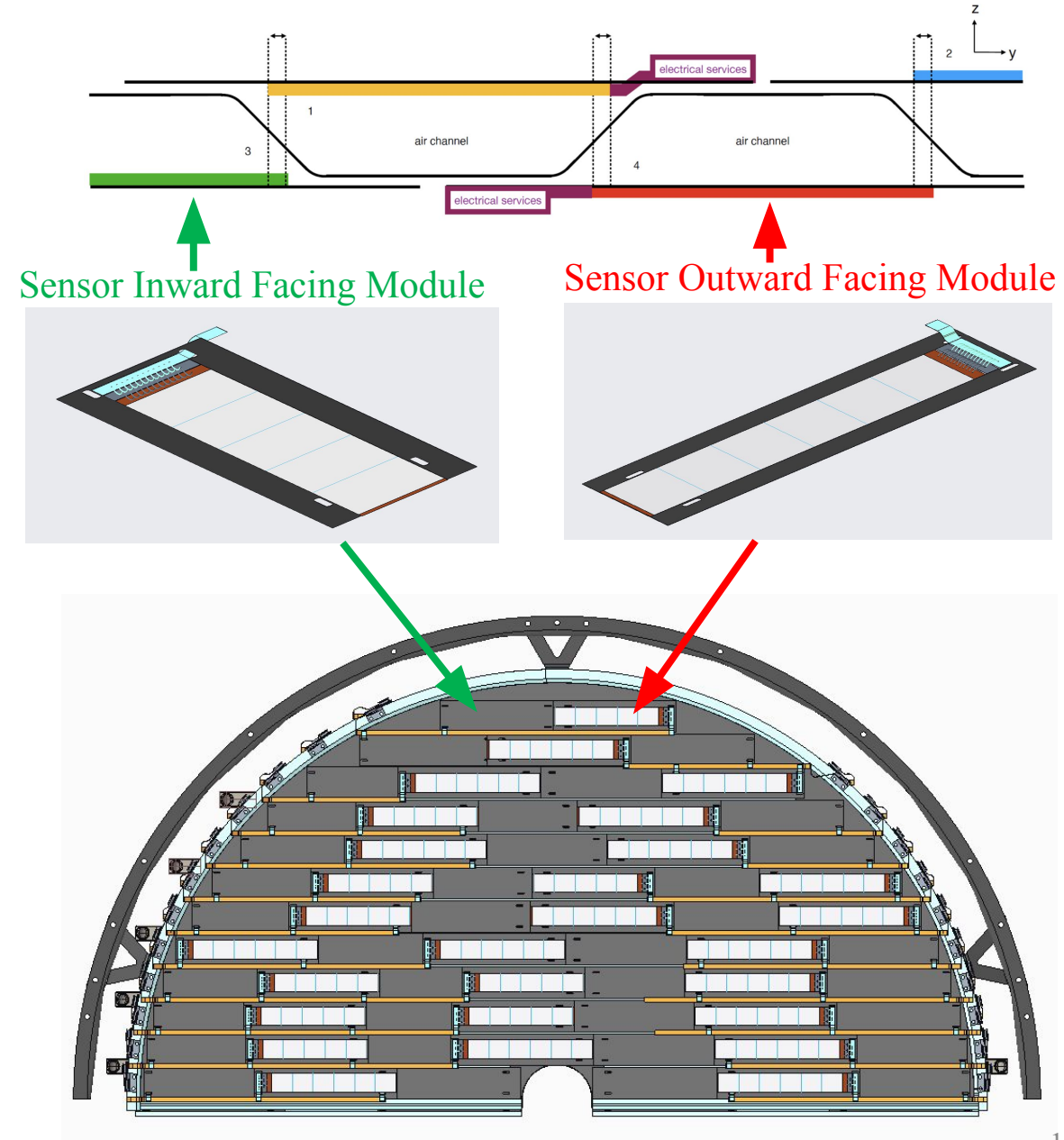
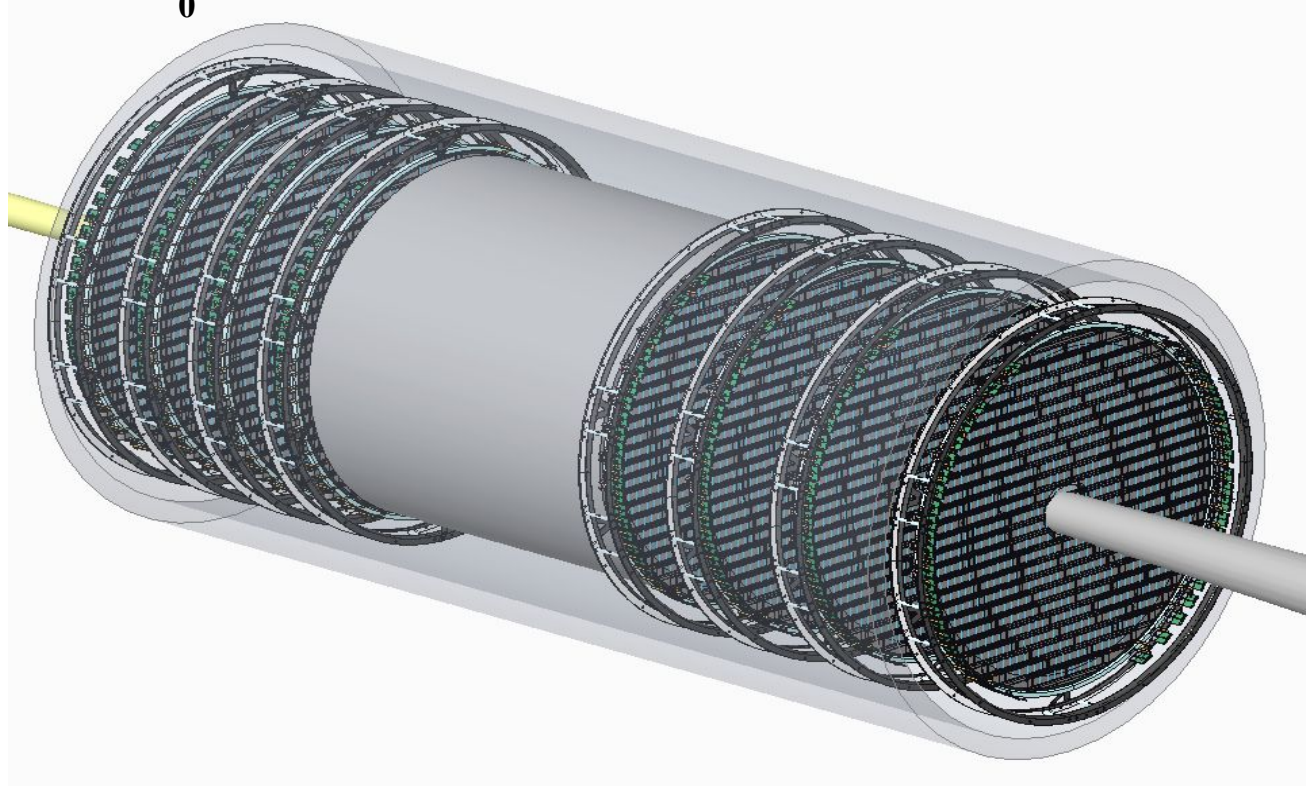
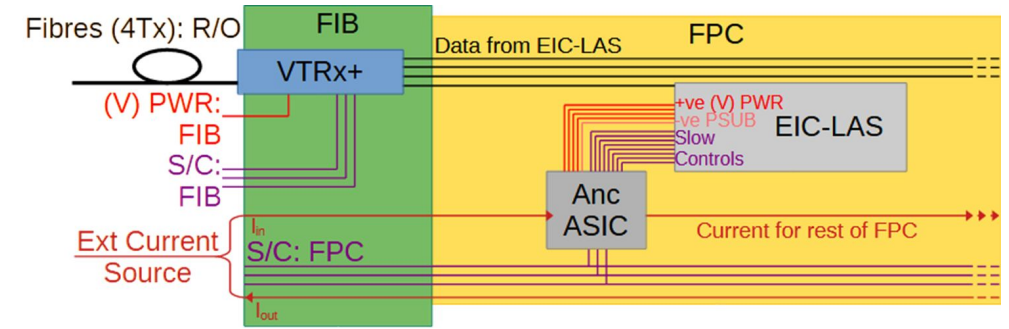
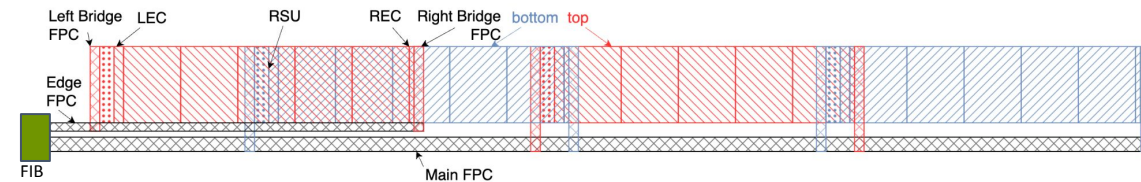
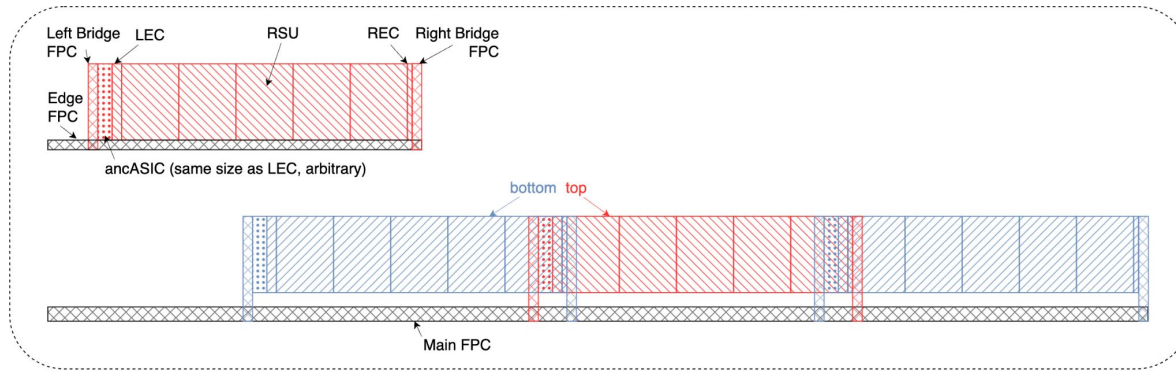


ePIC SVT Disks

- **EIC Large-Area Sensor** with design based on ITS3 MOSAIX, mounted on low-mass CF support structure with integrated air cooling
- **AncASIC** provide negative sensor bias voltage, serial power and slow control
- **Outer radius** ranging from 24 to 40 cm
- $X/X_0 \sim 0.24\%$



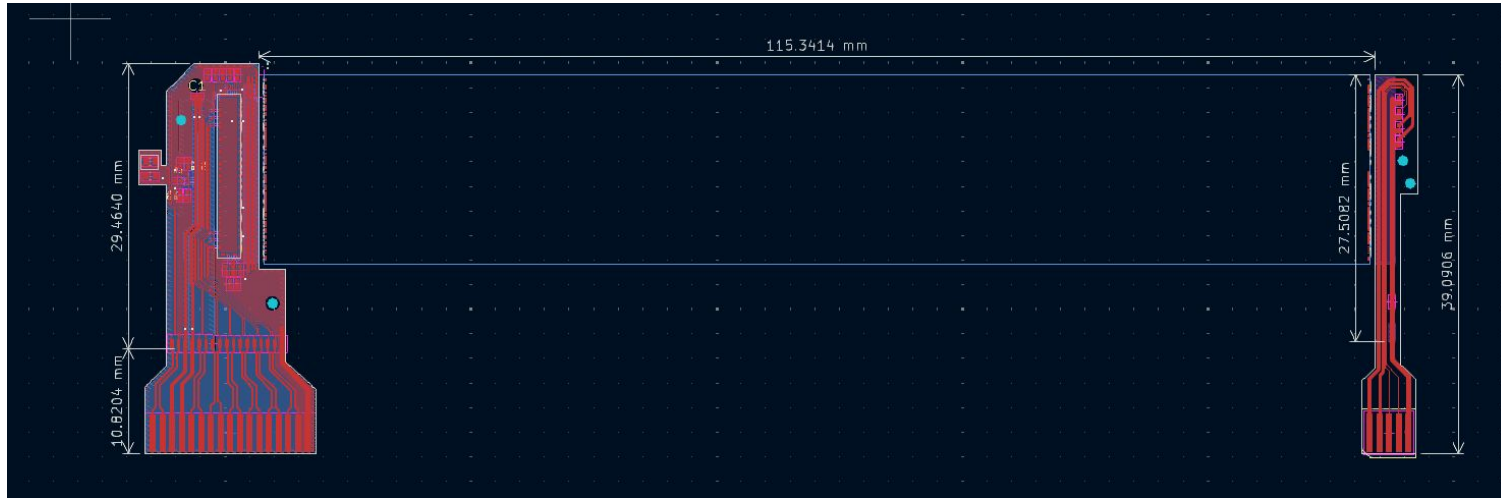
Electrical Interfaces for SVT Disks



bold: preferred option

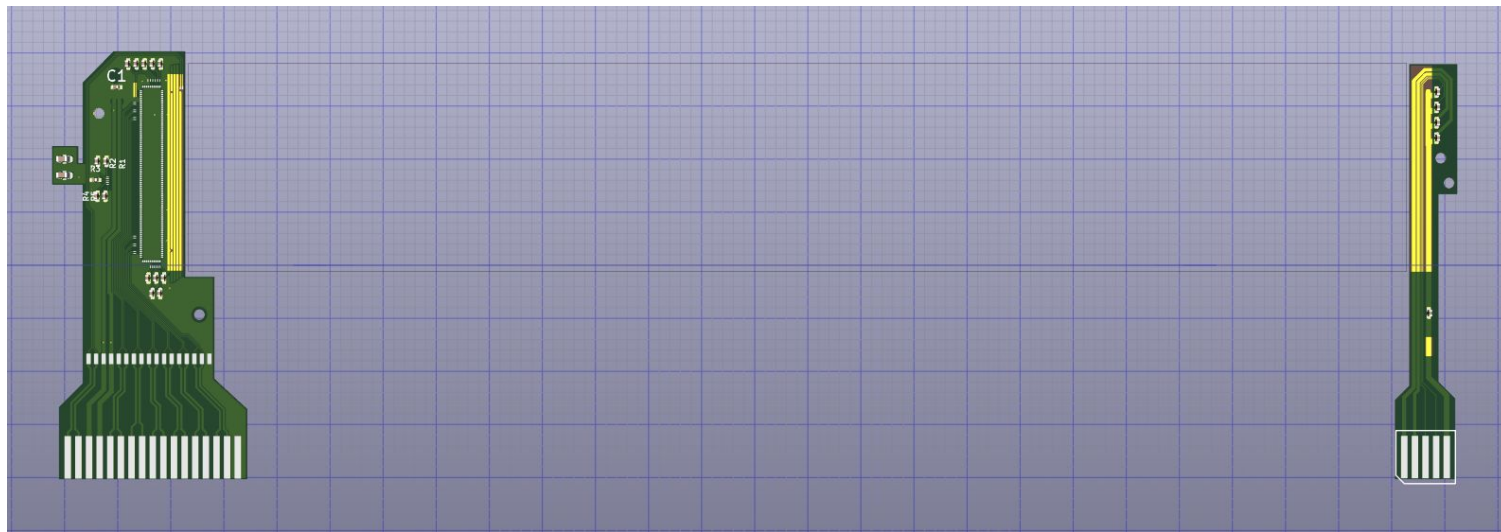
	FIB	Main/Edge FPC	Bridge FPC	AncASIC	EIC-LAS
FIB					
Main/Edge FPC	Connector, Soldering				
Bridge FPC	N/A	soldering, wire/TAB-bonding			
AncASIC	N/A	N/A	wire-bonding, TAB-bonding		
EIC-LAS	N/A	N/A	wire-bonding, TAB-bonding	wire-bonding	

Bridge FPC - Overview



- **Left bridge FPC with AncASIC** will handle **EIC-LAS** LEC power, slow control, high-speed data transmission.

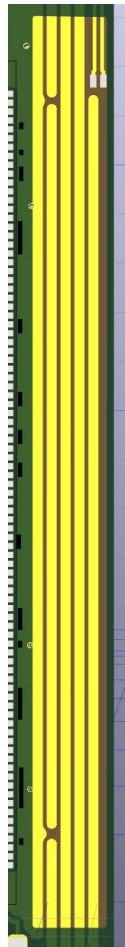
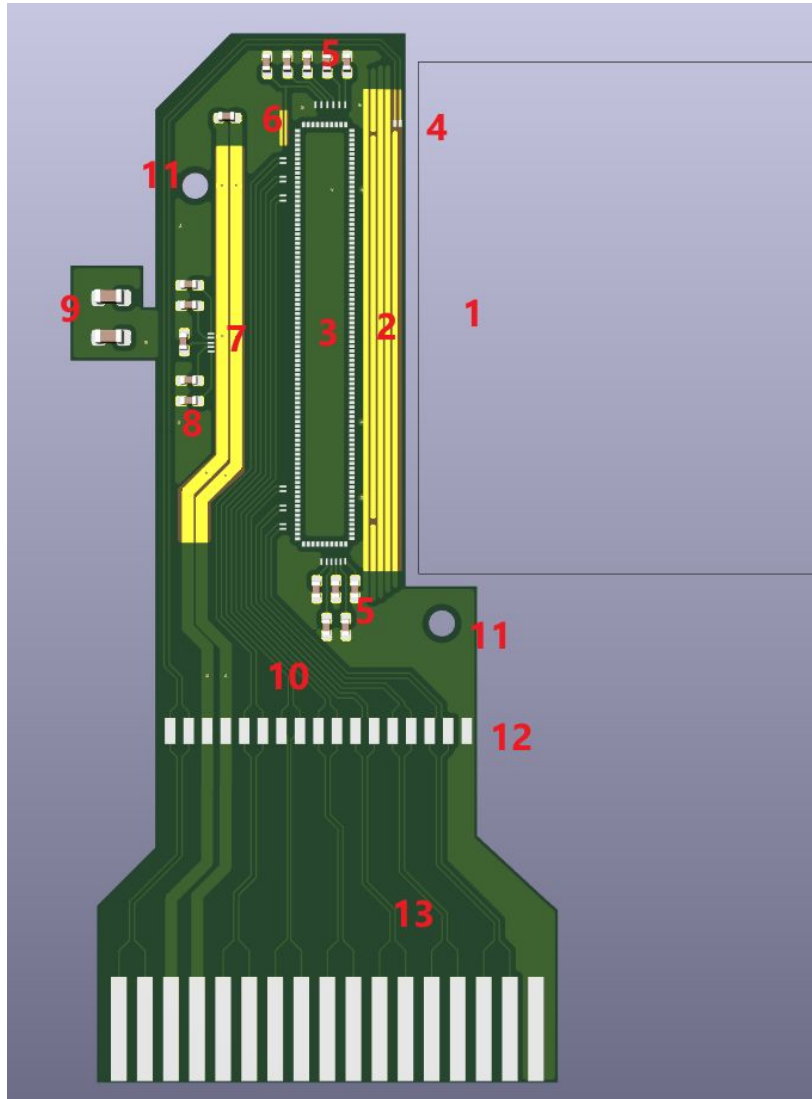
	Area (mm ²)	Copper area (mm ²)	Fill factor
Top Layer	278.2	190	0.69
Bottom Layer	278.2	260	0.94



- **Right bridge FPC** with power buses connected to GND through decoupling capacitors will connect to the **EIC-LAS REC**.

	Area (mm ²)	Copper area (mm ²)	Fill factor
Top Layer	78.9	32.9	0.42
Bottom Layer	78.9	0	0

Left-side bridge FPC



1. Left side of EIC-LAS

The distance between LAS and the FPC is **0.508 mm**. The size of the LAS is assumed as **114.330 * 19.564 mm**.

2. Power Bus

Net name from left to right: GND, PSUB, TXVDD, GSVDD, GAVDD, GDVDD.
Each trace is **8 mil width with 3 mil spacing**.

3. AncASIC

The distance between the edge of AncASIC and LAS is **2.4 mm**. The size of the ASIC is assumed as **16.434 mm × 2.388 mm**.

4. Pads of the HSD

width/space = 55um / 140 um. Since the pads of the HSD on LAS haven't been confirmed, I choose the HS_DATA<0> of MOSAIX as the HSD pad in this design. Length of HSD_P = 48.4mm, HSD_N = 48.9mm.

5. Decoupling Capacitors

All of the Decoupling Capacitors are in the 0201 footprint.

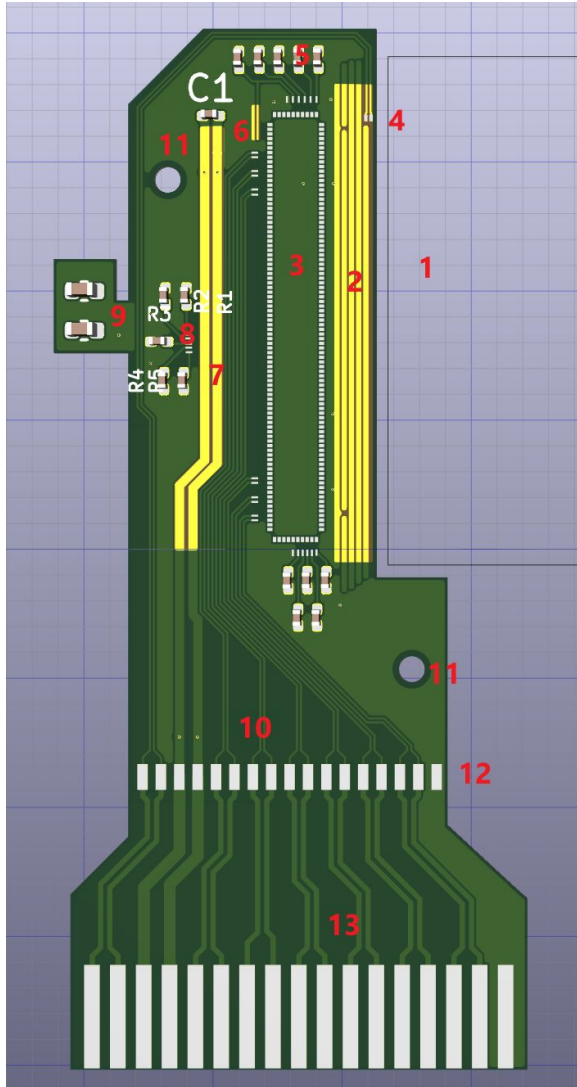
6. AncASIC address

There is an open window on the soldermask, so the address pads of AncASIC can be wire-bonded to ABVDD or GND.

Note 1: The 55um / 140um dimensions are empirical parameters for achieving $Z_{diff} = 100\Omega \pm 10\Omega$, which need to be validated through sample production and testing.

Note 2: The dimensions of the AncASIC are calculated as follows: $(\text{pad number} - 1) \times \text{pitch} (180 \mu\text{m}) + \text{pad width} (\text{assumed to be } 5 \text{ mil}) + \text{Corner Cell Width} (300 \mu\text{m}) \times 2$. The theoretical dimensions are 16.385 mm × 2.345 mm. Due to the precision limitations of the design software, the final dimensions are 16.434 mm × 2.388 mm. These dimensions only serve solely as a reference for the placement and routing of other components on the FPC.

Left-side bridge FPC



7. Iin/Iout bus

Width of Iin/Iout = 18 mil. To reduce the power consumption, there is another plane for each net on the bottom layer (see power consumption page)

8. SLDO Reference Current Resistor

All of the resistors are in the 0201 footprint.

9. Stiffer test

JLC suggested the FPC designer place a stiffer beneath the device that needs to be soldered. In this prototype, we placed a stiffer on this area to evaluate the impact of stiffer. There are two 0402 pads in this area, with a stiffener placed underneath one of them. We designed this structure to verify whether an FPC without a stiffener can **withstand the high temperatures of soldering**.

10. Slow control signals

Width/Spacing 55 um/140um.

11. Mounting hole

NPTH hole, diameter = 1 mm.

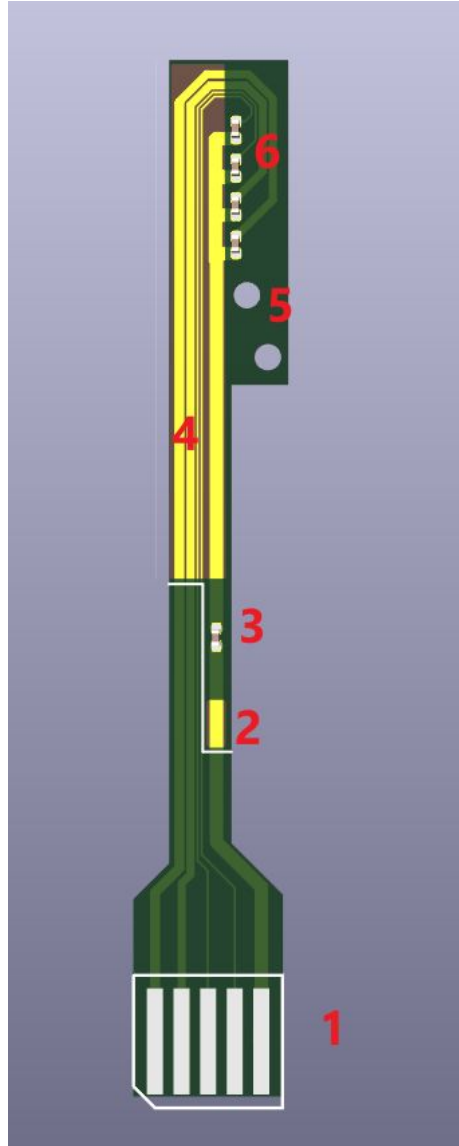
12. FPC Soldering Pads

The pads on the bottom edge are used to solder the bridge FPC to main FPC, pad width/spacing (**0.4mm/0.3mm**).

13. FPC wrapper

The FPC wrapper is designed to facilitate connecting this FPC to a test PCB with FPC connector such as 0522711779 Molex to facilitate module electrical test. The wrapper will be removed after QA.

Right-side bridge FPC



1. FPC wrapper.

The FPC wrapper is designed to facilitate connecting this FPC to a test PCB with FPC connector such [2005280050 Molex | Connectors, Interconnects | DigiKey](#), to facilitate module electrical tests. The wrapper will be removed afterwards.

2. Solder pads

Solder to the GND net on the Main FPC.

3. AC coupling Capacitors

The ground is AC coupled to the ground on the main FPC.

4. Power/GND Trace:

From left to right, net names and widths are **GDVDD (15mil)**, **GAVDD (12 mil)**, **GSVDD (3 mil)**, and **PSUB (3mil)**.

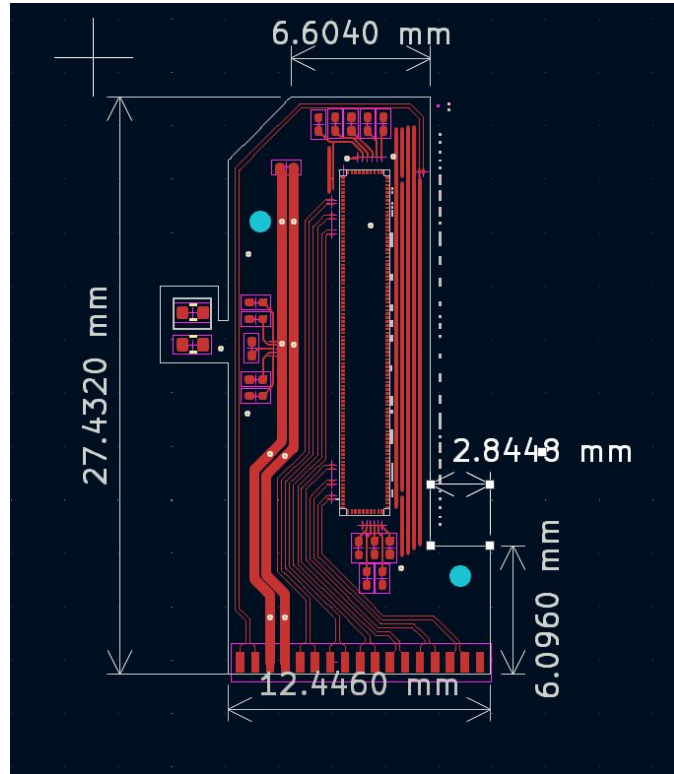
5. Mounting hole:

NPTH hole, **diameter = 1 mm**.

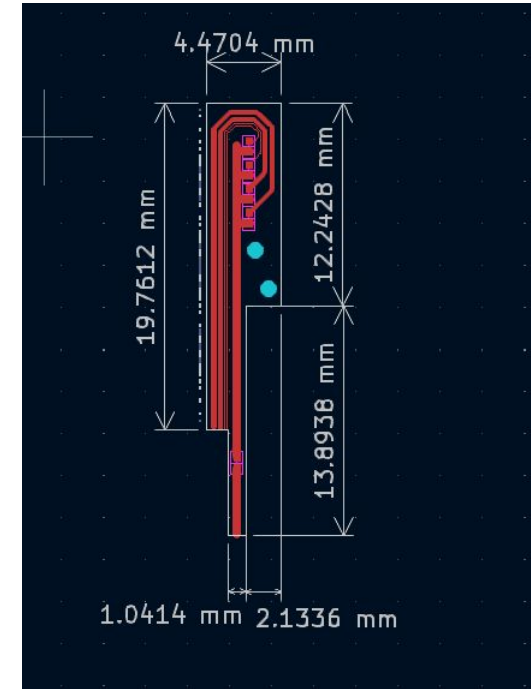
6. Decoupling Capacitor:

All of the resistors are in the 0201 footprint.

Bridge FPC - Feature dimensions

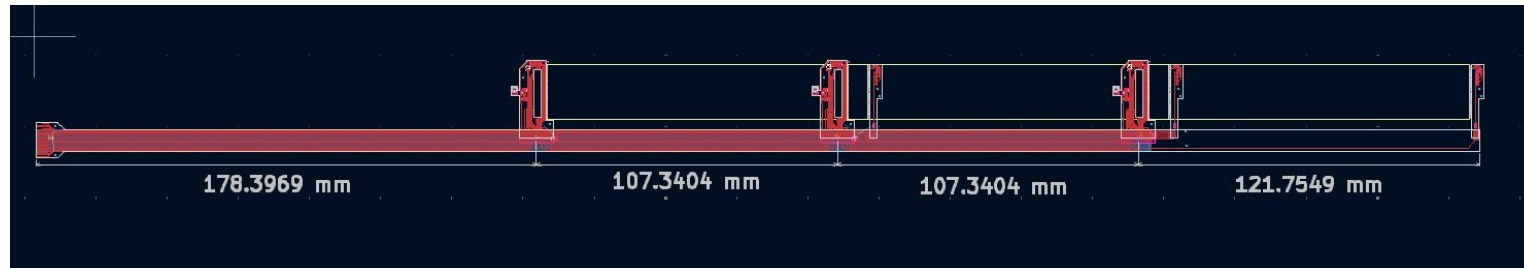
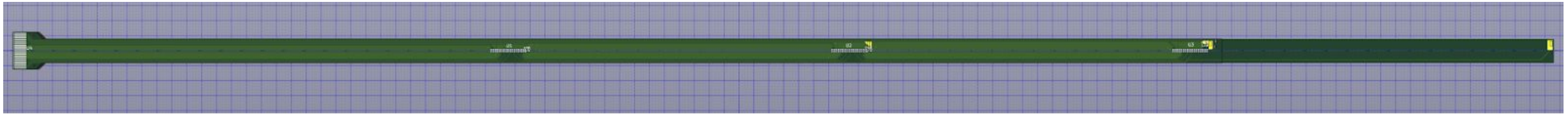
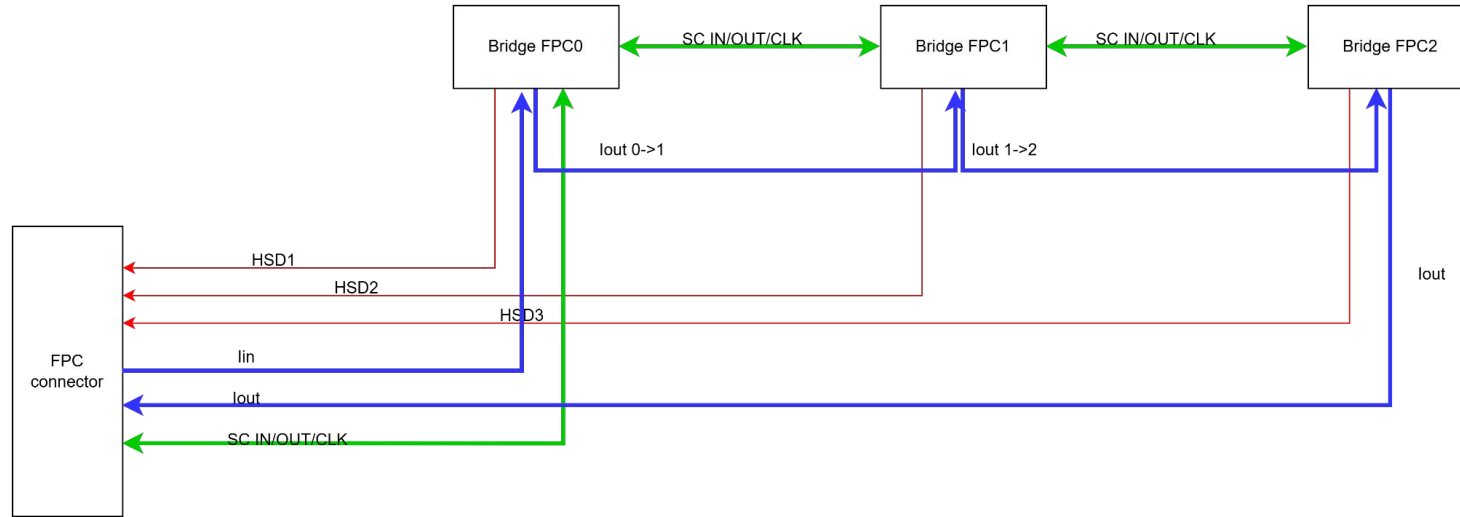


	Area (mm ²)	Copper area (mm ²)	Fill factor
Top Layer	276.2	190	0.69
Bottom Layer	276.2	260	0.94



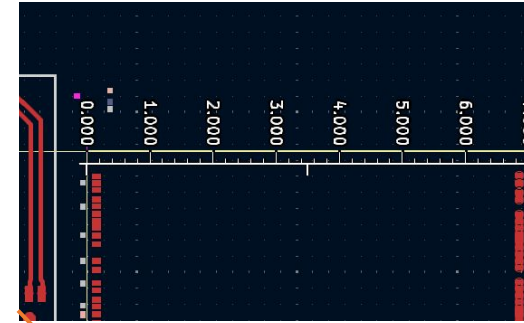
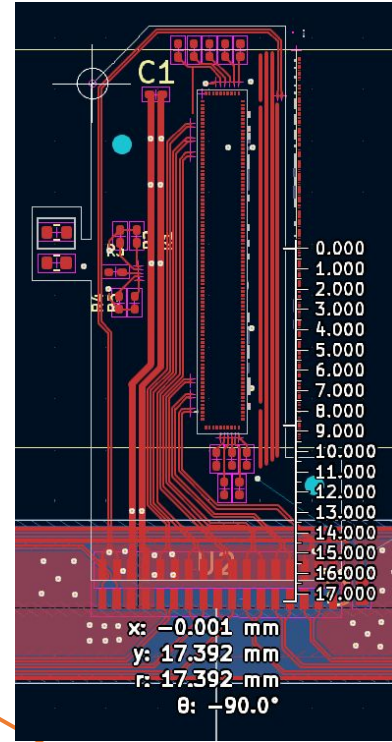
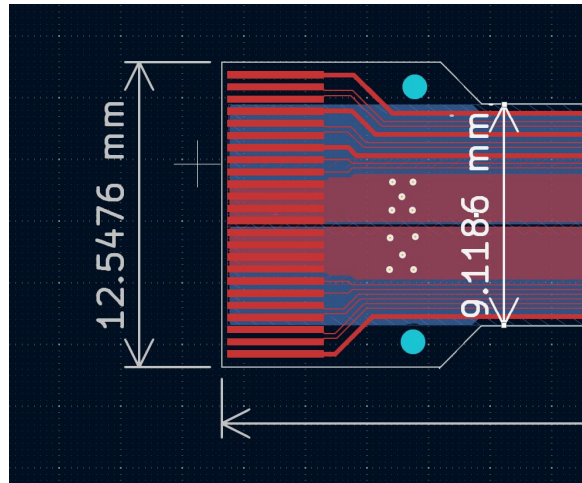
	Area (mm ²)	Copper area (mm ²)	Fill factor
Top Layer	78.9	32.9	0.42
Bottom Layer	78.9	0	0

Main FPC Overview

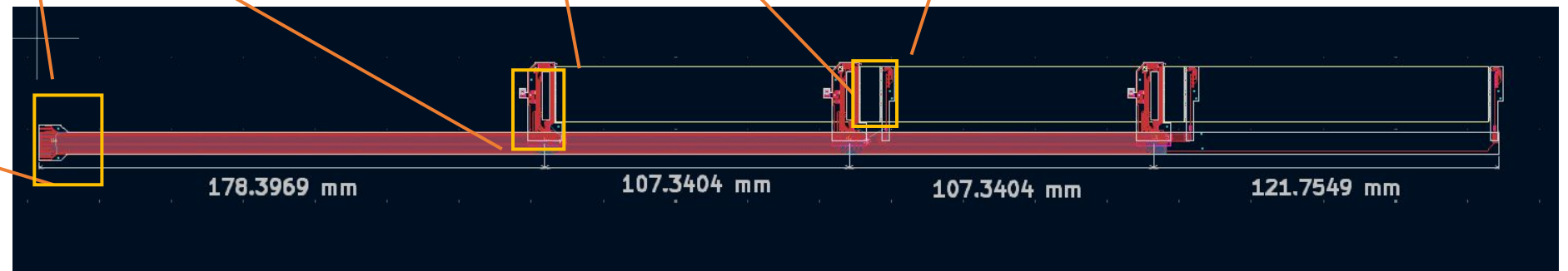


	Area (mm ²)	Trace Area (mm ²)	Power net area (mm ²)	Fill factor
Top Layer	4747.6	221.5	1875.6	0.45
Bottom Layer	4747.6	0	3202.2	0.68

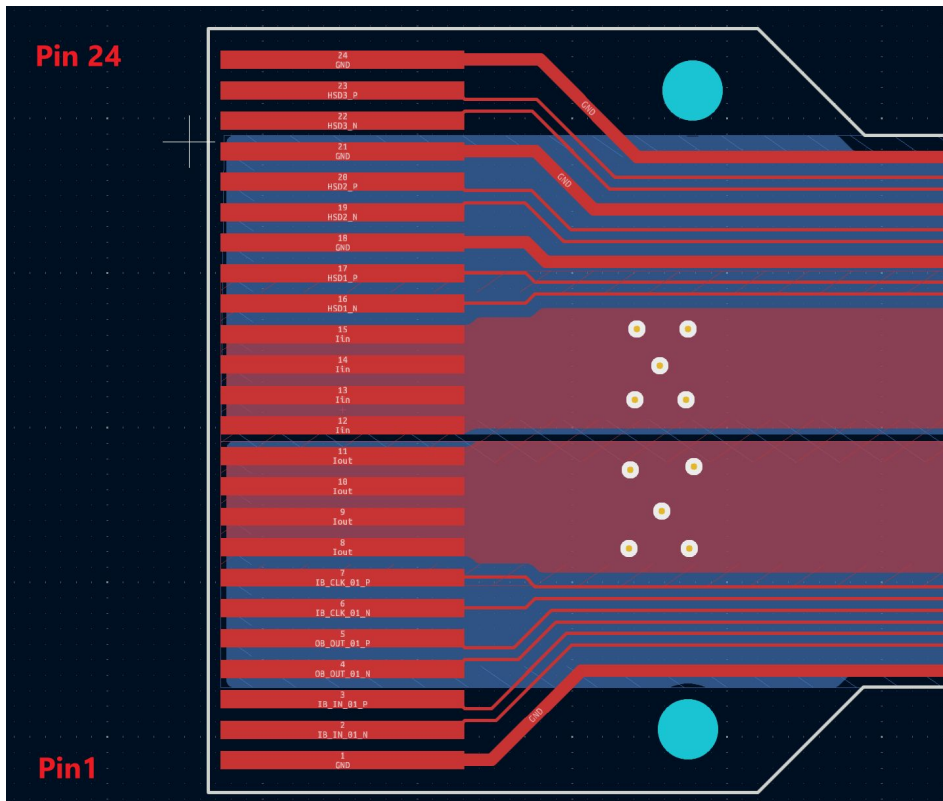
Main FPC - feature dimensions



Connector end width	12.5476mm
Body width	9.1186mm
Total length	514.83mm
Distance between Center of sensor and Main FPC	17.385 mm (theoretic) 17.392 mm (reality)
Overlap of RSU	1mm
Area	4747.6 mm ²
Fill factor Top	0.45
Fill factor Bottom	0.68



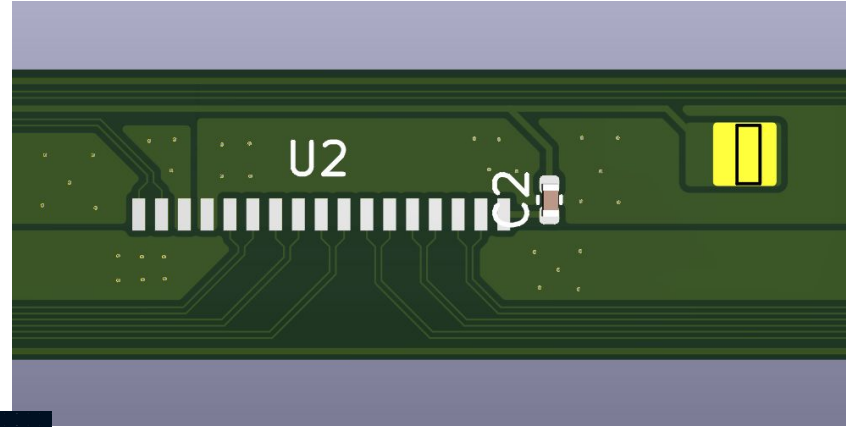
Main FPC - connector and nets



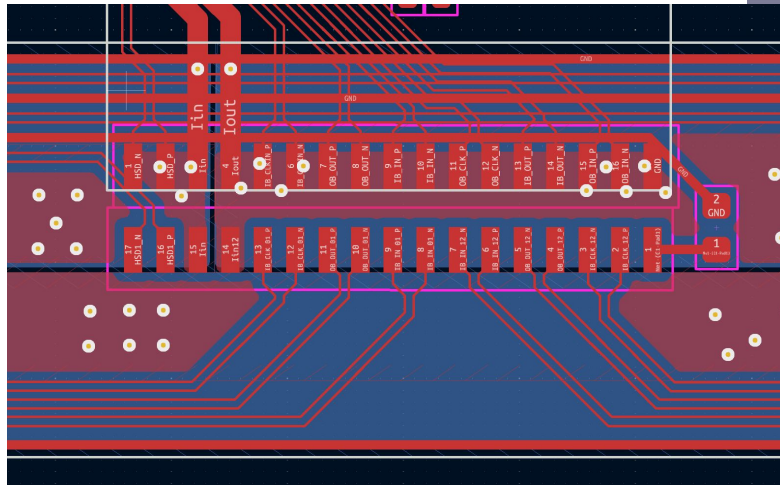
Pin Number	Description
24,21,18,1	GND trace, width = 0.2 mm
23,22	High Speed Data, connect to Bridge FPC2, width/spacing = 3 mil, length = 387 mm.
20,19	High Speed Data, connect to Bridge FPC1, width/spacing = 3 mil, length = 272 mm.
17,16	High Speed Data, connect to Bridge FPC0, width/spacing = 3 mil, length = 160 mm.
12-15	Iin (See following pages for details)
8-11	Iout (See following pages for details)
7,6	SC_CLK, width/spacing = 3mil,length = 162mm
5,4	SC_OUT, width/spacing = 3mil, length =162 mm
3,2	SC_IN, width/spacing = 3mil, length = 164 mm

Note: All GND traces are not interconnected on the main FPC; therefore, common grounding must be established externally (e.g. FIB) if needed.

Connecting Bridge FPCs to Main FPC

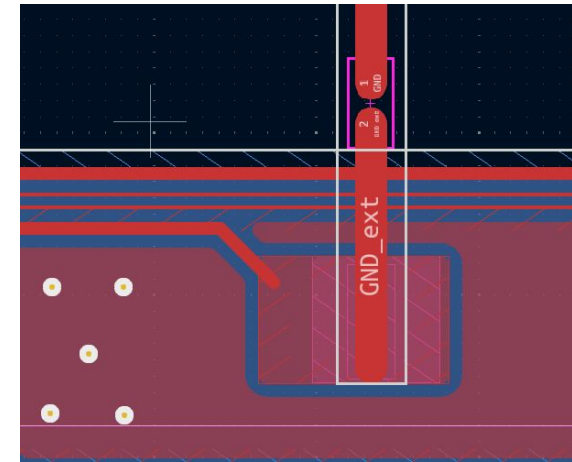


Left Bridge FPC:



The left bridge FPC will be soldered to the main FPC by 17 pairs of pads. **Each pad has width 0.4mm, length 1mm, pitch 0.7mm.**

Right Bridge FPC:



The right bridge FPC will be soldered to the main FPC by 1 pair of pads.

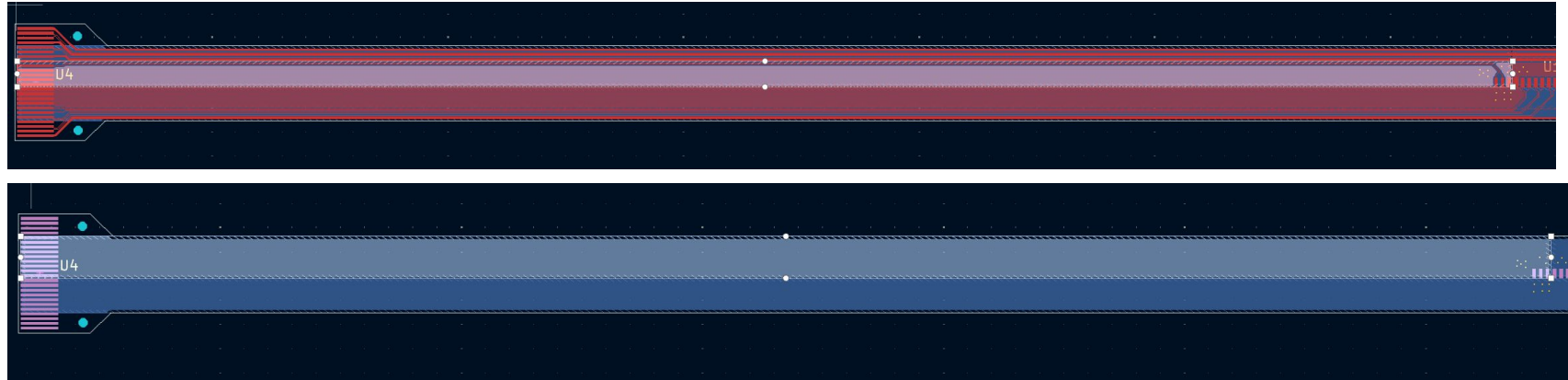
FPC Cross section

JLC	LTU
Pi: 12.5 um	Pi: 25um
Copper: 12 um	Aluminum: 15 um
	Pi: 10 um
Glue: 15 um	Glue: 5 um
Dielectric:25 um	Dielectric:25 um
Glue: 15 um	Glue: 5 um
Copper: 12 um	Aluminum: 15 um
	Pi: 10 um
Pi: 12.5 um	
Total: 104 um	Total: 125um

We plan to produce “mechanical” FPC prototypes with Cu traces by JLCPCB.

The power consumption calculations in the following slides are based on the LTU’s Al-based FPC structure.

Main FPC - Power consumption Estimation

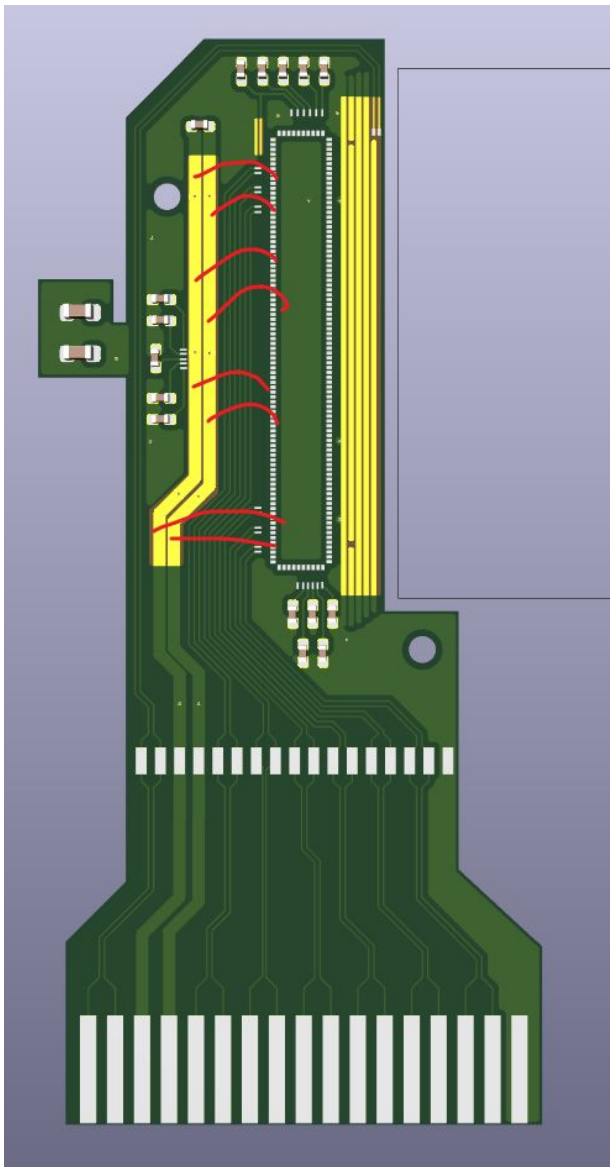


Net Iin on Top and Bottom Layer

Net	From	To	Material	Resistivity@ 20°C (ohm·m)	Thickness (m)	length (m)	Width on top (m)	Width on bottom (m)	Resistance Top	Resistance Bottom	Resistance
Iin	FPC connector	Bridge FPC0	Aluminum	2.65E-08	1.50E-05	0.17	0.00196	0.00460	1.53E-01	6.53E-02	4.58E-02
Iin12	Bridge FPC0	Bridge FPC1	Aluminum	2.65E-08	1.50E-05	0.107	0.00282	0.00460	6.70E-02	4.11E-02	2.55E-02
Iin23	Bridge FPC1	Bridge FPC2	Aluminum	2.65E-08	1.50E-05	0.107	0.00371	0.00460	5.10E-02	4.11E-02	2.27E-02
Iout	Bridge FPC2	FPC connector	Aluminum	2.65E-08	1.50E-05	0.387	0.00228	0.00371	3.14E-01	1.84E-01	1.16E-01

Assume the Iin/Iout current is 1.5 A, The power consumption is estimated as 473 mW.

Bridge FPC power consumption Estimation – Iin/Iout

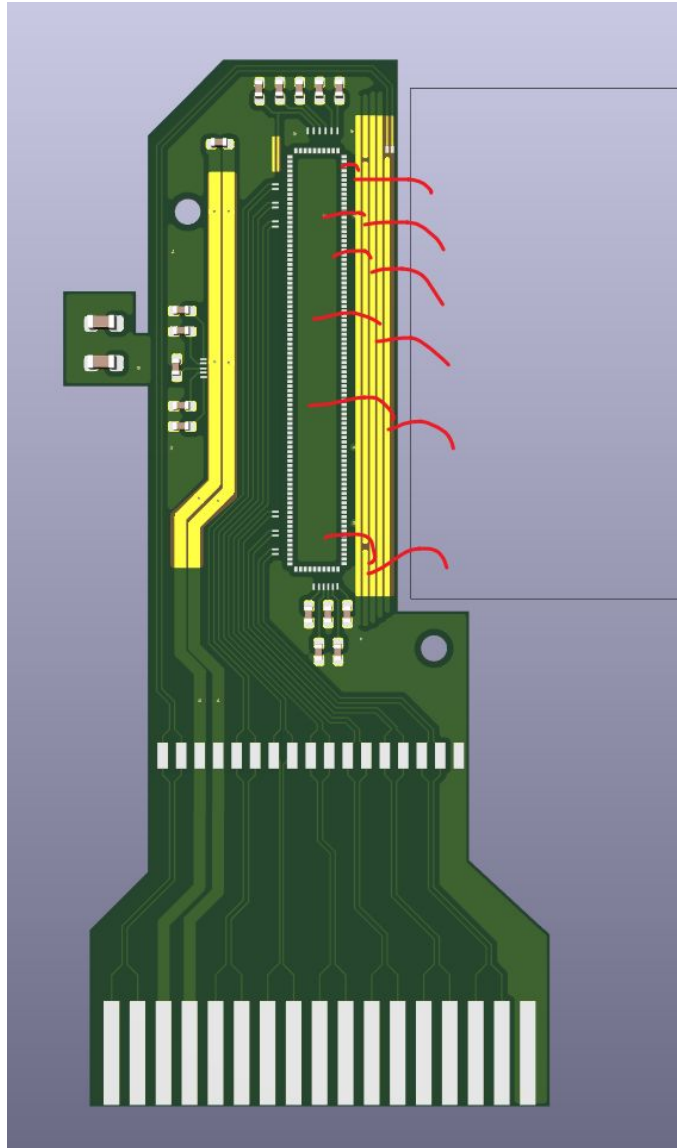


The resistance of Iin/Iout can be divided into two parts: Trace on FPC and bonding wire.

The estimated resistance and the parameters that used in the calculation is shown in the following:

Trace on FPC		Bonding wire	
ρ :Resistivity@20°C (ohm·m)	2.65E-8	ρ :Resistivity@20°C (ohm·m)	2.65E-8
H:Thickness (m)	1.50E-5	D:Diameter (m)	2.54E-5
W:Width on top (m)	0.0003084 (lin/lout)	L:Mean length (m)	0.0029(lin); 0.0023(lout)
Width on the bottom (m)	0.0022(lin); 0,0027(lout)		
L:Mean length (m)	0.017(lin/lout)	N:wire number	27(lin); 40 (lout)
Resistance (ohm)	0.0118 (lin) 0.0098(lout)	Resistance (ohm)	5.6e-3(lin);3e-3(lout)

Assume the current is 1.5 A, The power consumption is estimated as 68 mW. The main contribution is from the trace of Iin/Iout on FPC (~49 mW).



The power consumption of TXVDD/GSVDD/GAVDD/GDVDD can be divided into two parts: 1. From AncASIC to power bus; 2. From the power bus to the left edge of LAS (Power loss on the power bus is insignificant, as the current travels only a short distance on the it);

From AncASIC bonding to power bus		From power bus to left edge of LAS	
ρ : Resistivity@20°C(ohm·m)	2.65E-8	ρ : Resistivity@20°C (ohm·m)	2.65E-8
D:Diameter (m)	2.54E-5	D:Diameter (m)	2.54E-5
L(mm):	0.8(TXVDD); 1.1(GSVDD); 1.4(GAVDD); 1.7(GDVDD)	L1(mm):	1.9(TXVDD); 1.6(GSVDD); 1.3(GAVDD); 1(GDVDD)
Number of bonding wire:	3 (TXVDD); 6(GSVDD); 4(GAVDD); 15(GDVDD)	Number of bonding wire:	6 (TXVDD); 12(GSVDD); 8(GAVDD); 20(GDVDD)
Resistance:	1.4e-2(TXVDD);9.6e-3(GSVDD); 1.8e-2(GAVDD);5.9e-3(GDVDD)	Resistance:	1.7e-2(TXVDD);7.0e-3(GSVDD); 8.5e-3(GAVDD);2.6e-3(GDVDD)

Calculate the operating current for each power based on updated numbers form Chamonix:

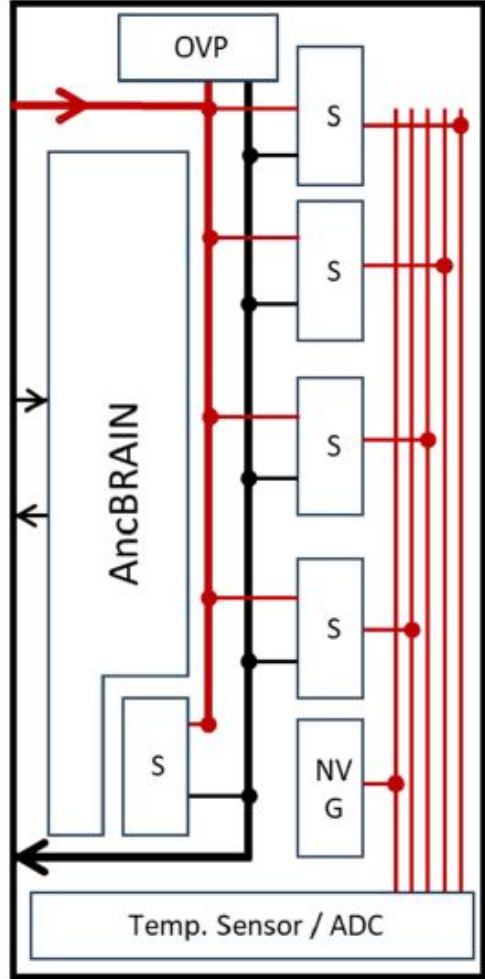
The power consumption on power net is 6.3 mW

	Voltage(V)	Typ Power (mW)			Max Power (mW)		
		ESR	Cham	Cham-SC	ESR	Cham	Cham-SC
GAVDD	1.32	222	222	222	356	356	356
GDVDD	1.32	908	1052	349	1148	1280	560
GSVDD	1.32	52	38	38	78	55	55
TXVDD	1.2	240	71	66	360	100	91
Total (LAS)		1422	1382	675	1942	1791	1062

Summary and Outlook

- **FPCs** provide electrical interfaces between EIC-LAS, AncASIC and FIB (lpGBT and VTRX+).
- A first layout design is completed for SVT disk FPC, taking into account the requirements of power and data transmission.
- Plan to produce a first batch of Cu-based mechanical prototypes to check FPC dimensions and inter-connection, with the main goal to facilitate disk module development.
- Will engage with **LTU** to design and produce Al-based FPCs for electrical functionality tests.
 - On-going work by UK and Trieste for bonding and data transmission with LTU FPCs

Sanity check on the “LAS side” of B-FPC



LEC

GSVDD/GSVSS

GAVDD/GAVSS

GDVDD/GDVSS

TXVDD/TXVSS

PSUB

HS DATA

CTRL,CLK, ETC

LEC: 152 pads, size: 144*91 um²;

~ symmetric pad distribution:
1 to 76; 77 to 152;

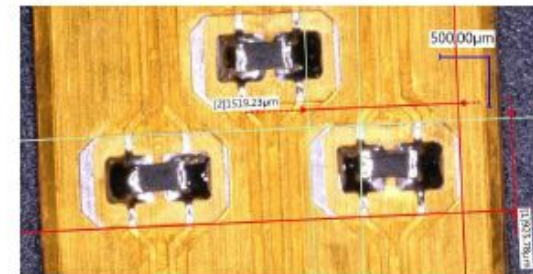
Q: GSVSS, GAVSS, GDSS, TXVSS, PSUB
have common ground?

Caps between AncASIC & LAS

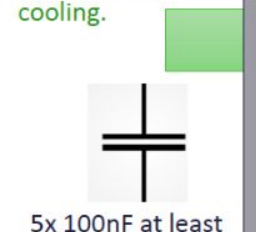
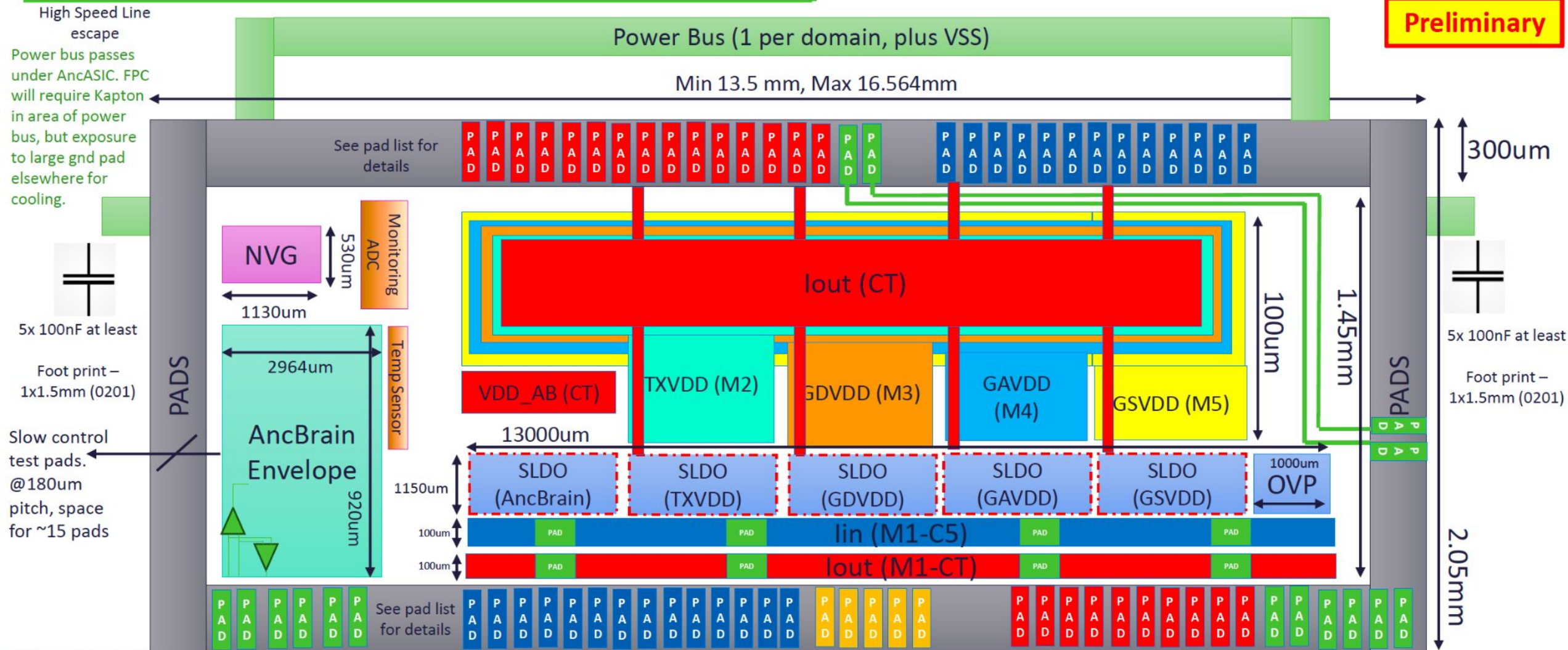


Example from LTU-made prototype FPC.

- On FPC components: 0201 (imperial).
- Sit within a 1 × 1.5 mm window.
- Exact position on b-FPC depends on location of (MOSAIX) pads for the power domains.
 - Number of caps needed is still to be determined.



Preliminary

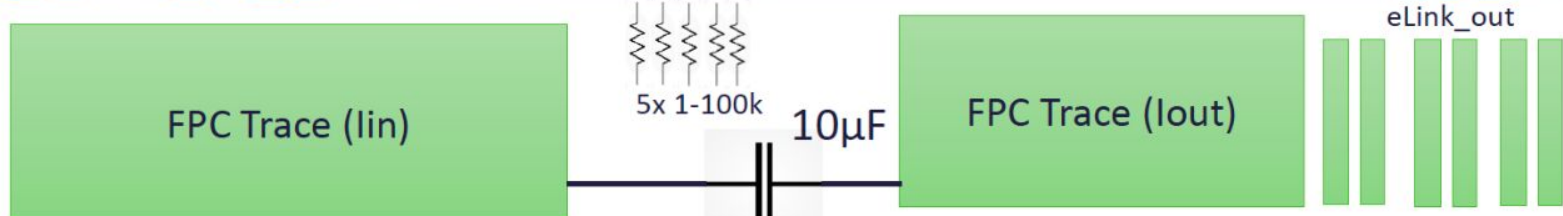
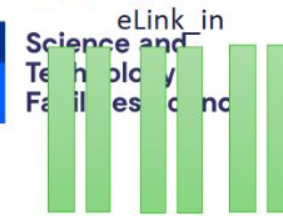


Foot print – 1x1.5mm (0201)

Slow control test pads. @180um pitch, space for ~15 pads



Foot print – 1x1.5mm (0201)



ePIC SVT Disk Architecture

ePIC SVT - disk and barrel power and readout architecture

Sichtermann, Glover, Silber

Rev	Date	Author	Description
v1	2025-10-09	Joe Silber (LBNL)	imported <u>original diagram from Ernst</u> , added details on sizes, counts, and connection interfaces
v2	2025-10-15	Joe Silber (LBNL)	visual cleanup, approx dims on furcation tubes, power wire pairs, and CB-FIB ribbon
v3	2025-10-16	Joe Silber (LBNL)	incorporated comments from Nikki on barrel vs disk variations; made MFPC and bridge connections more visually clear
vx			in-progress – added ref links

Nomenclature

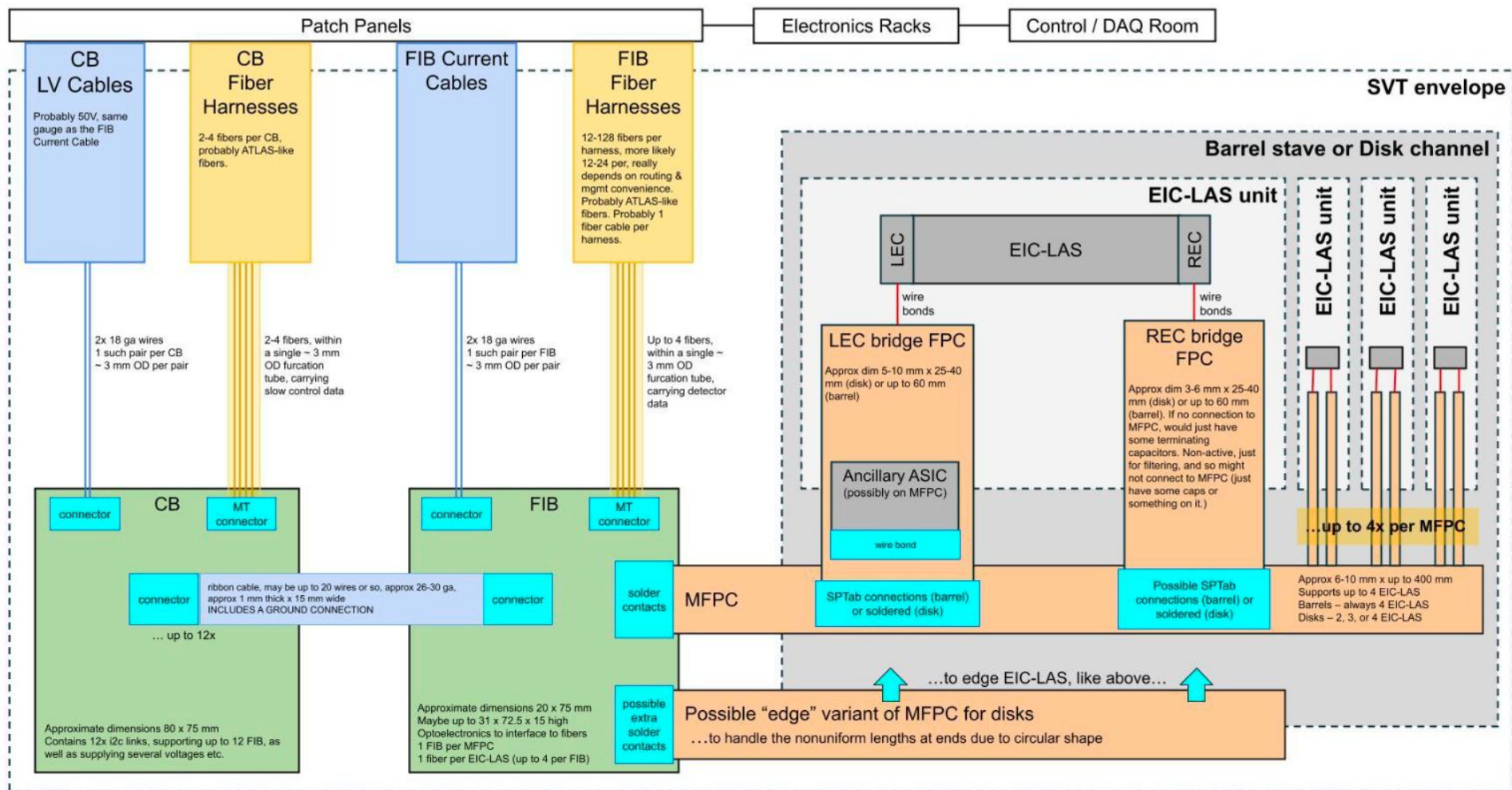
FPC ... Flexible Printed Circuit
 CB ... Control Board
 FIB ... FPC Interface Board
 LV ... Low Voltage
 MFPC ... Main FPC
 BFPC ... Bridge FPC
 SPTab ... bonded overlapping Al/Kapton

Notes

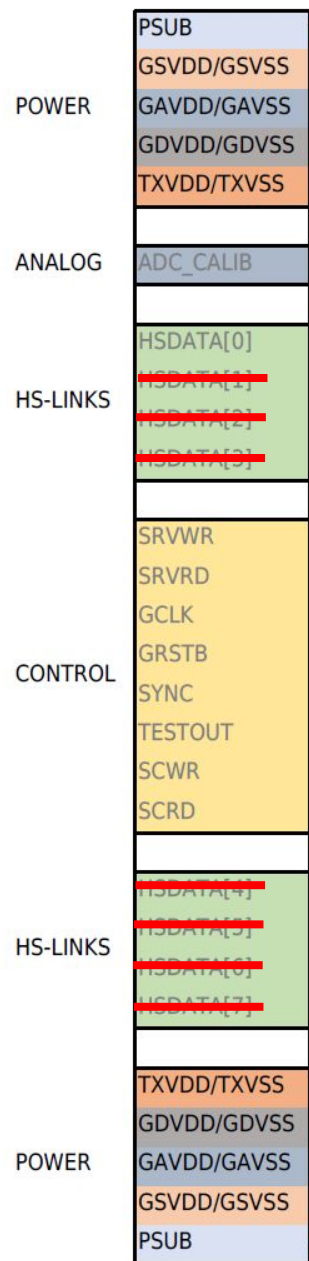
- Not to scale.
- Color-coding consistency not guaranteed.

References

- [module drawing from Nikki 2025-08-22](#)

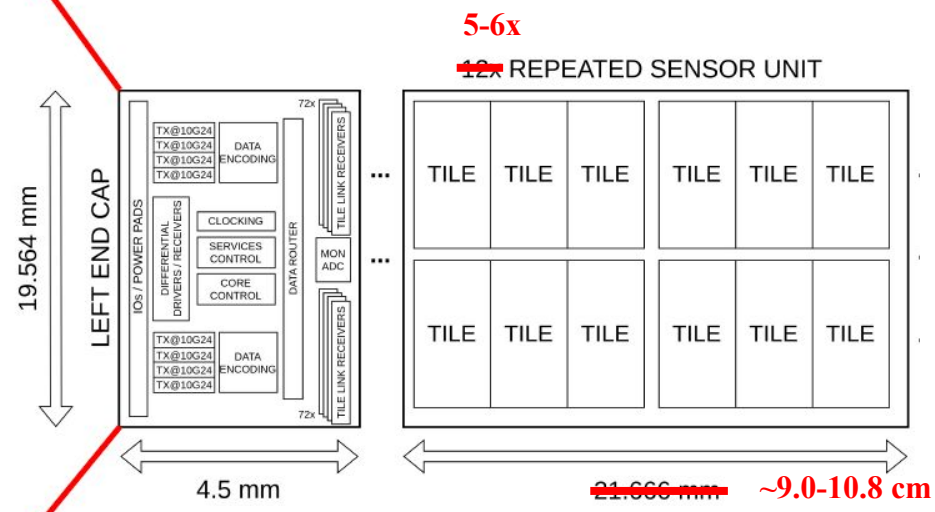


EIC-LAS



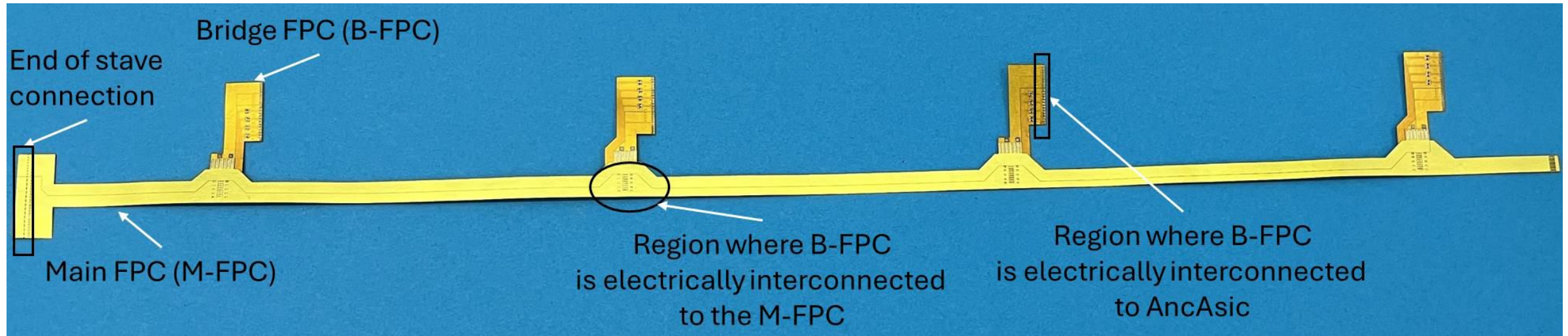
Supply	Typ (mA)	Max (mA)
PSUB (-1.2V)		
GSVDD/GSVSS (1.32V/0V)	40	60
GAVDD/GAVSS (1.32V/0V)	170	270
GDVDD/GDVSS (1.32V/0V)	526	816
TXVDD/TXSVSS (1.2V/0V)	200	300

Signal	Frequency
GCLK	80/160 MHz
SYNC	N/A
GRSTB	N/A
SRVWR/RD	5 Mbps
SCWR/RD	5 Mbps
HSDATA[0...7]	5.12/10.24 Gbps



GSVDD/GSVSS : Global Services domain (1.2V/0V), **always-on, used for on-chip services**
 GAVDD/GAVSS : Global Analog domain (1.2V/0V)
 GDVDD/GDVSS : Global Digital domain (1.2V/0V)
 TXVDD/TXVSS : Serializer domain (~~1.0V/0V~~), **1.2V/0V, only used for serializers**
 PSUB : Substrate bias (-1.2V .. 0V), **used for substrate biasing**
 Control pads : Powered by the services domain

STFC-LTU FPC Prototypes



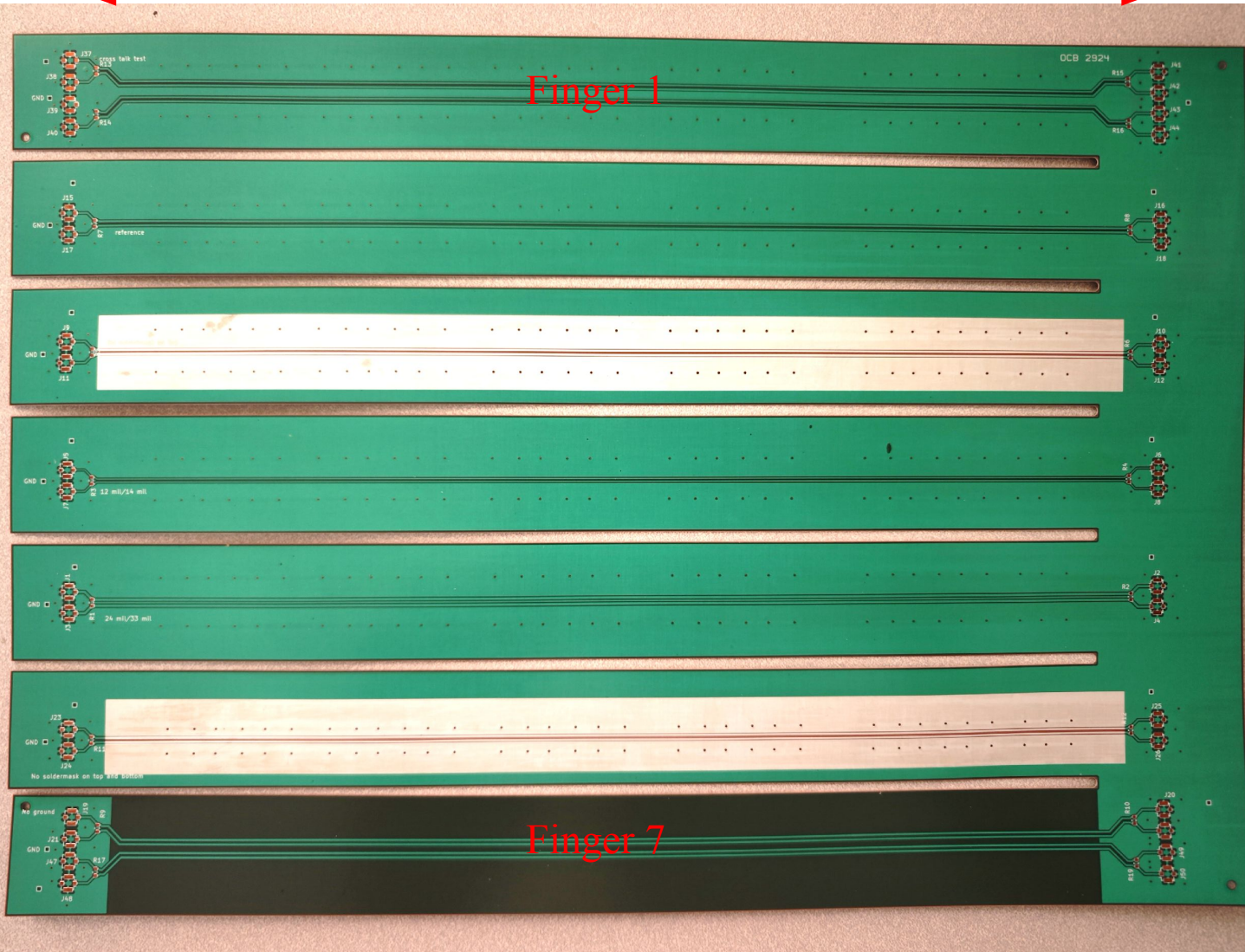
Cover layer (insulating)	Pi 12.5 (25)um	Kapton	Ni-SnBi (for soldering)
Glue ~5um			
Top Layer (signals)	Al 14um	FDI-A-24	
	Pi 10um		
Glue ~5um			
Spacer	Pi 25um	Kapton	
Glue ~5um			
Bottom (GND)	Al 14um	FDI-A-24	
	Pi 10um		

LTU FPC

Components	Thickness (um)	Material	X0(cm)	X0(%)
Metal layers	15 + 15*0.69	Aluminum	8.897	0.028
Dielectric	10+10+25+25	Polyimide	28.57	0.023
glue	15	TBC	39.07	0.004
Total				0.055

LBL-OMNI FPC Prototypes

25 cm

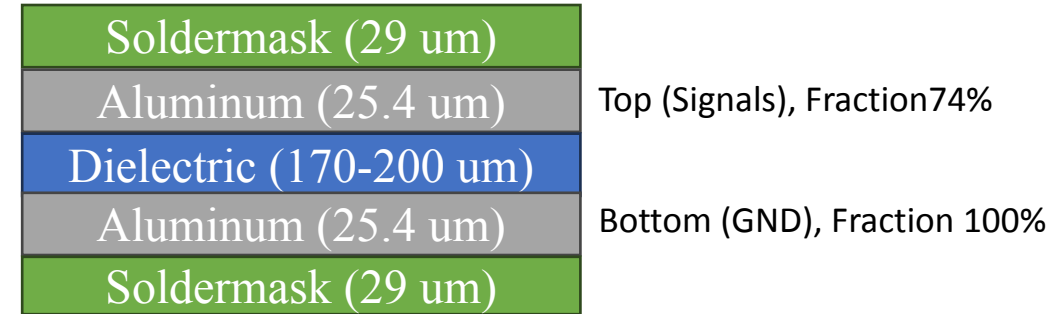


12 FPCs, 2 for each of the following:

- Different metals: Al, Cu
- Different dielectric: FR4, polyimide, EM 528K

Each FPC has 7 fingers with different layouts:

1. 2 pairs of differential lines with GND
2. 1 pair of differential line with width/space of 18mil/22mil
3. No soldermask on top
4. 12 mil/14 mil
5. 24 mil/33mil
6. No soldermask on top or bottom
7. 2 pairs of differential lines without GND on top



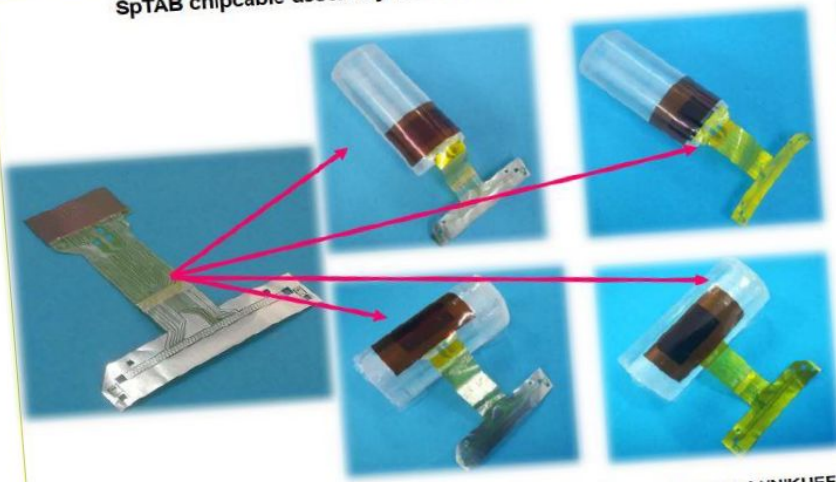
Components	LTU FPC				OMNI FPC in 2nd set			
	Thickness (um)	Material	X0(cm)	X0(%)	Thickness (um)	Material	X0(cm)	X0(%)
Metal layers	15 + 15*0.69	Aluminum	8.897	0.028	25.4+25.4*0.74	Aluminum	8.897	0.05
Dielectric	10+10+25+25	Polyimide	28.57	0.023	58 + (170~200)	Soldermask Ink + Arlon 528K	28.57	0.08~0.09
glue	15	TBC	39.07	0.004				
Total				0.055				0.13-0.14

The average material budget over the full area of a module/stave/disk may be within specs

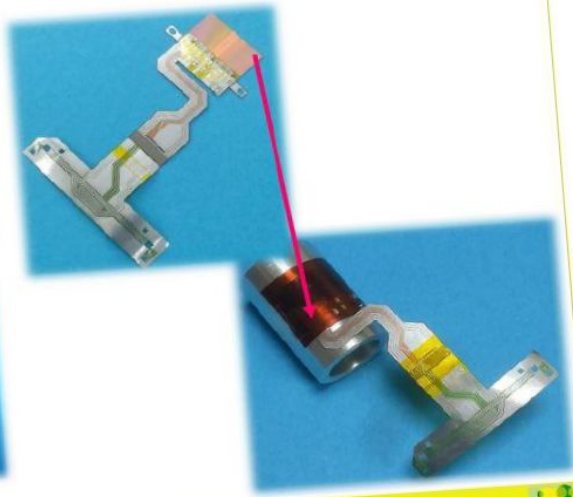
3-D (volumetric) approach realized by LTU's FPCs: ALICE ITS3 prototypes

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SpTAB chipcable assembly with ALPIDE chip



SpTAB single-ALPIDE prototype



Note: activity performed in close cooperation with CERN, Uni Bergen, Uni Utrecht/NIKHEF
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4.8.3 Fall-back options

Sp-TAB technique

The Single-point Tape Automated Bonding (SpTAB) technique has been considered as an alternative option to interconnect the ITS3. The main features of this technique and approach are:

- adhesiveless aluminum-polyimide thin single-layered and multi-layered flexible printed circuits to interconnect the chip to the external data and power transmission buses;
- conductive aluminum layer thicknesses ranging from 15 to 100 μm to realize low-mass interconnection elements;
- SpTAB direct connections of ribbon aluminium leads to chip pads providing uniform, highly reliable and mechanically stable monometallic joints;
- welded joint encapsulation after SpTAB;
- possibility to perform quick repair weld joints during manufacture of the pixel module;
- possibility of using standard industrial automated equipment for basic assembly processes (welding, gluing and encapsulating welded joints).

The SpTAB technique allows interconnection of the curved chip to the flexible circuit as well as for bending the pre-interconnected assembly. Using thin single layered circuits for sensor-to-bus interconnections allows electrical functional testing to be performed before final mounting on support structures or further assembly. The approach described has been used to create and characterise single-chip test assemblies using ALPIDE chips (see Fig. 4.59). In order to

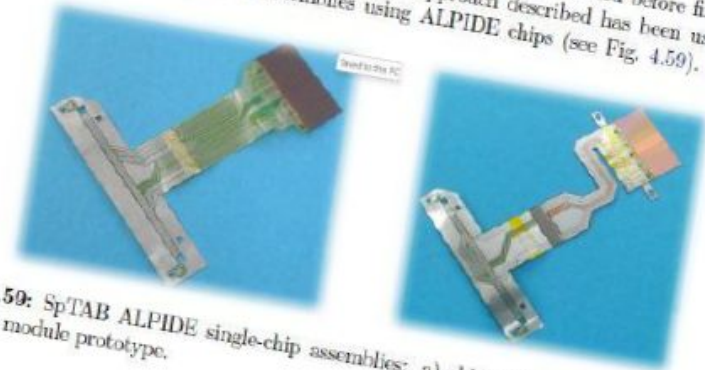
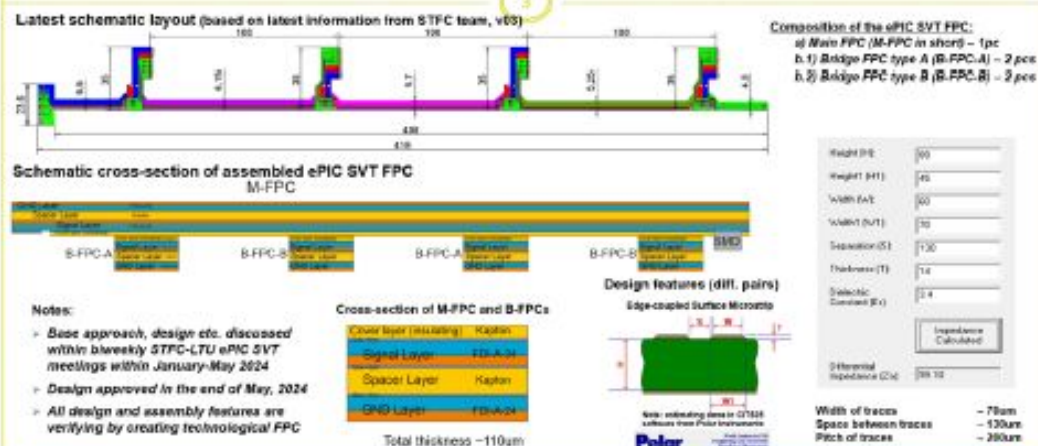


Figure 4.59: SpTAB ALPIDE single-chip assemblies: a) chip cable with chip assembly; b) single-chip module prototype.

Base approach and features (reminder)

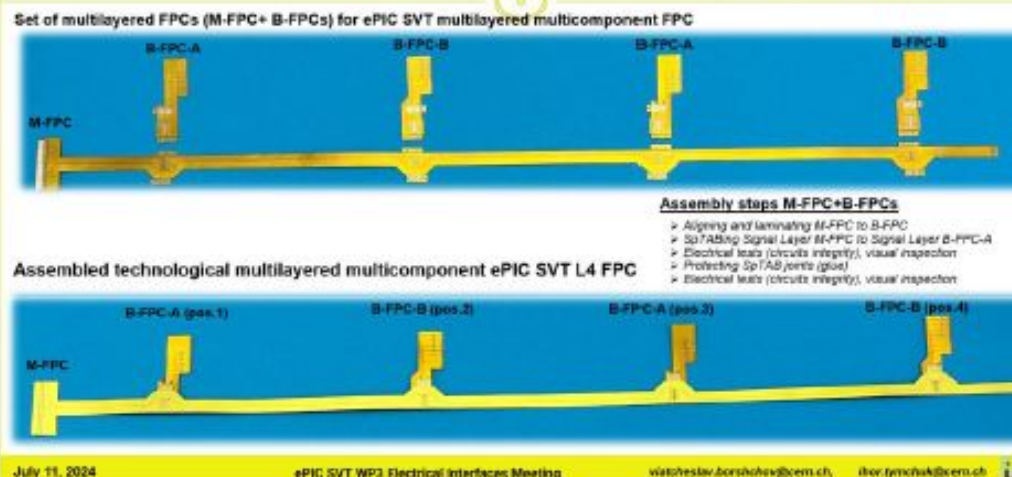
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Base layout and cross-section

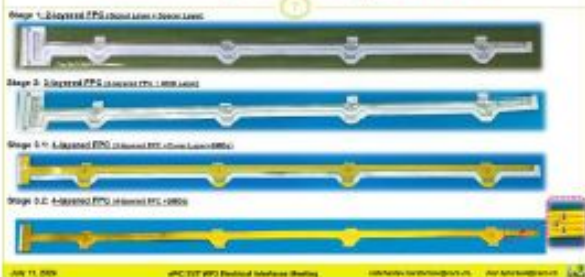


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Technological ePIC SVT L4 FPCs



Assembling technological M-FPC



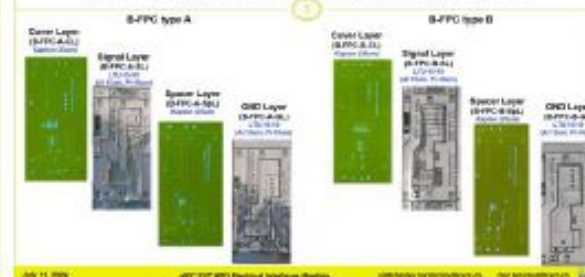
Assembling technological B-FPCs



Technological M-FPC: flexible layers



Technological B-FPCs: flexible layers



Pros:

- OMNI can add small pieces of copper at the soldering positions on the FPC, making soldering possible;
- OMNI supports vias between different layers of the FPC
- 10.24Gbps IBERT test results from prototype produced by OMNI at a length of 25 cm are promising;

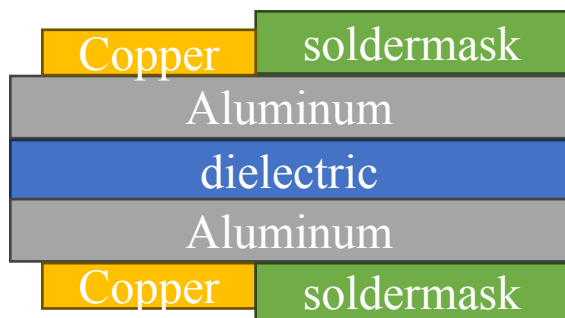
Cons:

- Dielectric (Al) thickness is around 230-260 (25.4) μm , in comparison to LTU's 70 (15) μm , leading to 0.13~0.14% X_0 compared to LTU 0.055% X_0 ;
- The minimum trace width and space are 152.4/152.4 μm , which are larger than LTU's (70 μm /130 μm);
- The prototypes received so far are not very flexible, and may break when bent to a radius of 4 mm.
- Can't do spTAB

Material Budget

Table : Structure of EM 528K Al-FPC

Layer	Material	Thickness [um]	X0 [cm]	Fraction	X0(%)
Soldermask	Not sure	29.2	28.57 (TBC)	0.995	0.0102
Copper	Copper	29.2	1.436	0.005	0.0010
Aluminum	Aluminum	25.4	8.897	0.97	0.0277
Dielectric	EM 528K	175.3	28.57 (TBC)	1	0.0613
Aluminum	Aluminum	25.4	8.897	0.97	0.0277
Copper	Copper	29.2	1.436	0.005	0.0010
soldermask	Not Sure	29.2	28.57 (TBC)	0.995	0.0102
					0.1392



The parameters of soldermask and EM 528K are considered as Isola.

The estimated material budget of EM528K,FR4 and Isola are 0.1392%, 0.1876% and 0.1574%, respectively.