Eic Main + Bridge FPC Prototype

Signal Integrity tests on prototype main+bridge FPC compared to main FPC only.

W.Helsby

Update 1/04/2026

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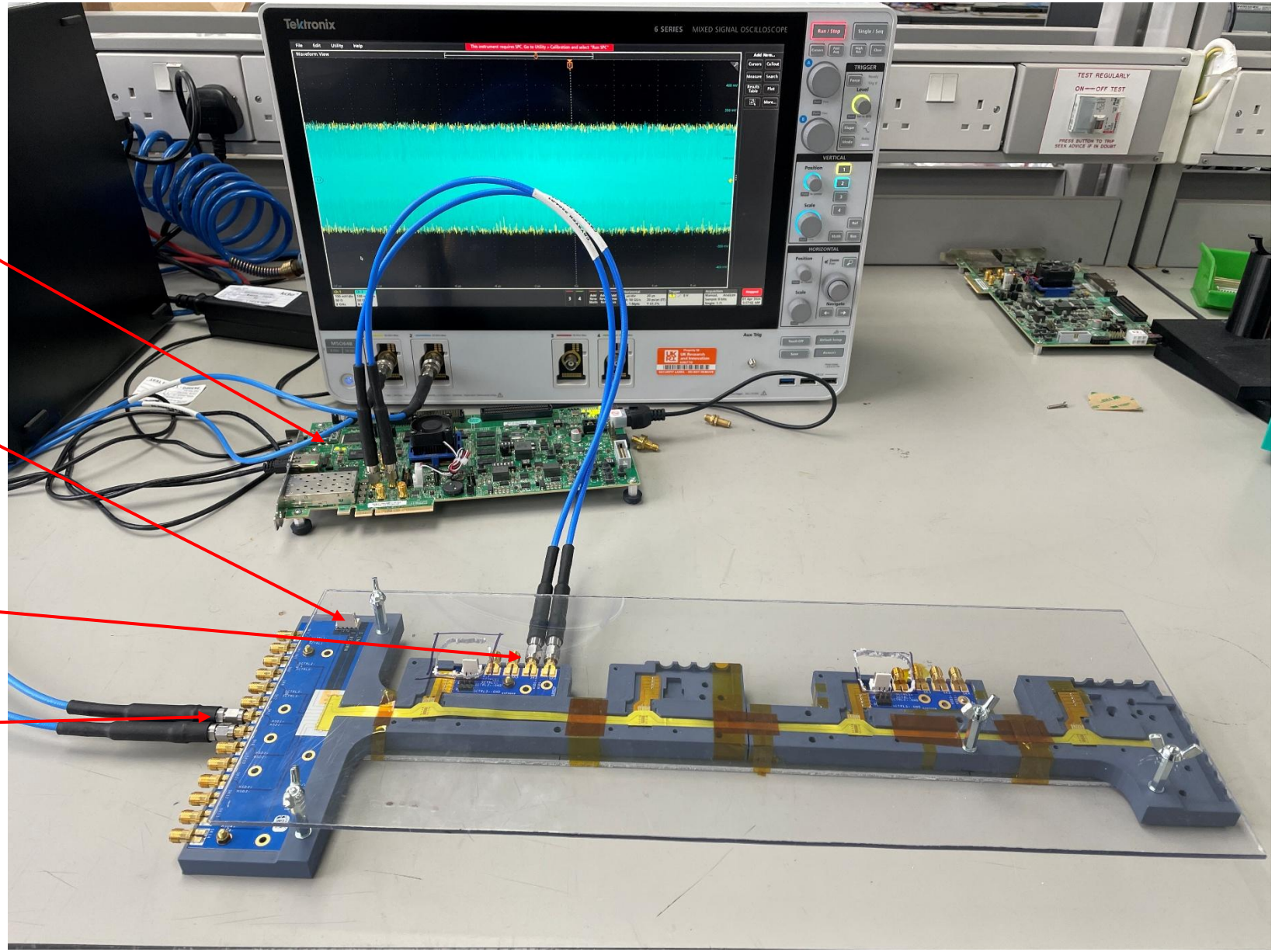
Main FPC connected to KCU105 and Tektronix MSO6B ’scope

KCU105 AMD Kintex Ultrascale+ FPGA board

Main+Bridge FPC with test boards left and at bridge positions 1 and 3

Signal input from bridge1. HSD1

Signal output from LHS test board.



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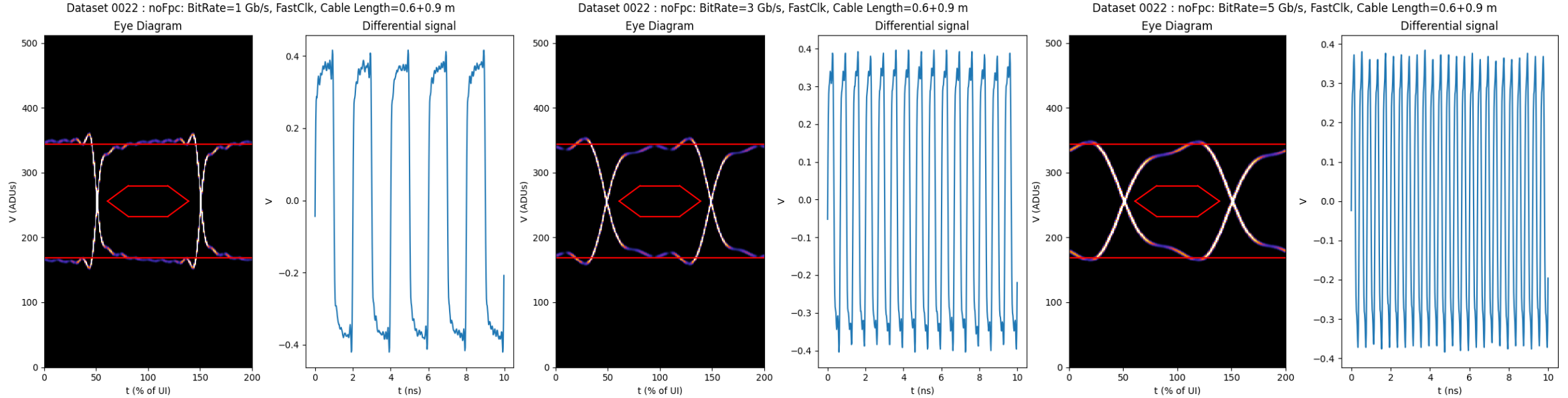
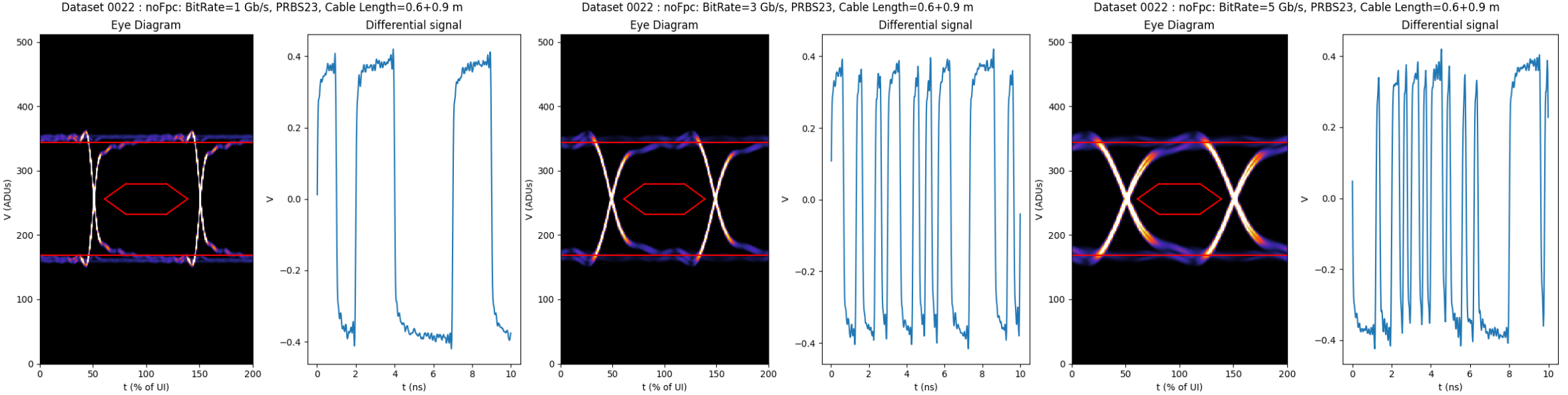
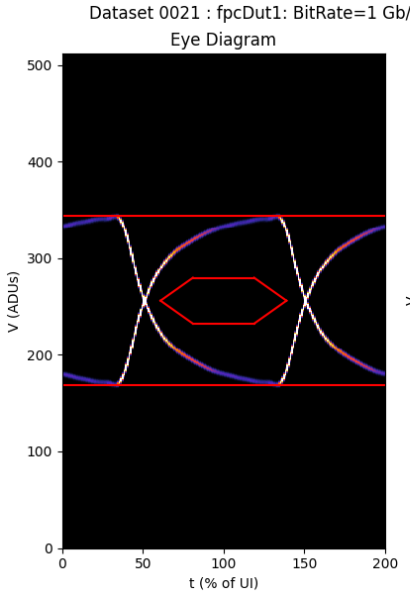
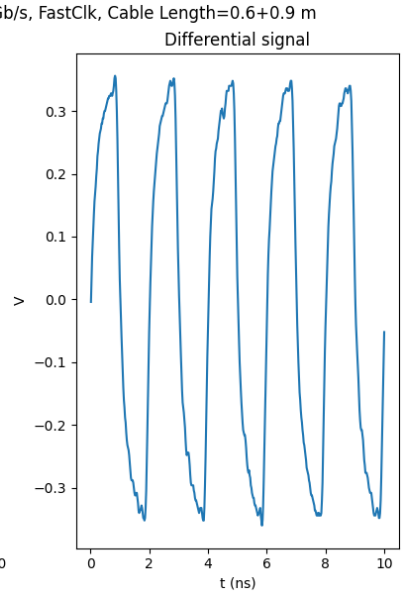
Test rig (KCU105, cables and 8 GHz ‘scope) without FPC.

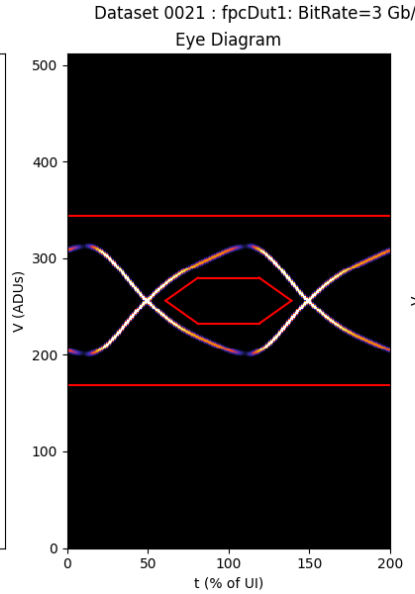


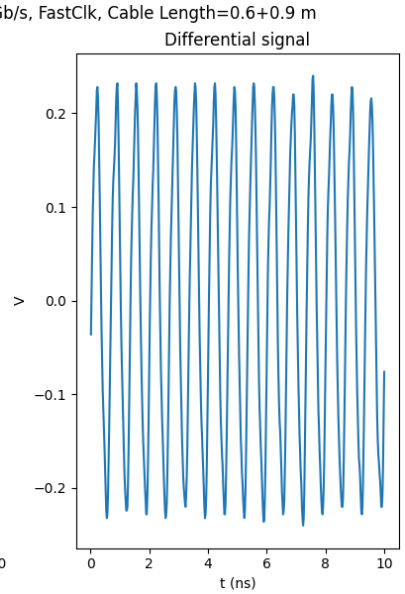


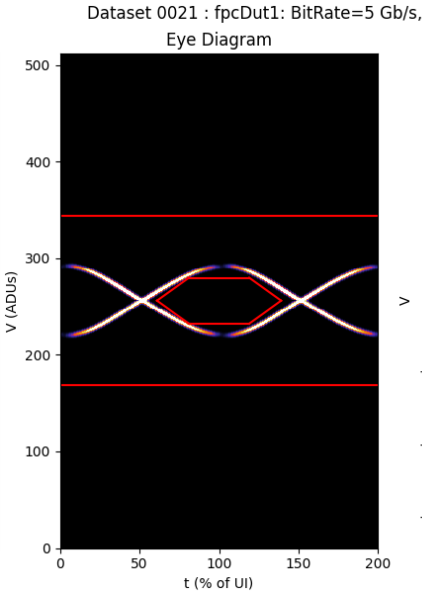
Signal transmitted via main FPC SCTRL2. (8 GHz scope)

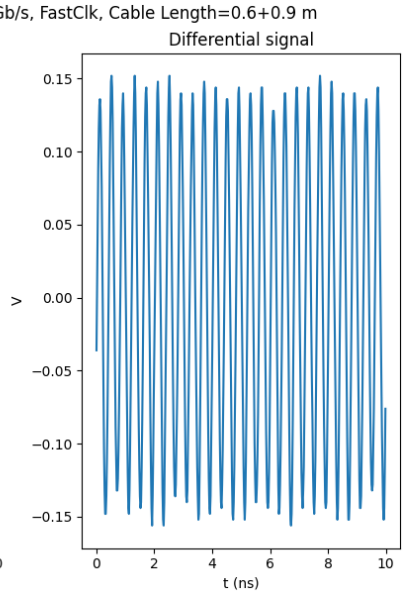


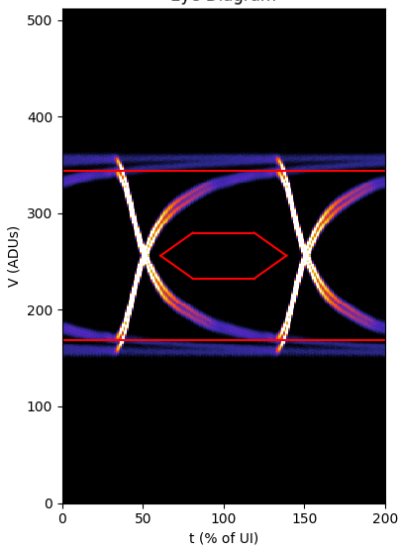


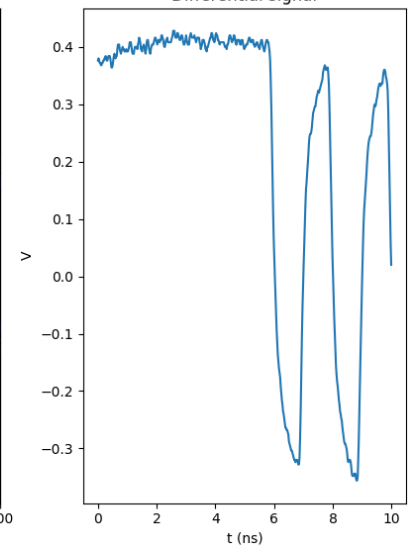


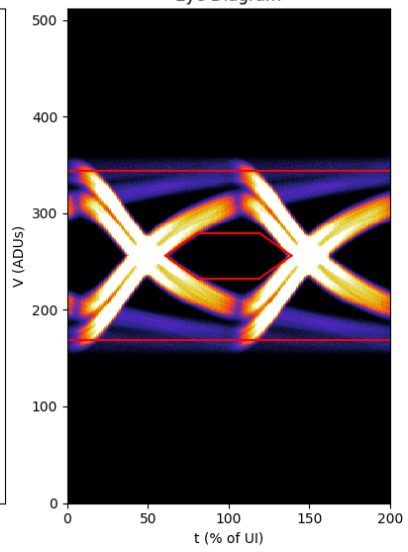


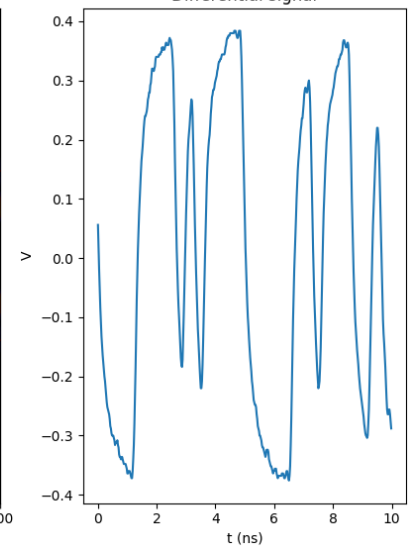


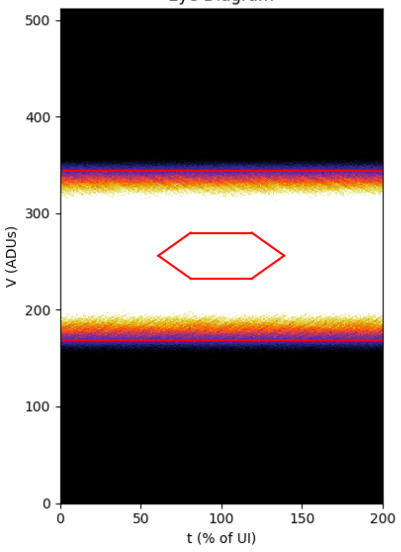


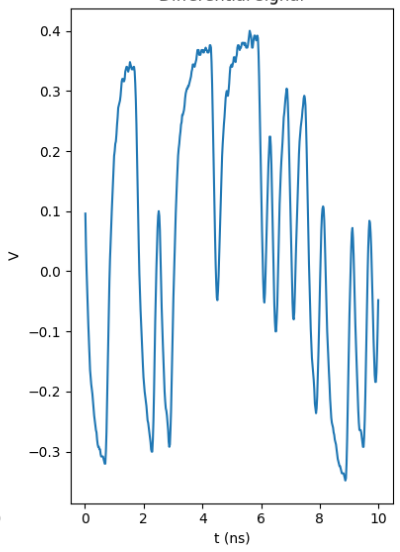




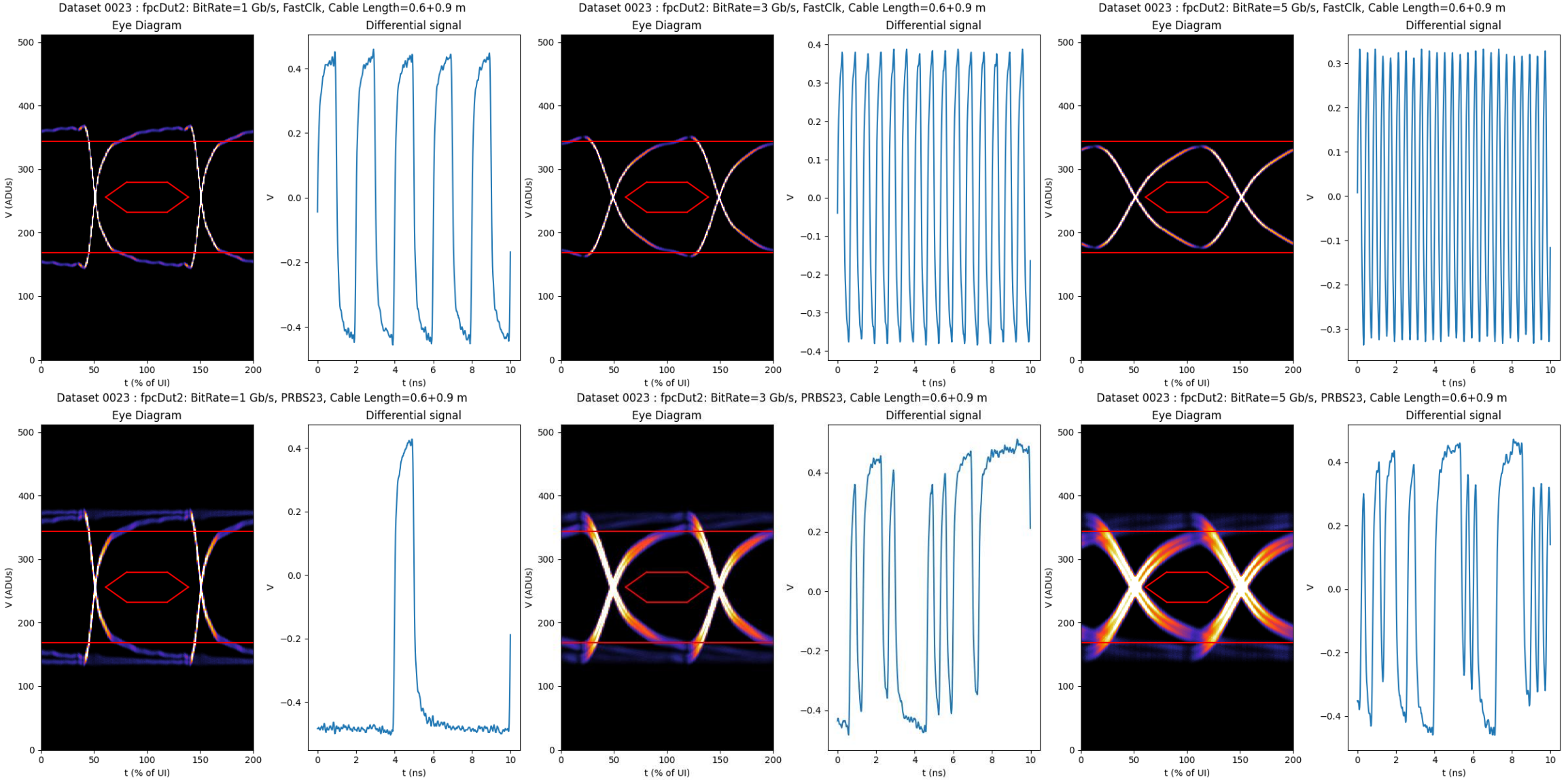




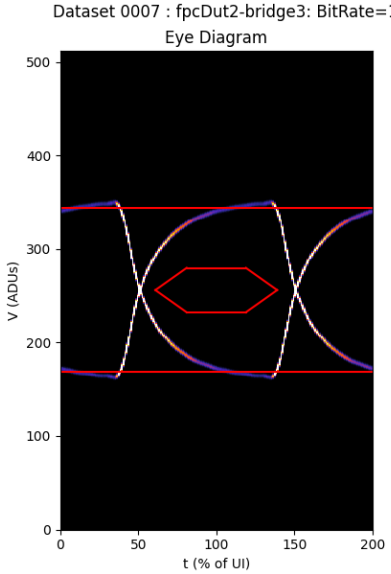


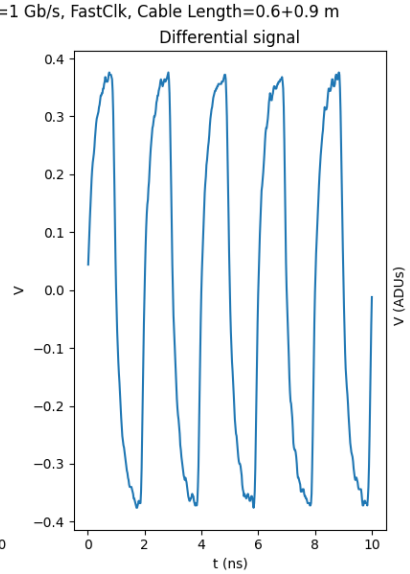


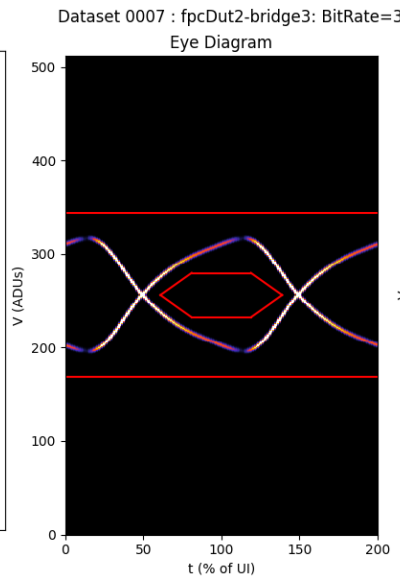
Signal transmitted via from bridge 1 through main fpc

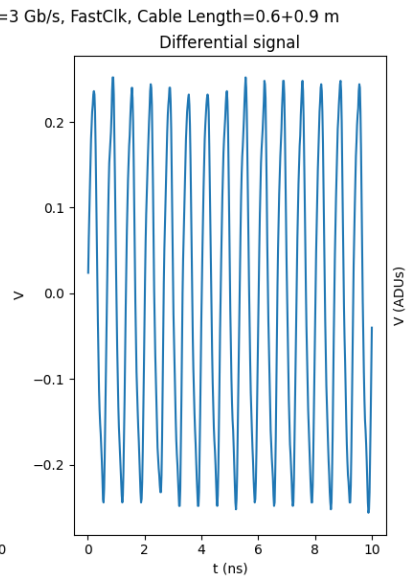


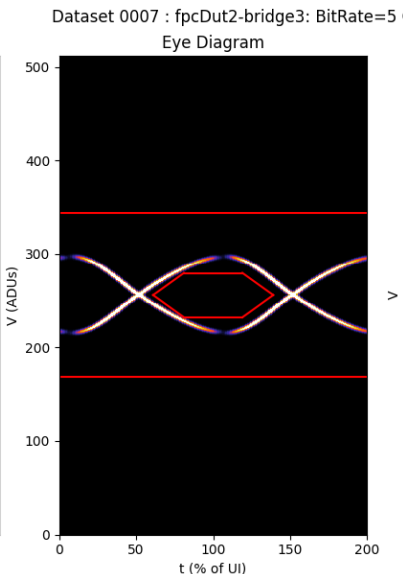
Signal transmitted via from bridge 3 through main fpc

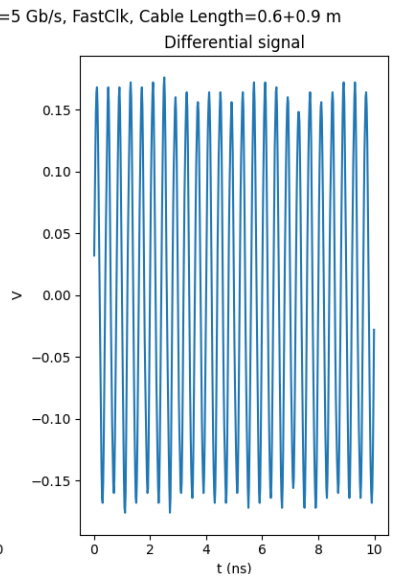


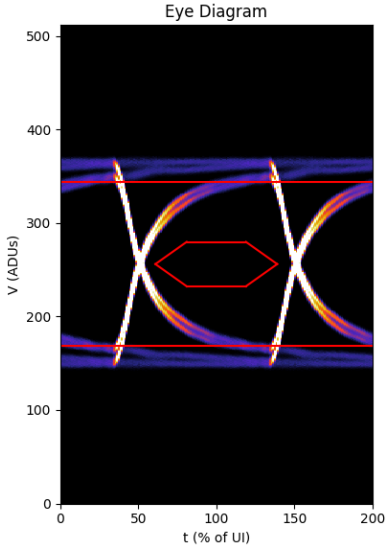


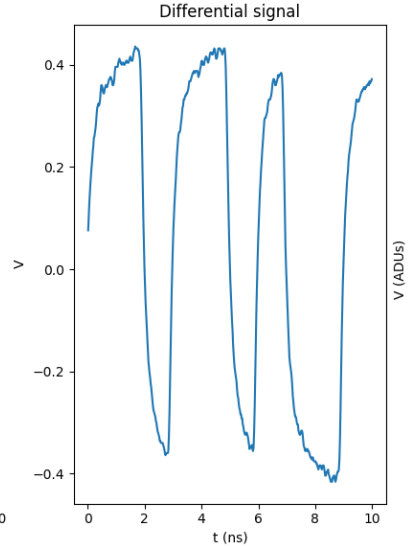


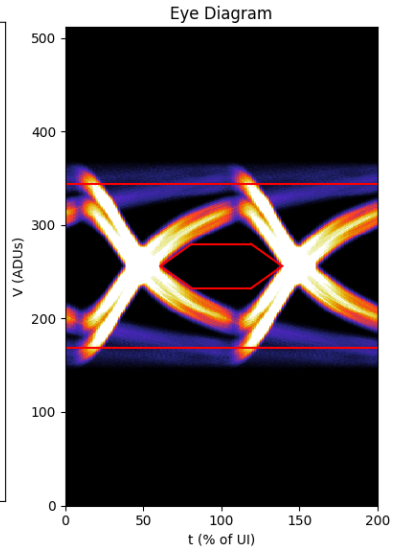


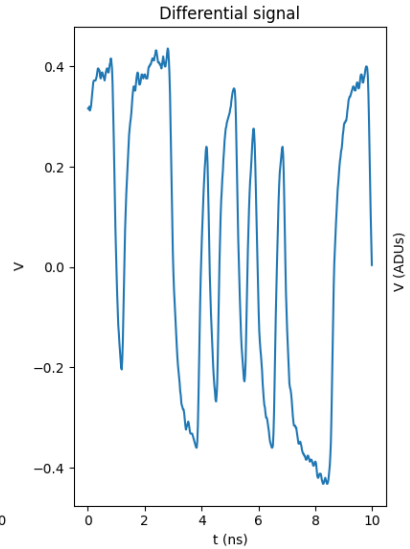


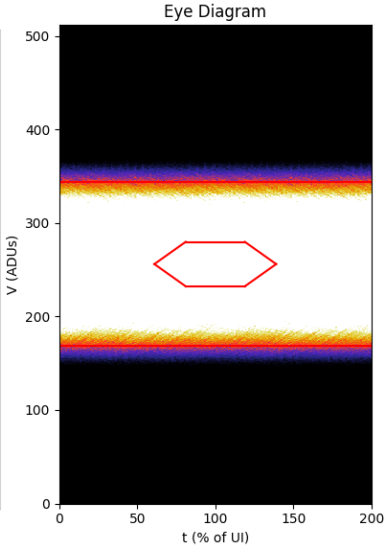


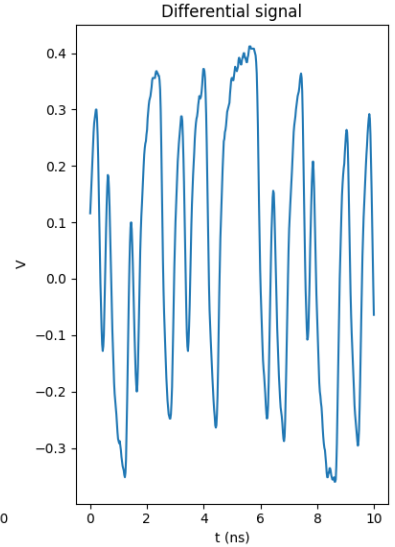




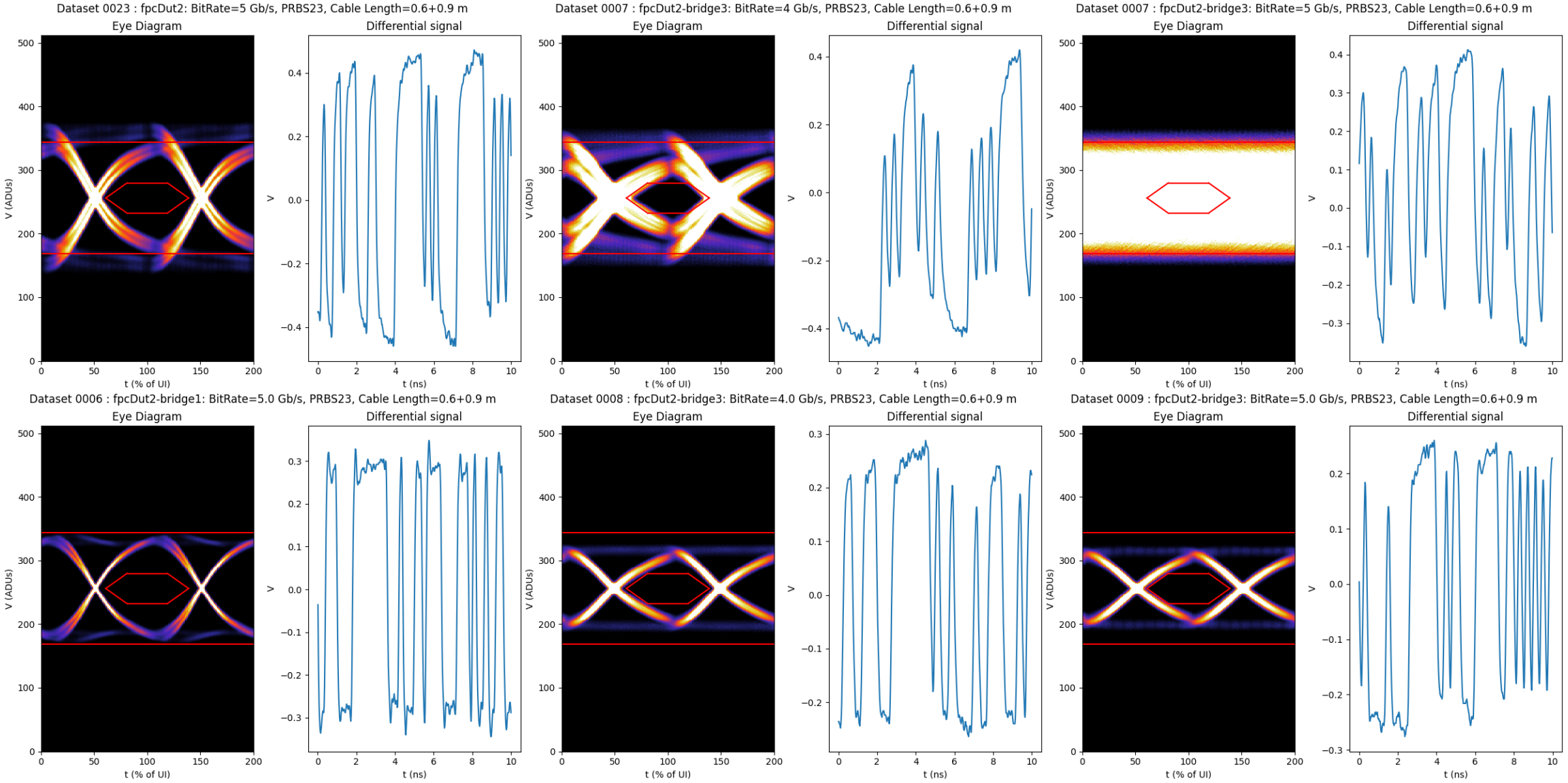




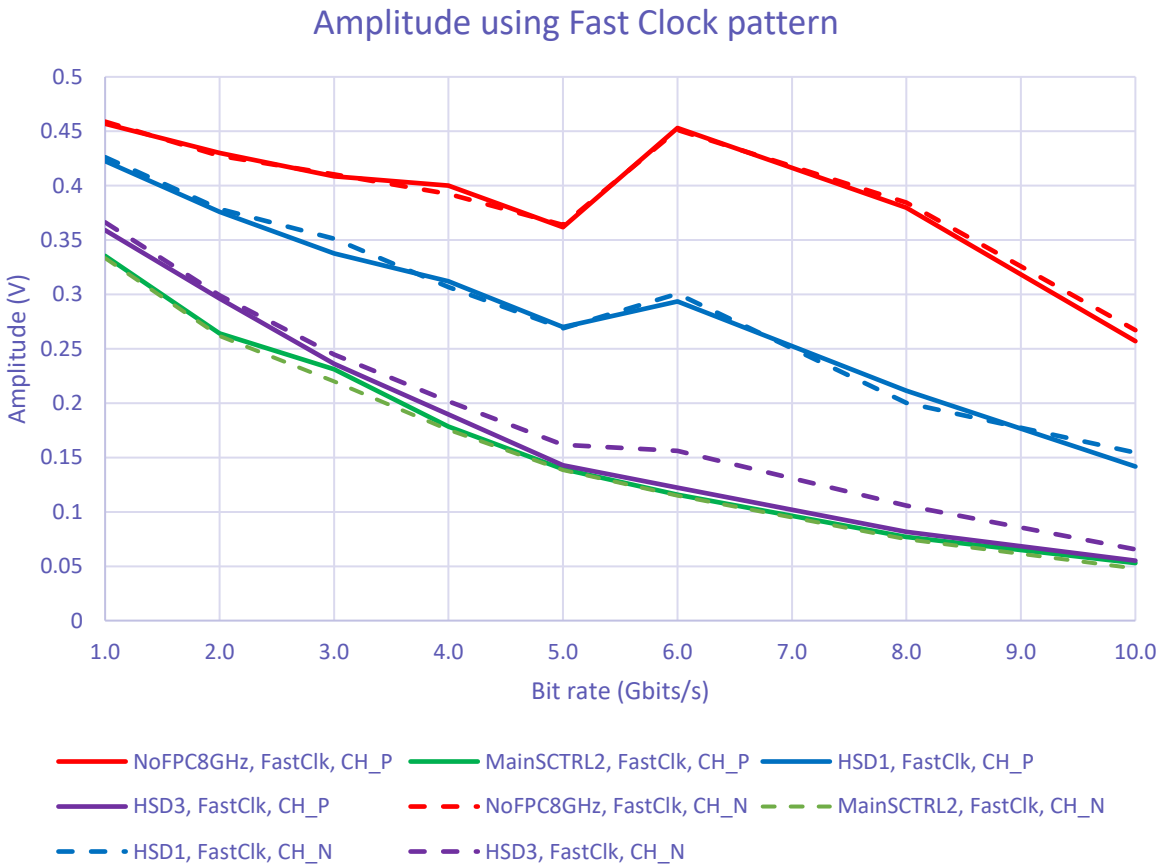


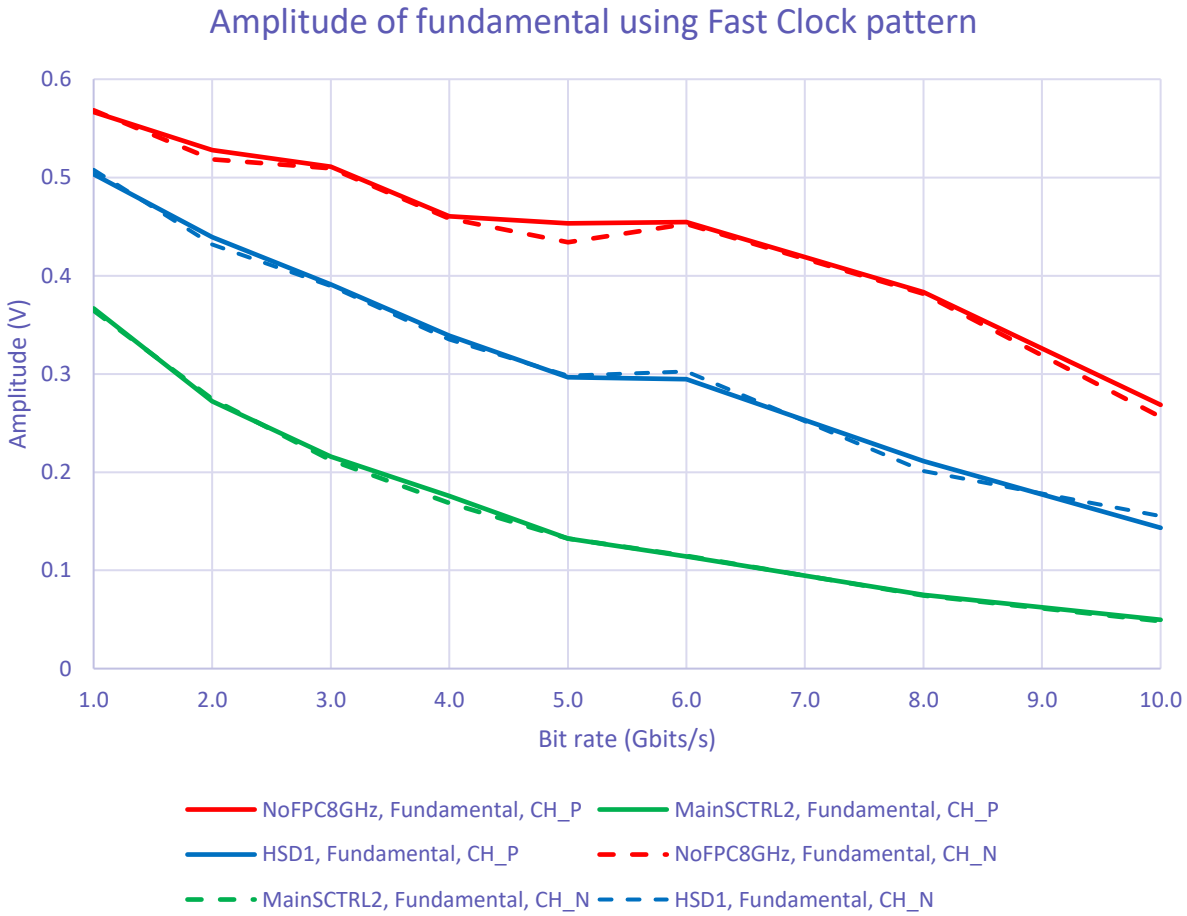


Using Post Cursor corrections.



Amplitudes using Fast Clk, full bandwidth and fundamental





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Transmission of the fast clock fundamental frequency.

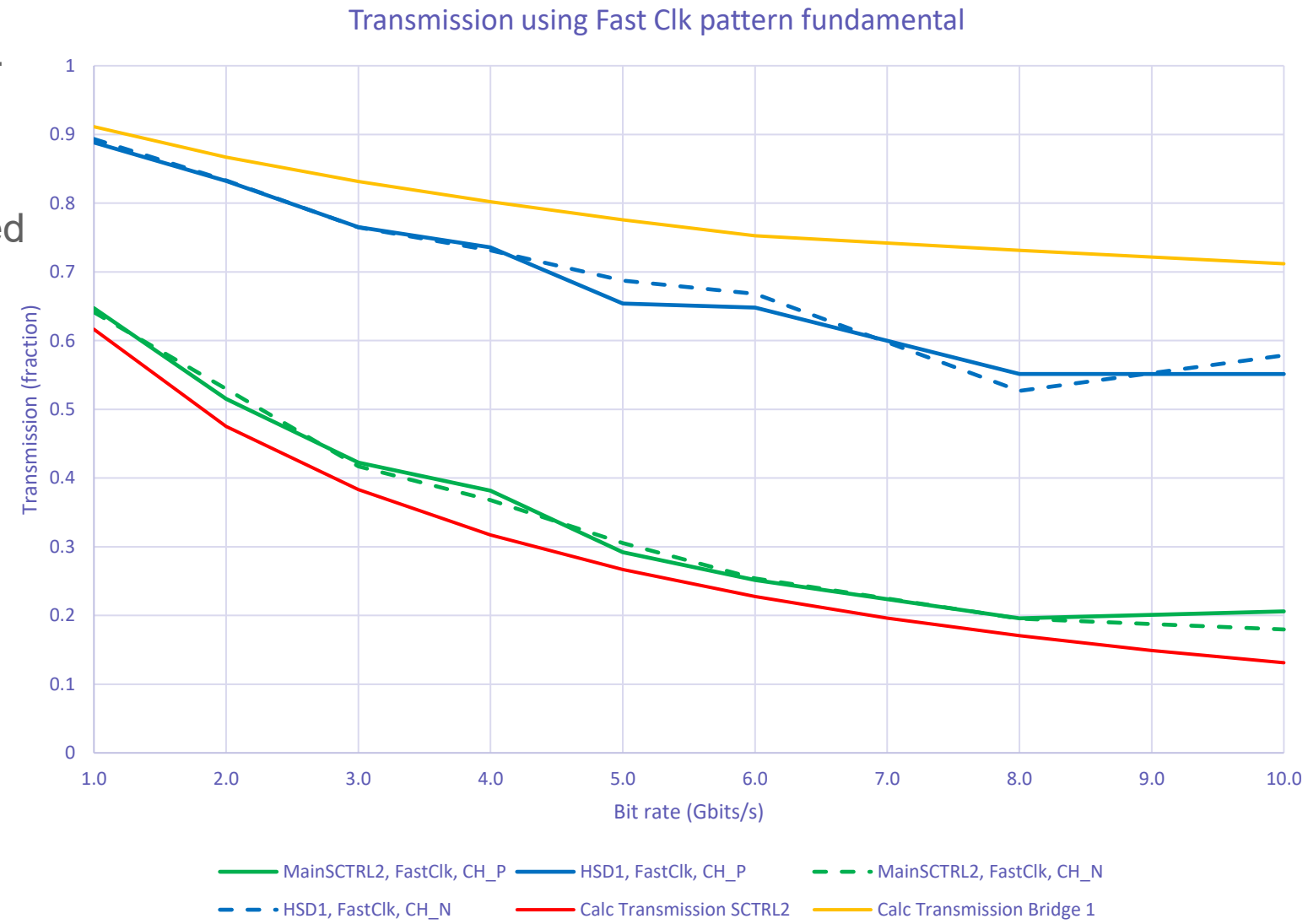
Adjusted for DC coupling without FPC.

For SCTRL2: DC transmission 100/(100+2*13)=0.8

Attempt at calculating loss shown in red and orange

SCTRL2 matches calculation.

HDS1 (first bridge) has higher transmission but does not match calculations.



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Eye mask specification

From: **Versatile Link+ Technical Specification, part 2.1**
EDMS Document Number: **1719329**

Table 6: VTRx+ Eye Mask Parameters.

#	Specification	X1	X2	X3	Y1	Y2	Y3
4.1.7	Tx Output Eye Mask Unit (UI = 97.66 ps)	22.5 ps	33.2 ps	42 ps	0.27 Norm. Amp.	0.35 Norm. Amp.	0.40 Norm. Amp.
4.2.5	Tx Input Eye Mask Unit (UI = 97.66 ps)	10.7 ps	30.3 ps		95 mV	350 mV	
4.4.5	Rx Output Eye Mask Unit (UI = 390.6 ps)	28.3 ps	48.8 ps		95 mV	350 mV	

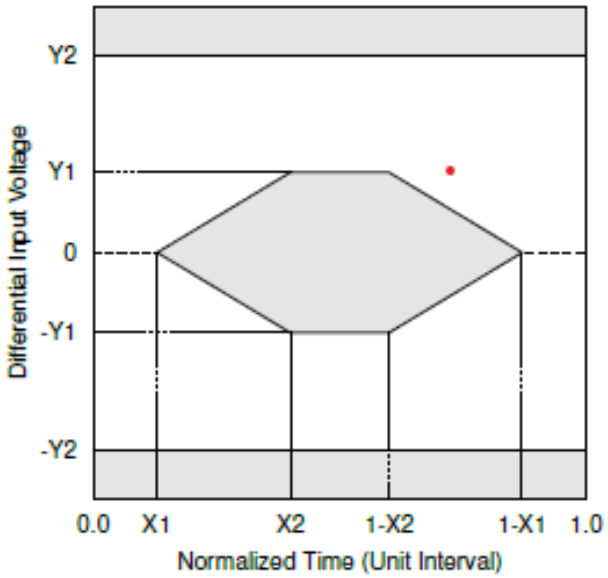

Figure 6: Electrical Eye Mask for 4.2.5 Tx Input & 4.4.5 Rx Output

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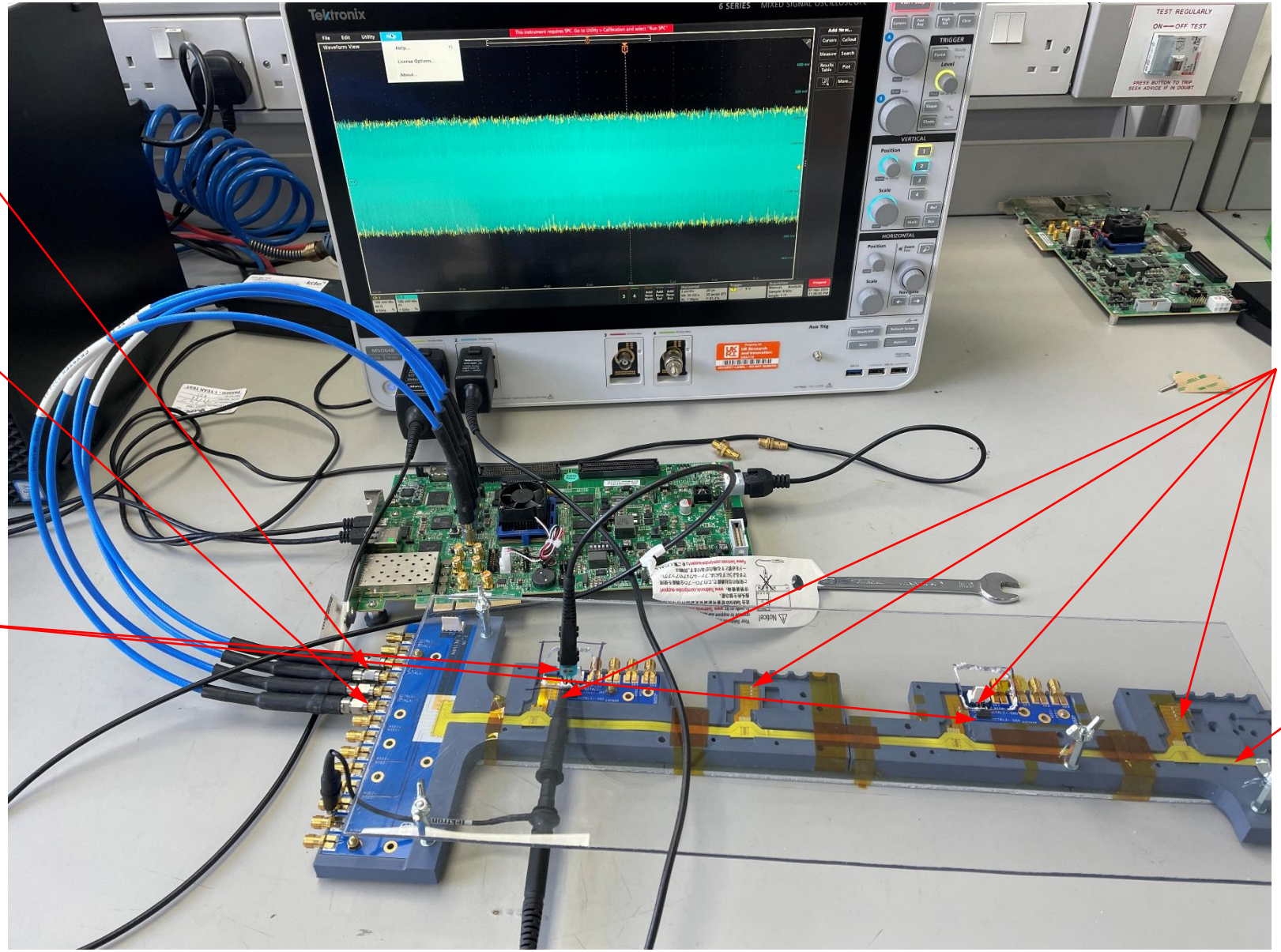
Bussed slow control signals – Clock and TX

SCTRL2 driven by USER CLK output of KCU105, 100R termination Differential SSTL18 drivers

SCTRL3 driven by USER GPIO output of KCU105. No termination at FPGA

Firmware can swap clk and data pattern.

SCTRL2 measured via 4 GHz active differential probe at bridge 1 or 3



All 4 bridge FPCS are present giving stubs.

100 R termination at far end.

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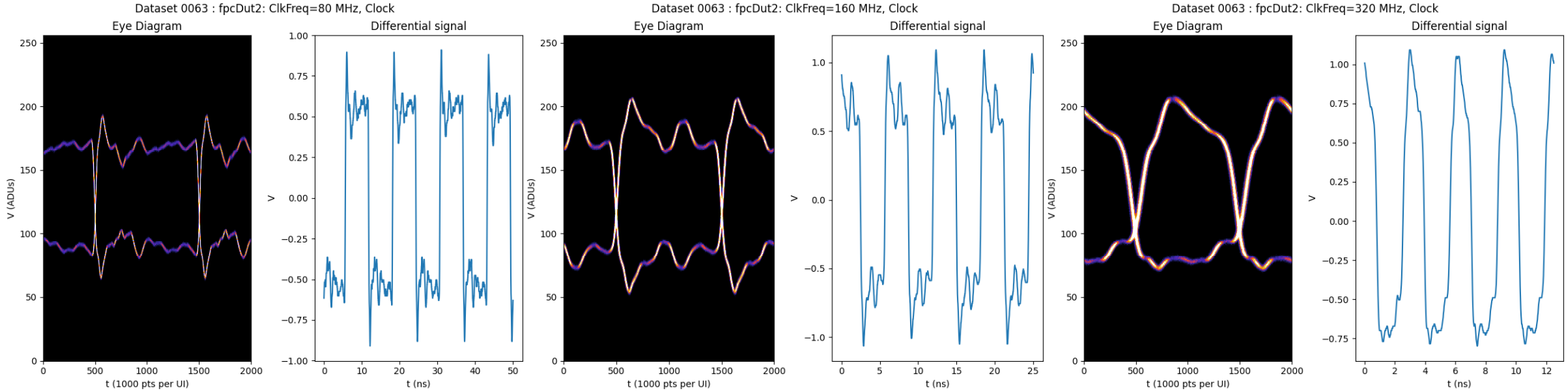
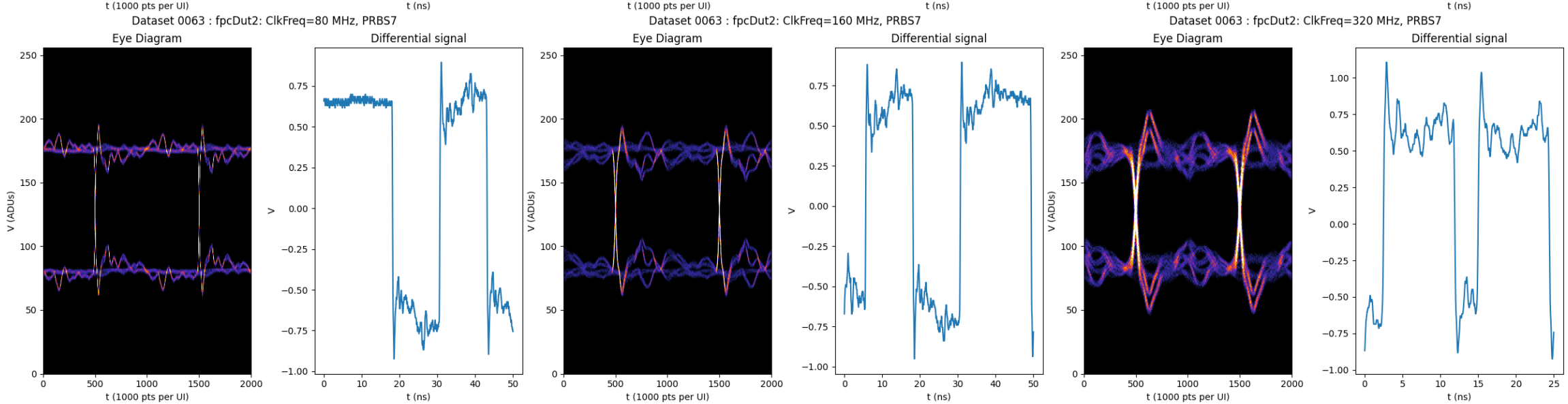
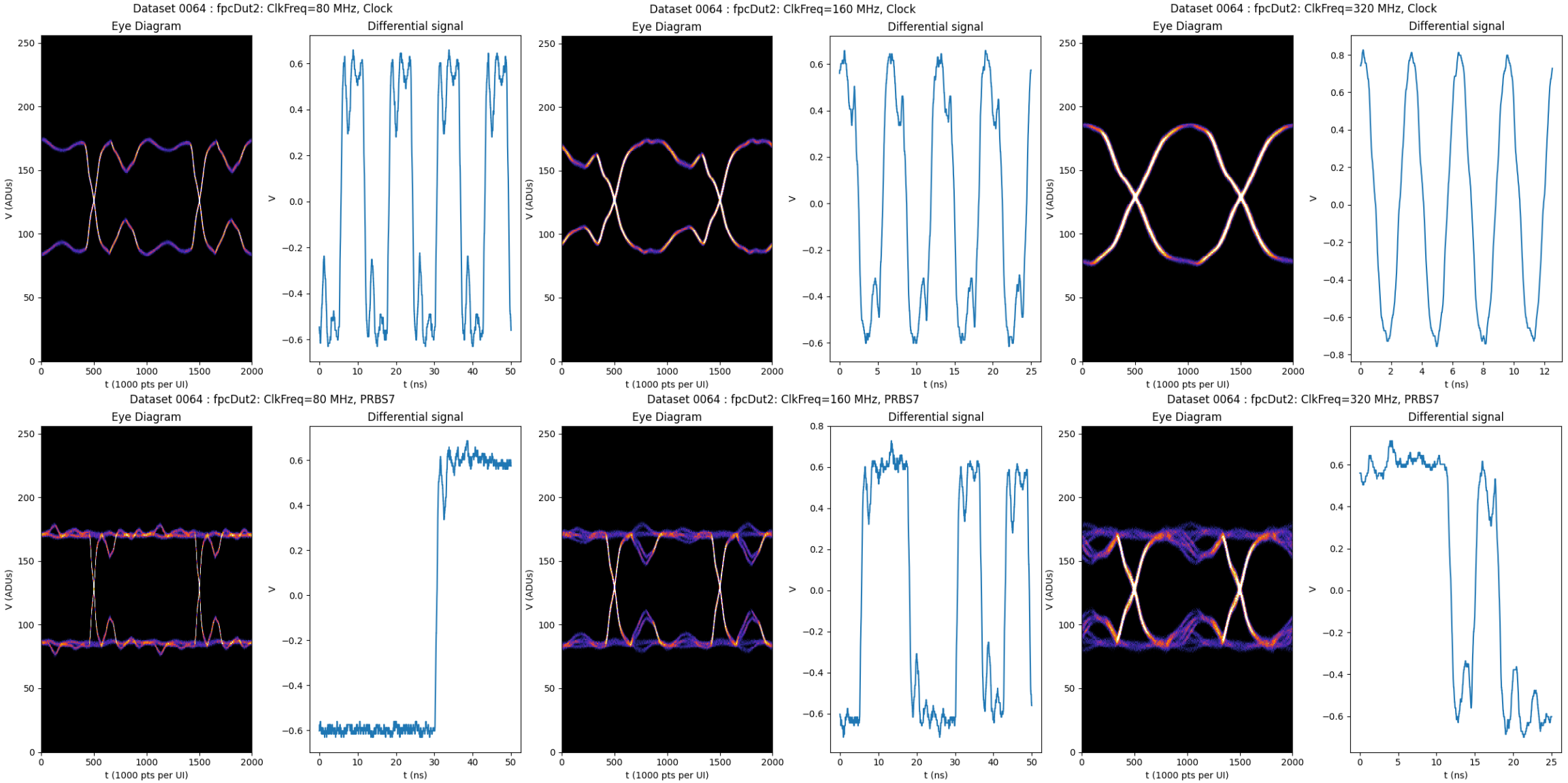
SCTRL2 to Bridge 1

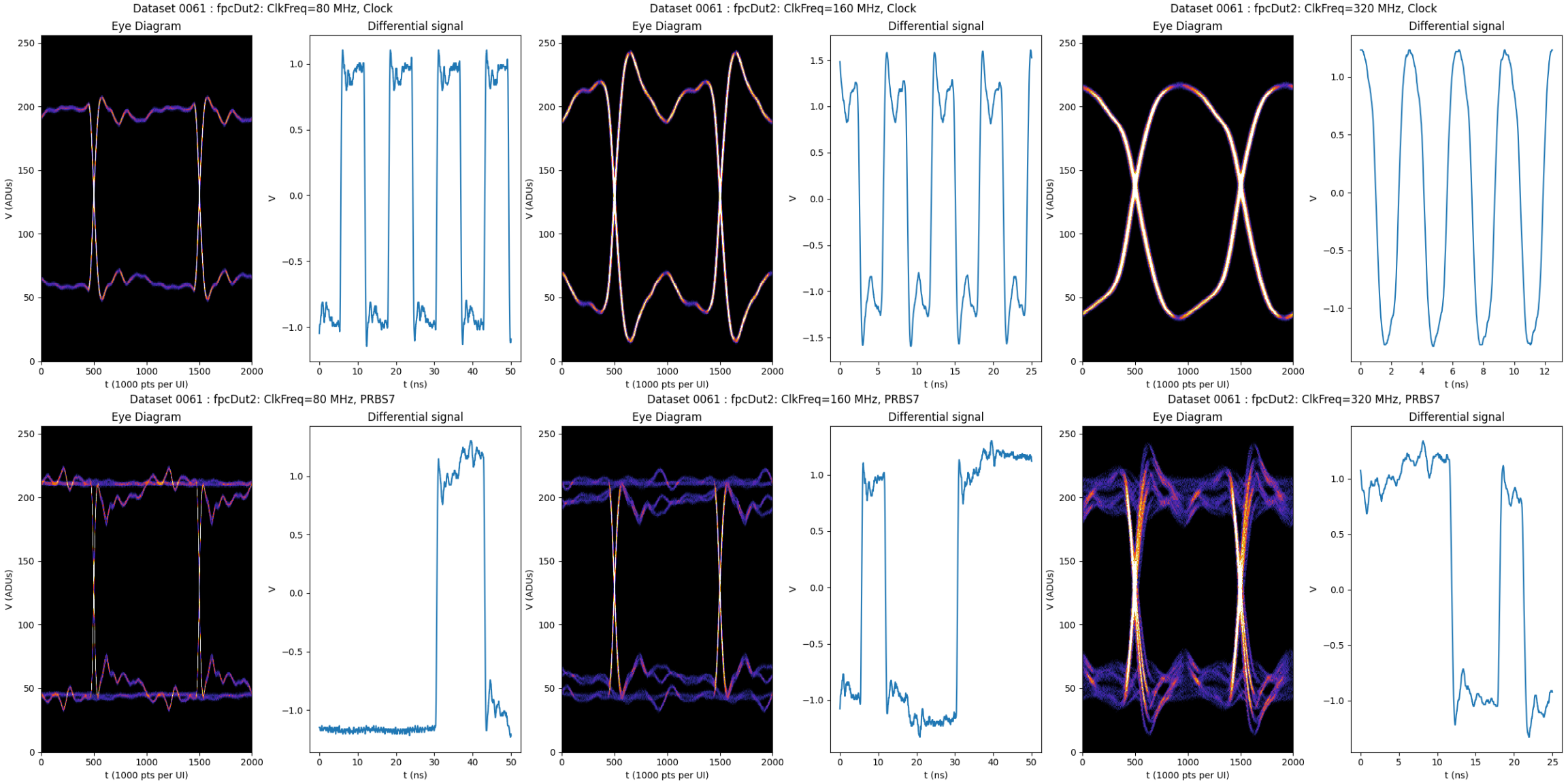




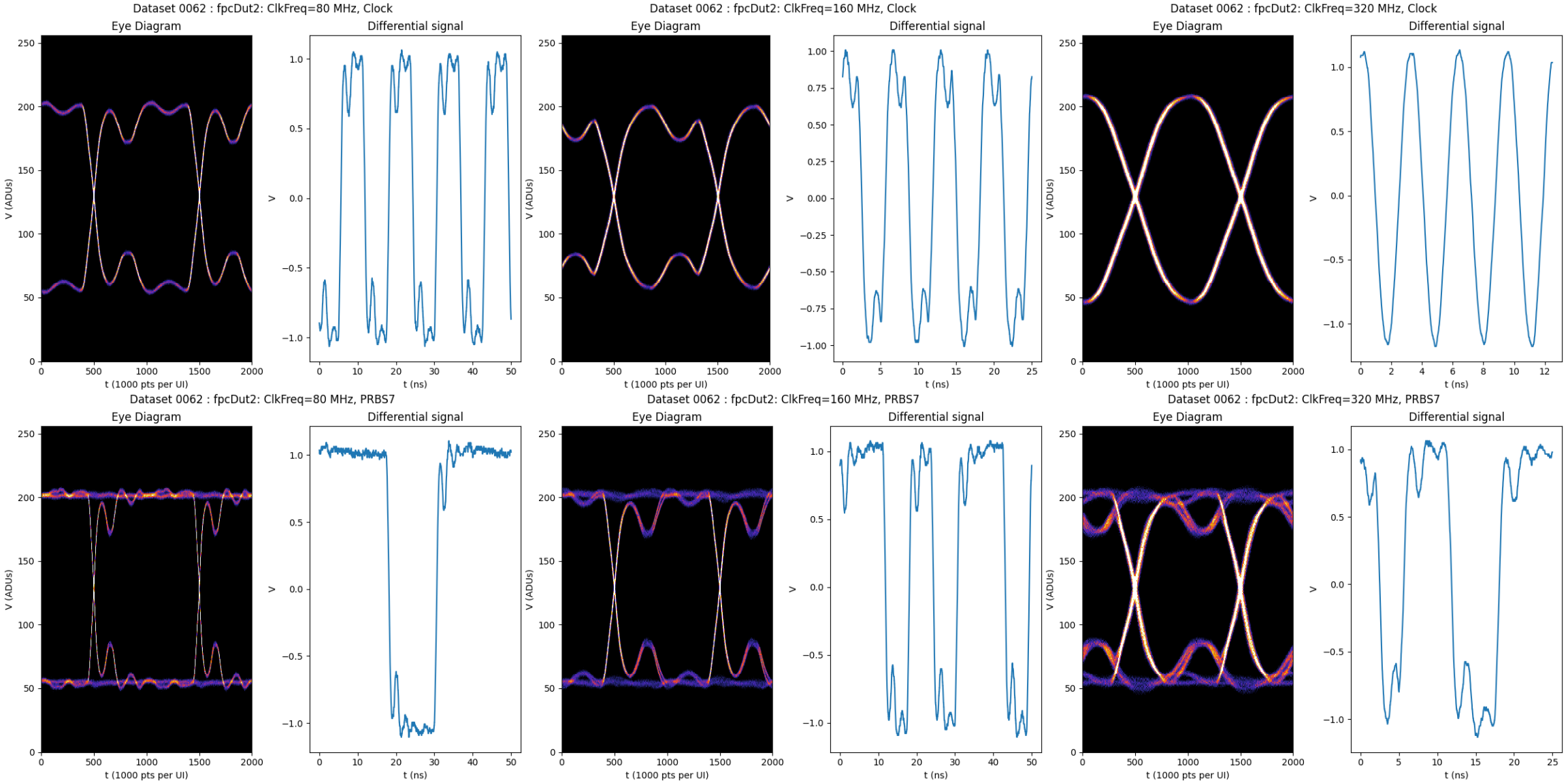
SCTRL2 to Bridge 3



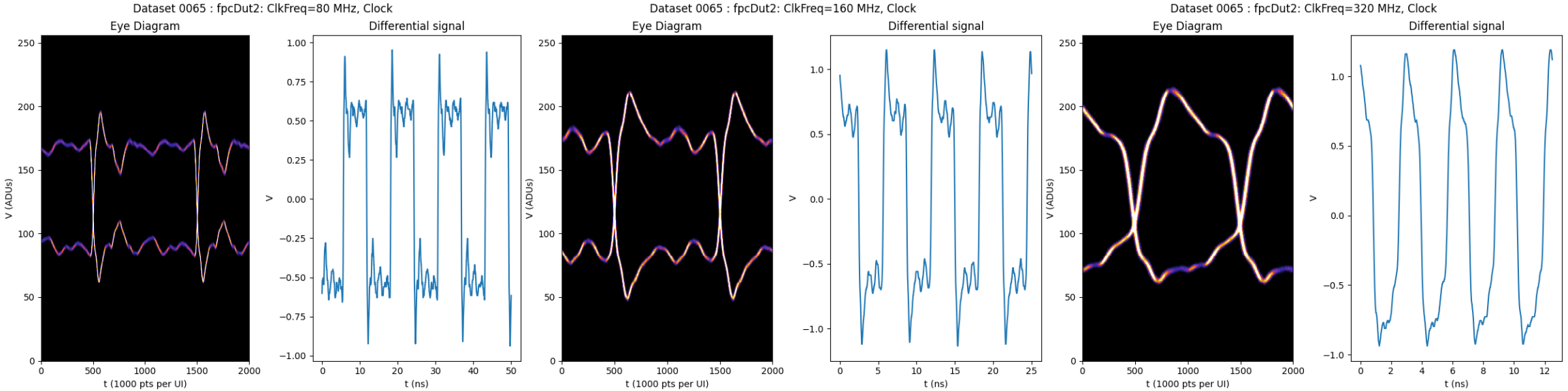
SCTRL3 to Bridge 1

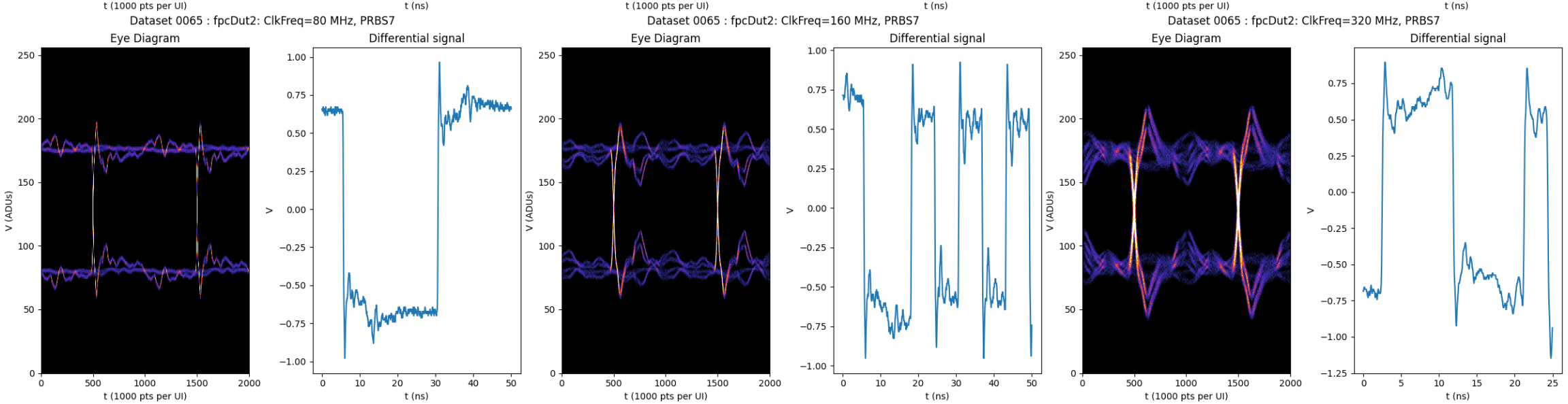


SCTRL3 to Bridge 3

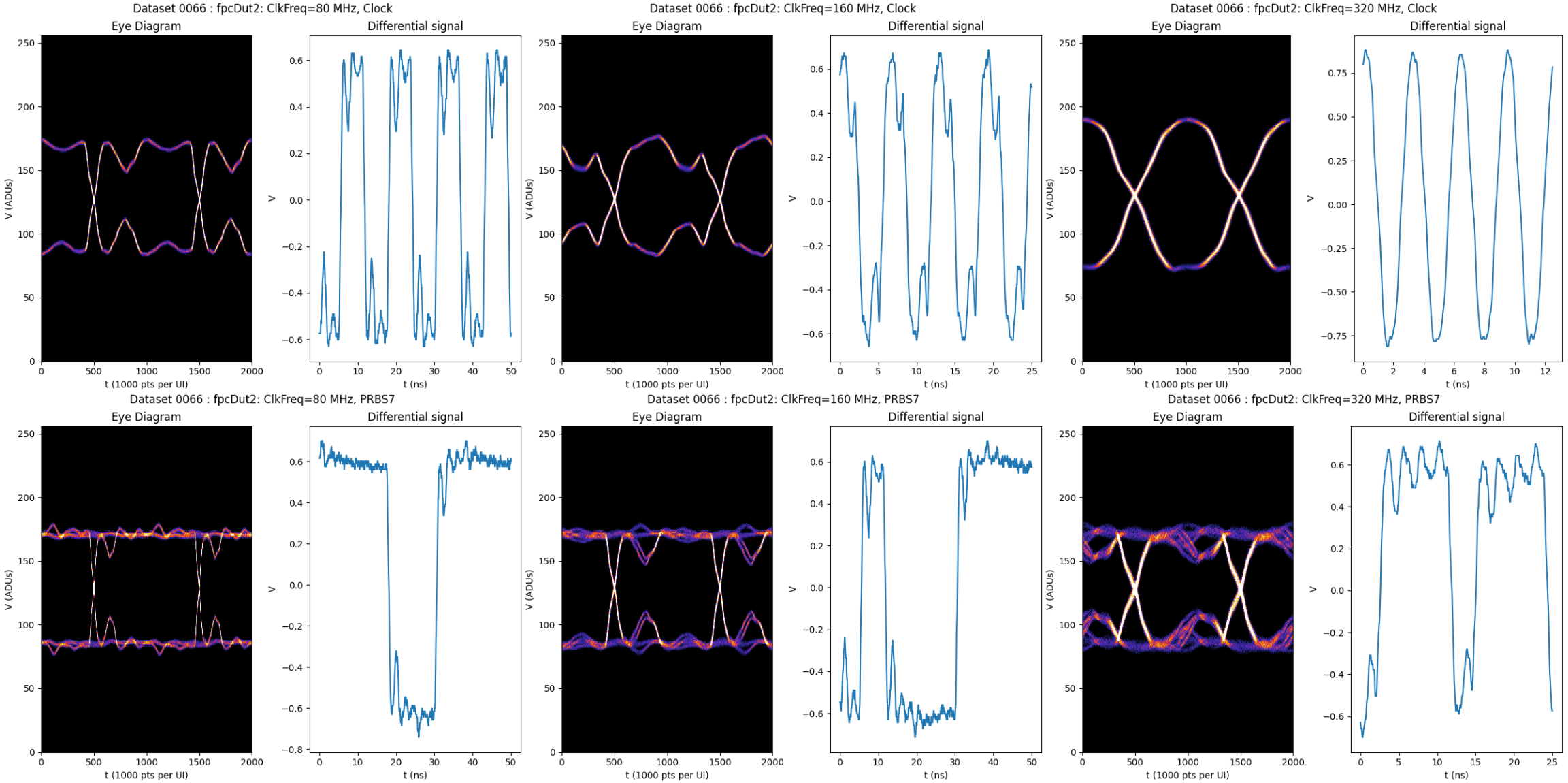


SCTRL3 to Bridge 1, but driven by USER_SMA_CLOCK

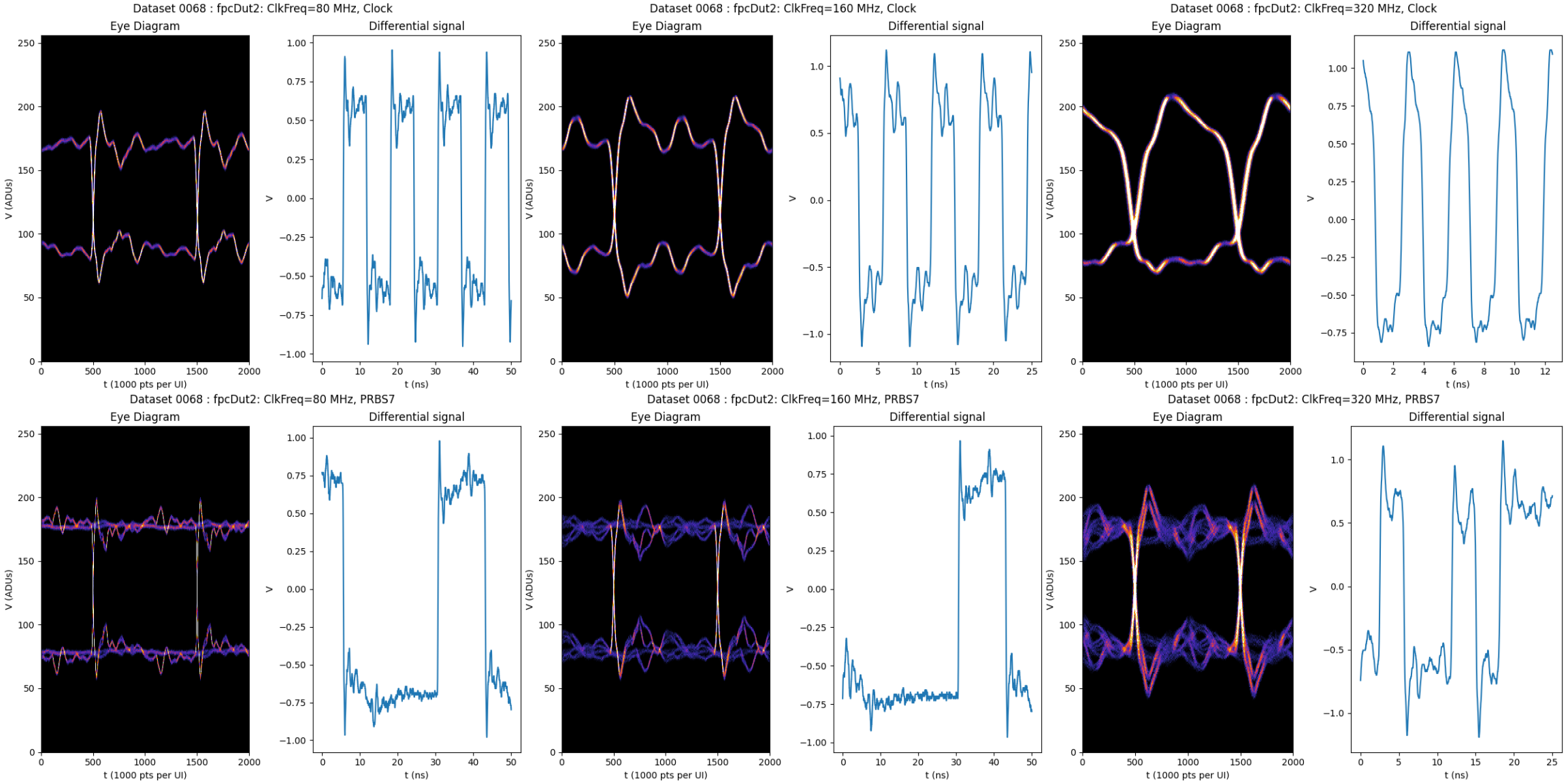




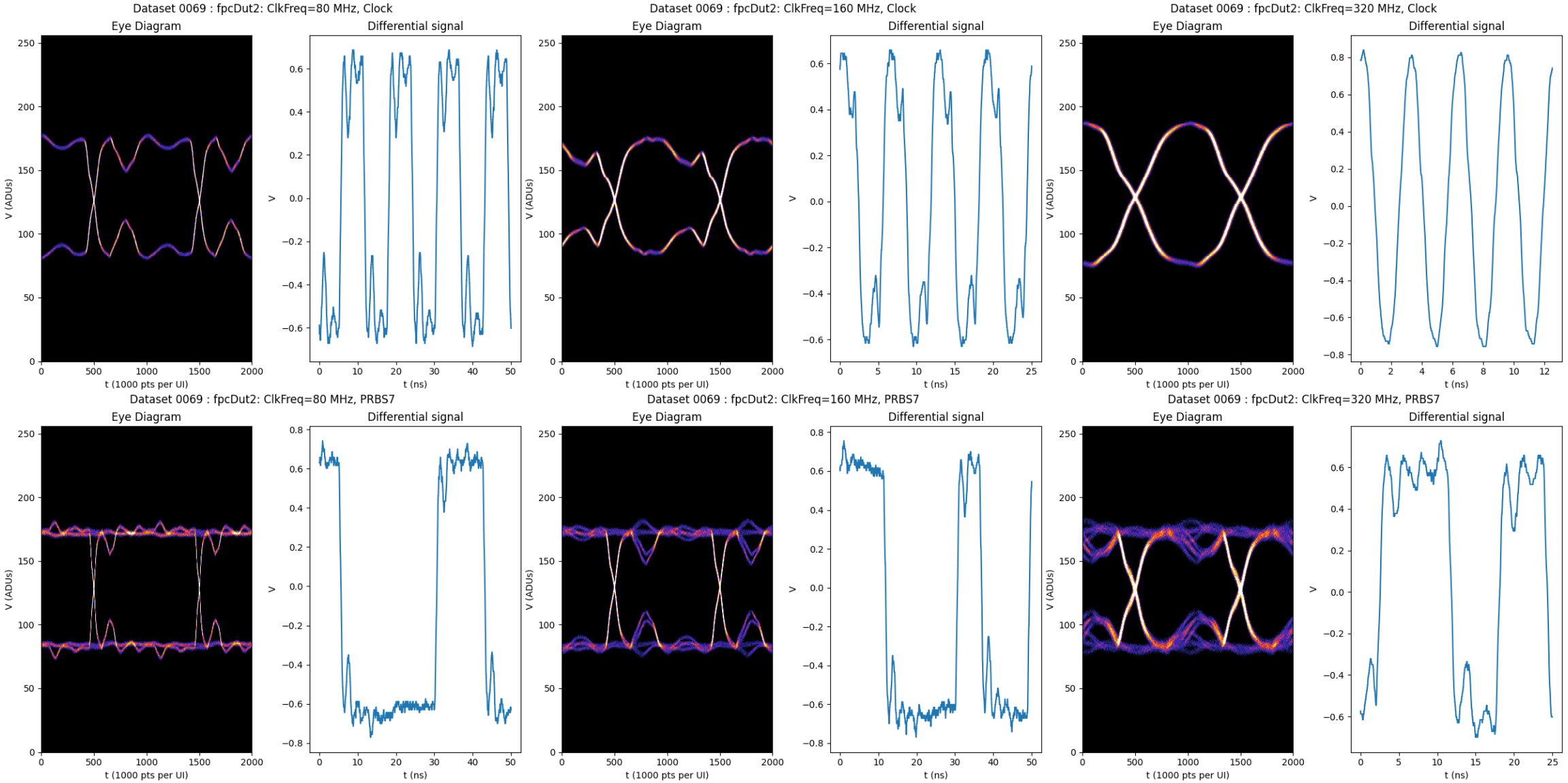
SCTRL3 to Bridge 3, but driven by USER_SMA_CLOCK



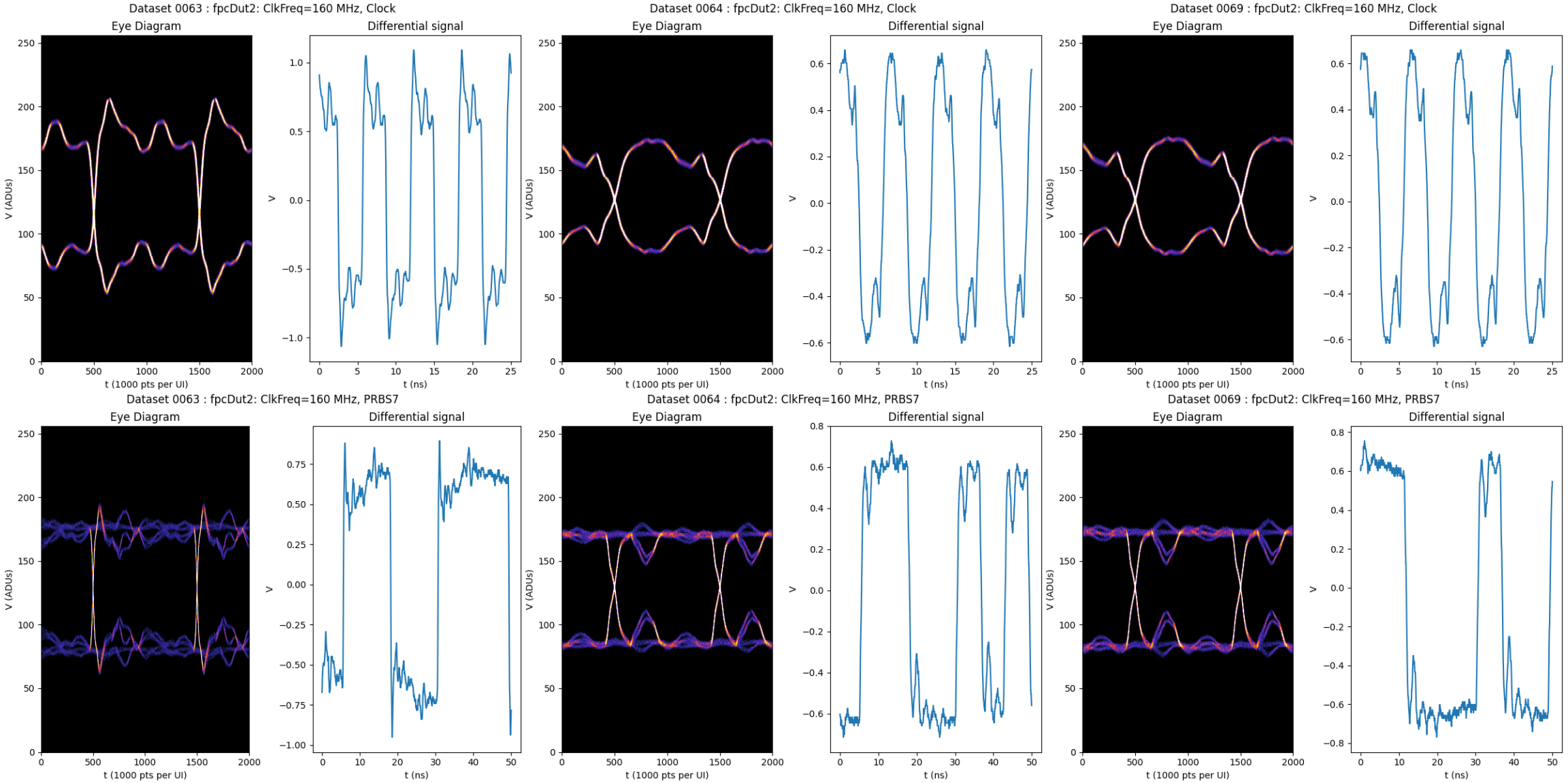
SCTRL2 to Bridge 1, USER_SMA_CLOCK, no 1k



SCTRL2 to Bridge 3, USER_SMA_CLOCK, no 1k



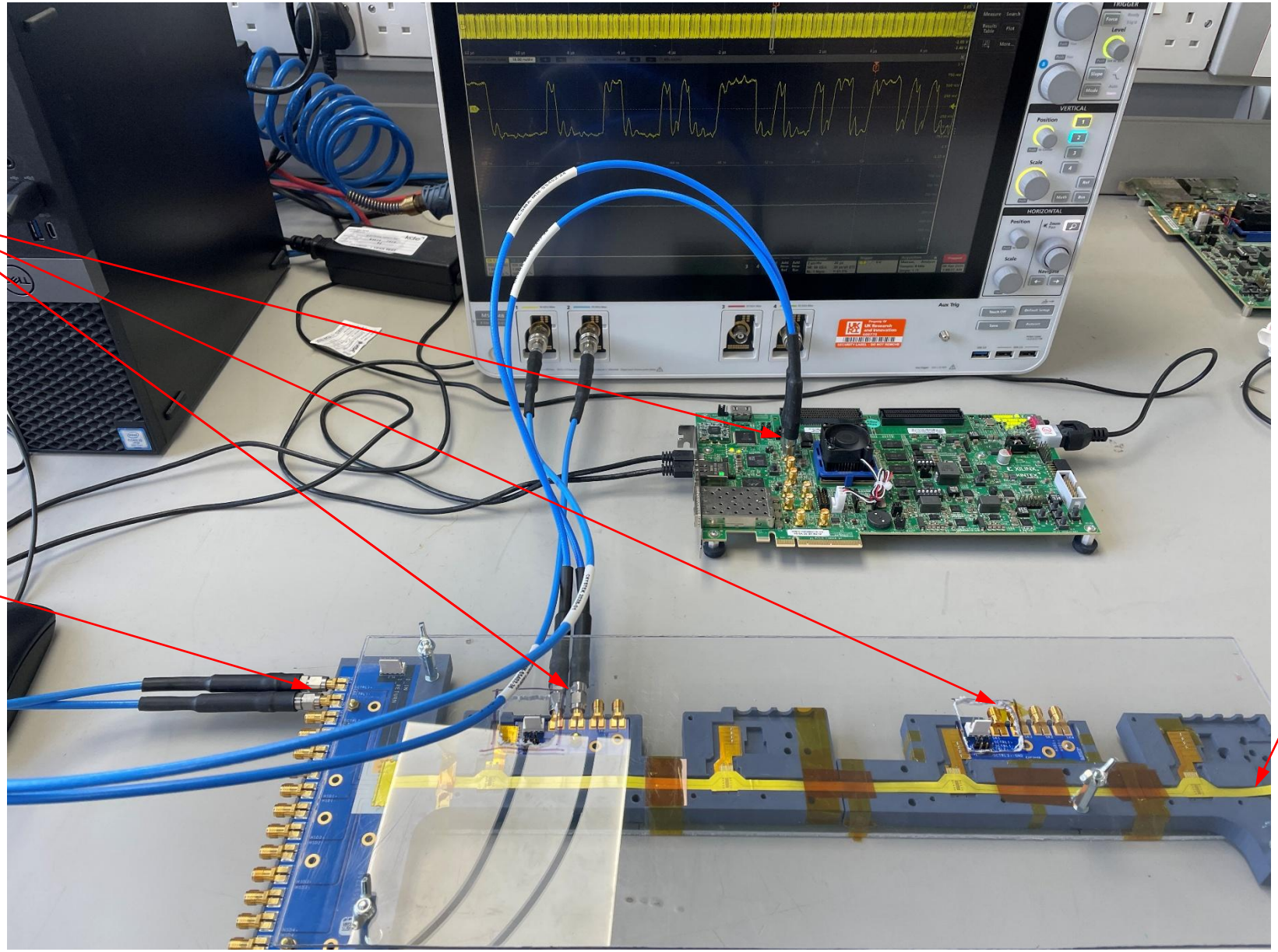
Comparison, 160 MHz Clock



Slow Control RX

Test pattern driven to SCTRL1 via bridge 1 or 3

Signal connected directly to scope with 50Ω termination to GND



100 R differential termination at the far end

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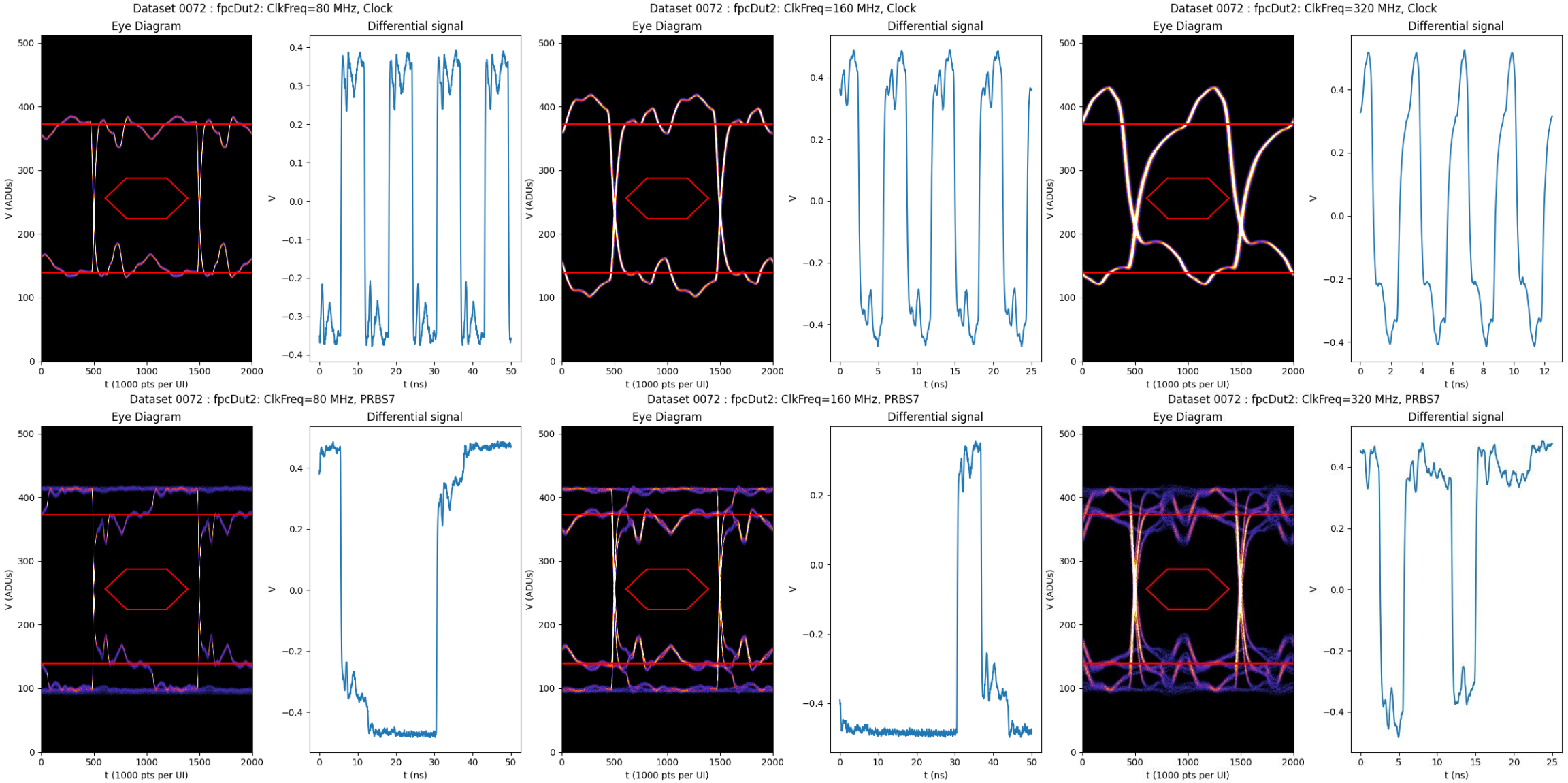
SCTRL1 RX from Bridge 1, USER_SMA_CLOCK



SCTRL1 RX from Bridge 3, USER_SMA_CLOCK