# Update on Disk FPCs

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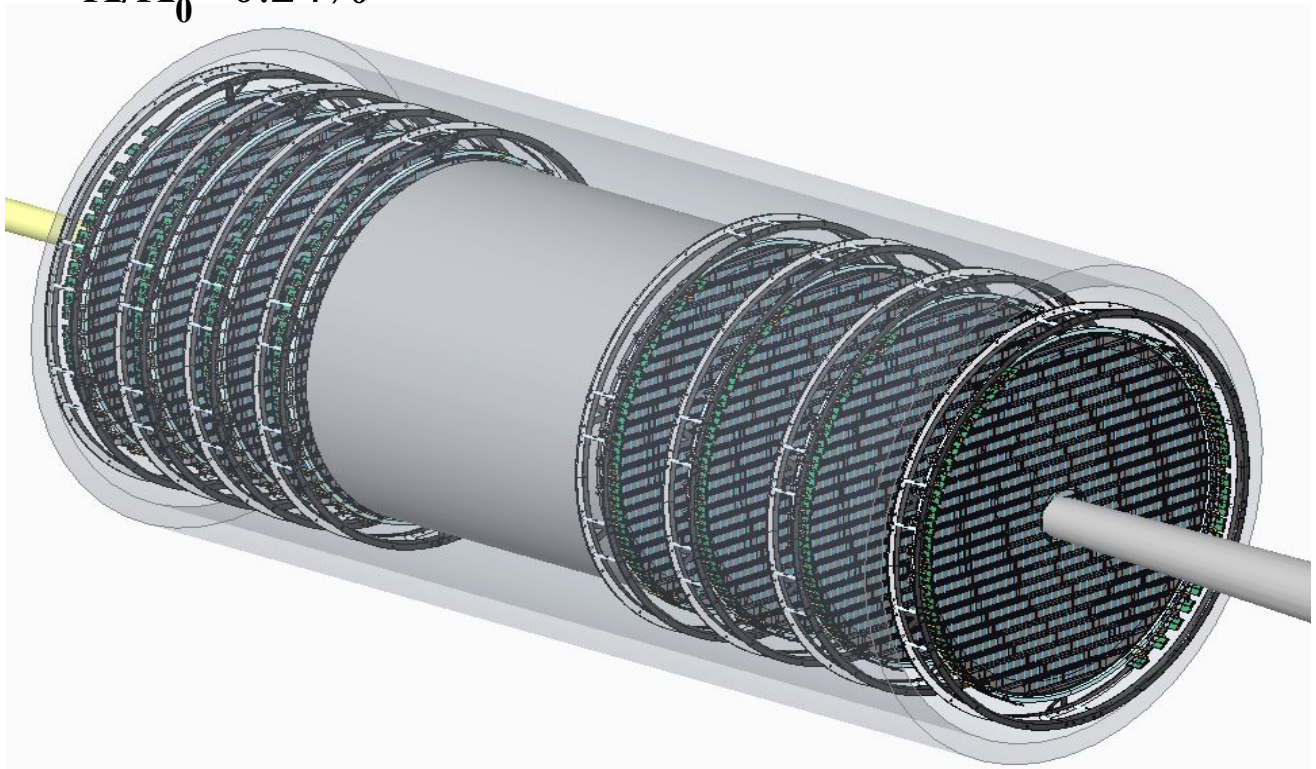
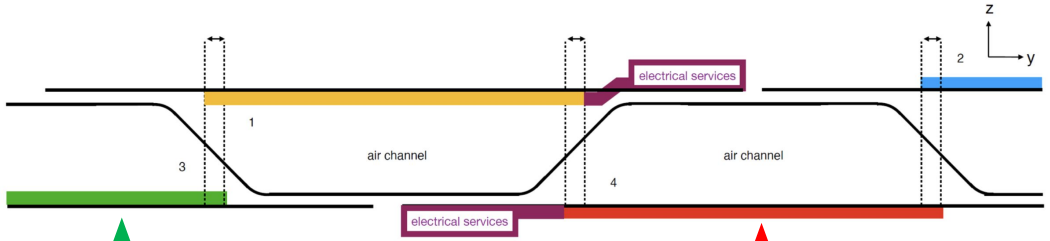
# ePIC SVT Disks

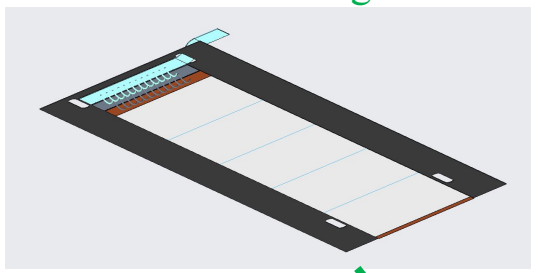
- **EIC Large-Area Sensor** with design based on ITS3 MOSAIX, mounted on low-mass CF support structure with integrated air cooling
- **AncASIC** provide negative sensor bias voltage, serial power and slow control
- **Outer radius** ranging from 24 to 40 cm
- **$X/X_0$** ~0.24%

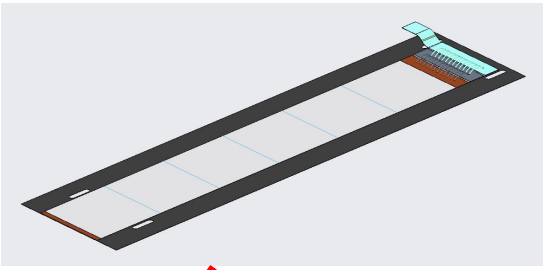


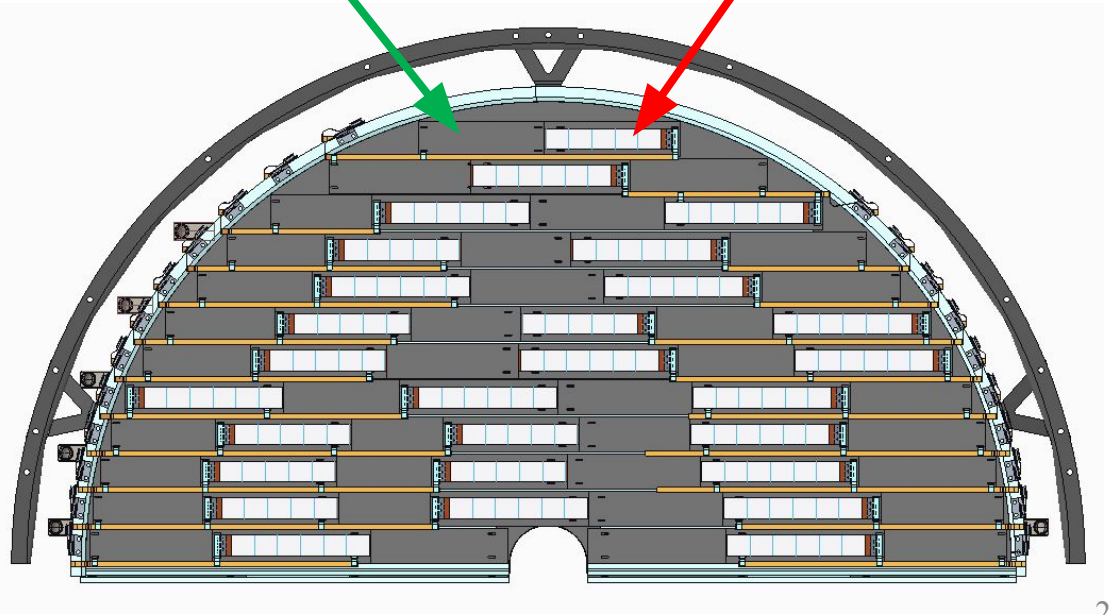



Sensor Inward Facing Module

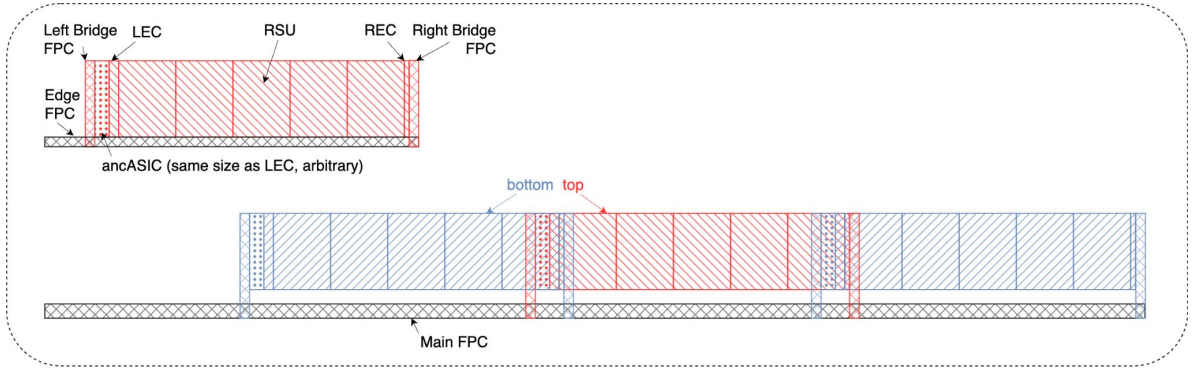
Sensor Outward Facing Module

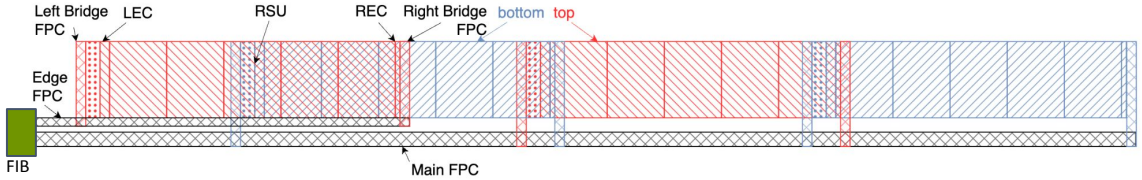


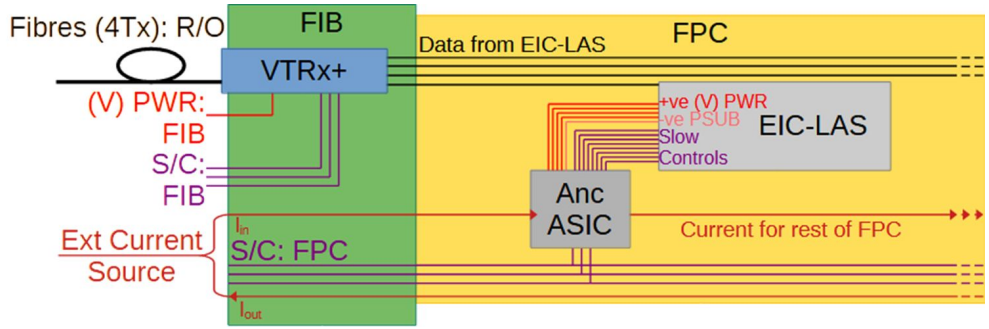




# Electrical Interfaces for SVT Disks



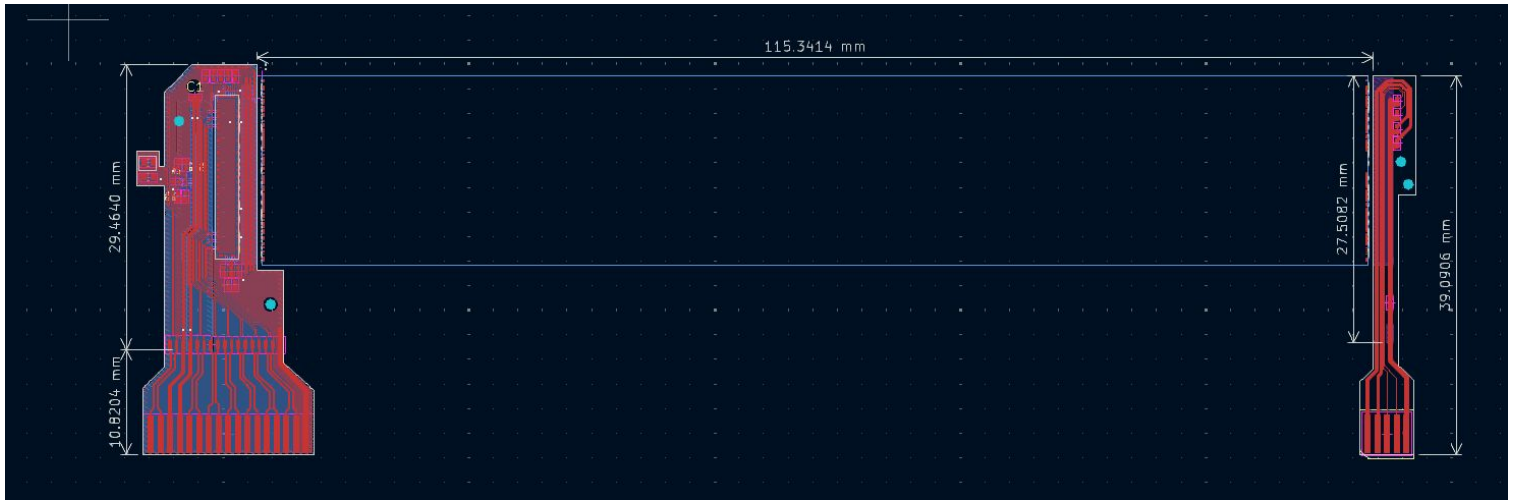




**bold: preferred option**

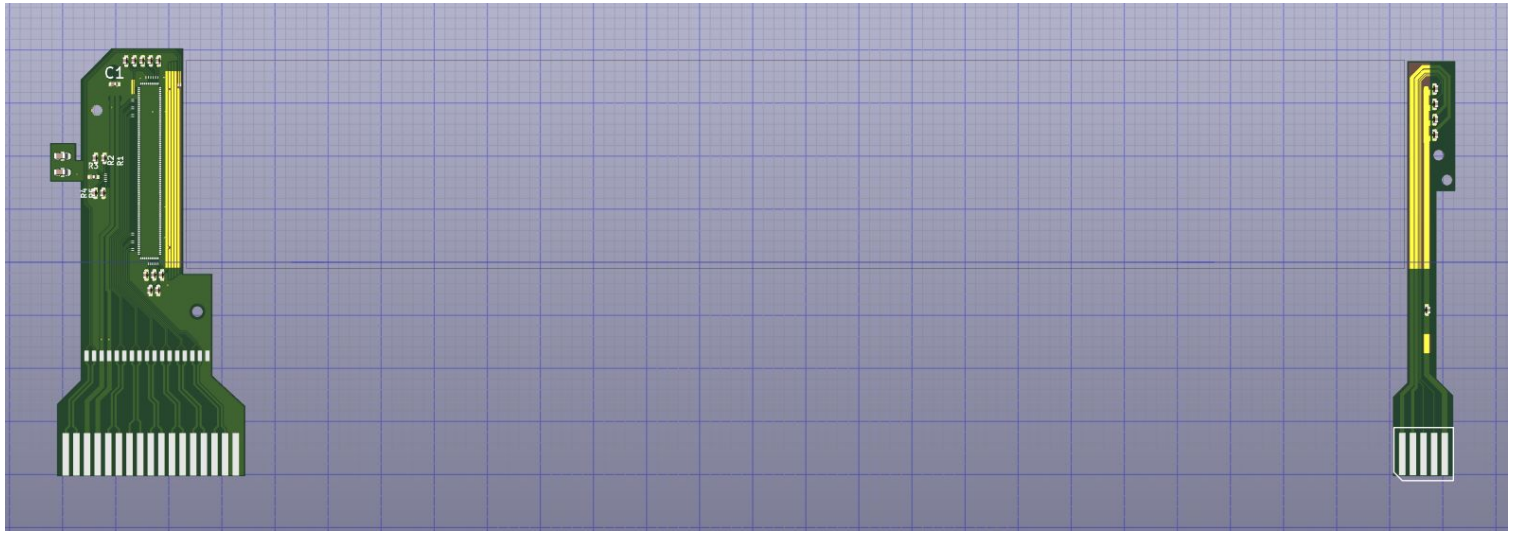
| | FIB | Main/Edge FPC | Bridge FPC | AncASIC | EIC-LAS |
|---|---|---|---|---|---|
| FIB | | | | | |
| Main/Edge FPC | **Connector**, Soldering | | | | |
| Bridge FPC | N/A | **soldering**, wire/TAB-bonding | | | |
| AncASIC | N/A | N/A | **wire-bonding**, TAB-bonding | | |
| EIC-LAS | N/A | N/A | **wire-bonding,** TAB-bonding | **wire-bonding** | |

# Bridge FPCs - Overview




- **Left bridge FPC** with **AncASIC** will handle **EIC-LAS LEC** power, slow control, high-speed data transmission.

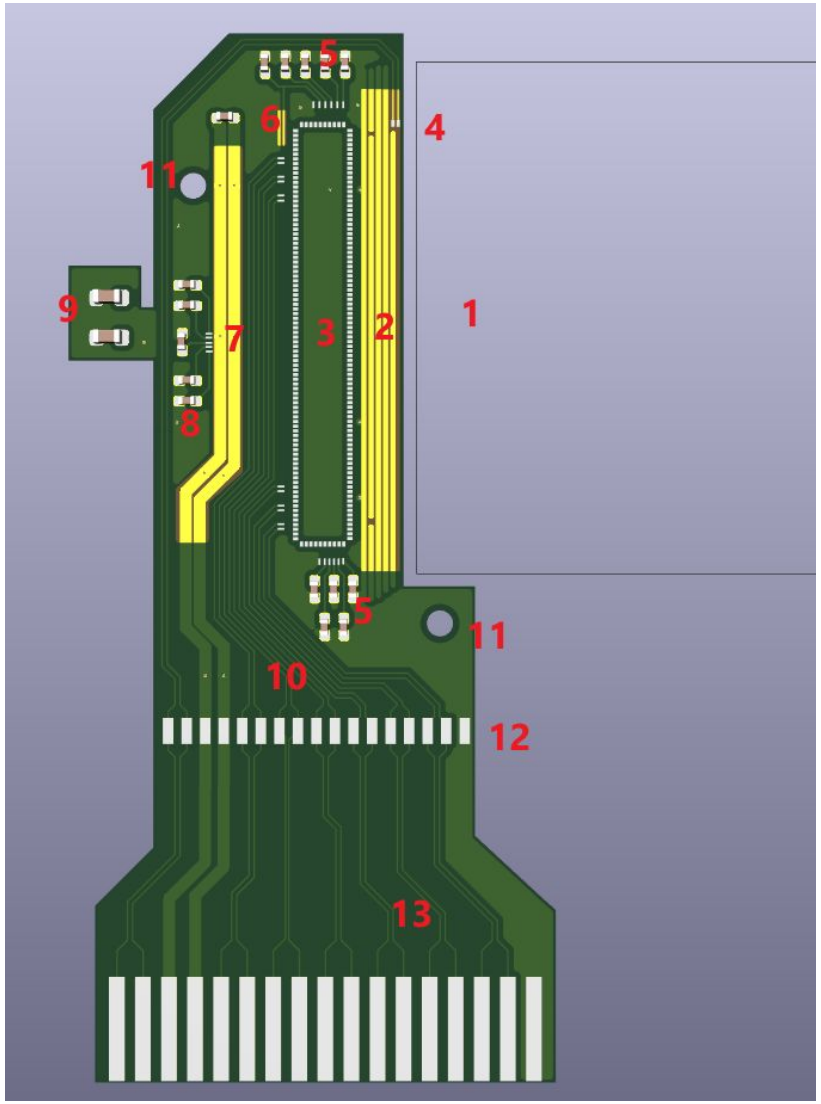
| | Area ($mm^2$) | Metal area ($mm^2$) | Fill factor |
|---|---|---|---|
| Top Layer | 278.2 | 190 | 0.69 |
| Bottom Layer | 278.2 | 260 | 0.94 |



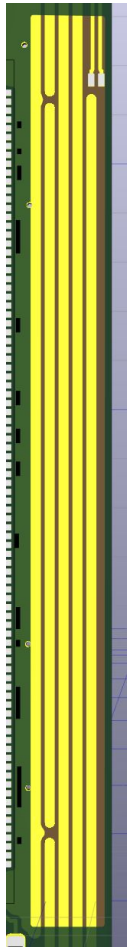

- **Right bridge FPC** with power buses connected to GND through decoupling capacitors will connect to the **EIC-LAS REC**.

| | Area ($mm^2$) | Metal area ($mm^2$) | Fill factor |
|---|---|---|---|
| Top Layer | 78.9 | 32.9 | 0.42 |
| Bottom Layer | 78.9 | 0 | 0 |

# Left Bridge FPC




AncASIC/MOSAIX pad lists from Iain Sedgwick March 2026



**1. Left side of EIC-LAS**
The distance between LAS and the FPC is **0.508 mm**. The size of the LAS is assumed as **114.330 * 19.564 mm.**

**2. Power Bus**
Net name from left to right: GND, PSUB, TXVDD, GSVDD, GAVDD, GDVDD.
Each trace is **8 mil width with 3 mil spacing**.

**3. AncASIC**
The distance between the edge of AncASIC and LAS is **2.4 mm**. The size of the ASIC is assumed as **16.434 mm × 2.388 mm**.

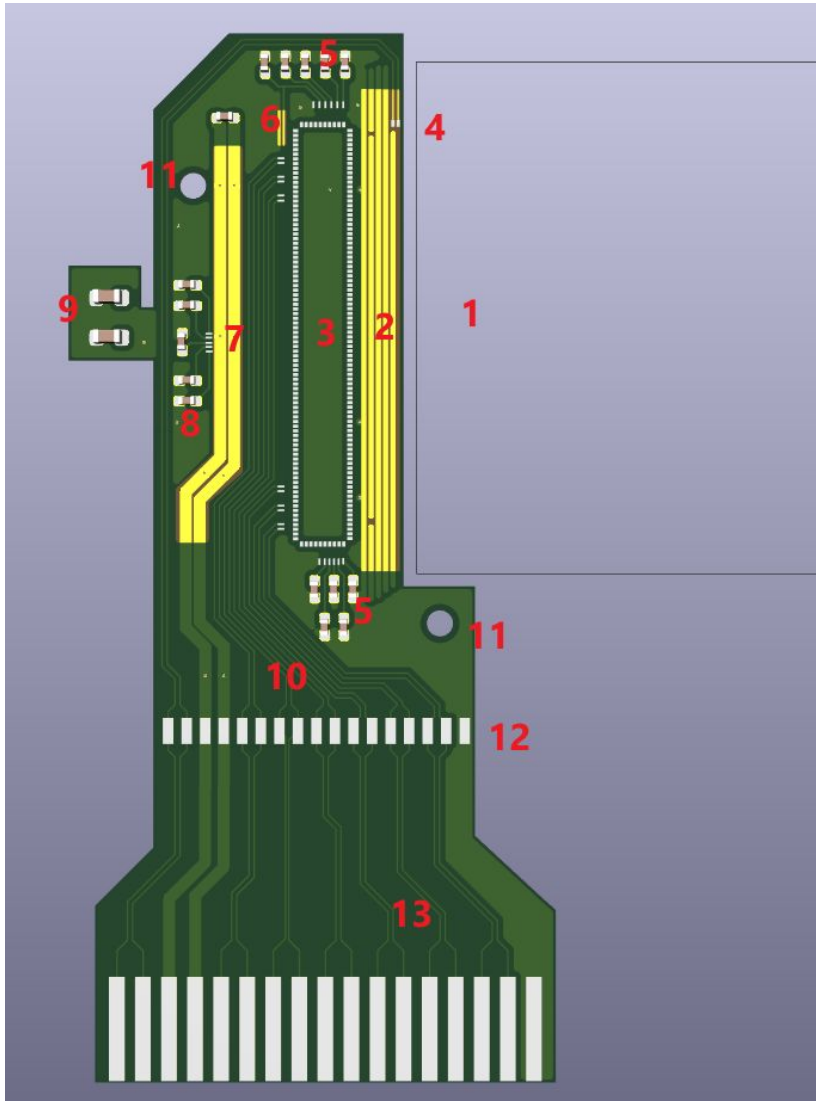
**4. Pads of the HSD**
**width/space = 55um / 140 um**. Since the pads of the HSD on LAS haven't been confirmed, I choose the HS_DATA<0> of MOSAIX as the HSD pad in this design.
Length of HSD_P = 48.4mm, HSD_N = 48.9mm.

**5. Decoupling Capacitors**
All of the Decoupling Capacitors are in the 0201 footprint.

**6. AncASIC address**
There is an open window on the soldermask, so the address pads of AncASIC can be wire-bonded to ABVDD or GND.

**Note 1:** The 55um / 140um dimensions are empirical parameters for achieving Zdiff =100Ω± 10Ω, which need to be validated through sample production and testing.
**Note 2:** The dimensions of the AncASIC are calculated as follows: (pad number - 1) × pitch (180 μm) + pad width (assumed to be 5 mil) + Corner Cell Width (300 μm) × 2. The theoretical dimensions are 16.385 mm × 2.345 mm. Due to the precision limitations of the design software, the final dimensions are 16.434 mm × 2.388 mm. These dimensions only serve solely as a reference for the placement and routing of other components on the FPC.

# Left Bridge FPC




AncASIC/MOSAIX pad lists from Iain Sedgwick March 2026

**7. $I_{in}/I_{out}$ bus**
**Width of Iin/Iout = 18 mil**. To reduce the power consumption, there is another plane for each net on the bottom layer (see power consumption page)

**8. SLDO Reference Current Resistor**
All of the resistors are in the 0201 footprint.

**9. Stiffer test**
JLC suggested the FPC designer place a stiffer beneath the device that needs to be soldered. In this prototype, we placed a stiffer on this area to evaluate the impact of stiffer. There are two 0402 pads in this area, with a stiffener placed underneath one of them. We designed this structure to verify whether an FPC without a stiffener can **withstand the high temperatures of soldering**.

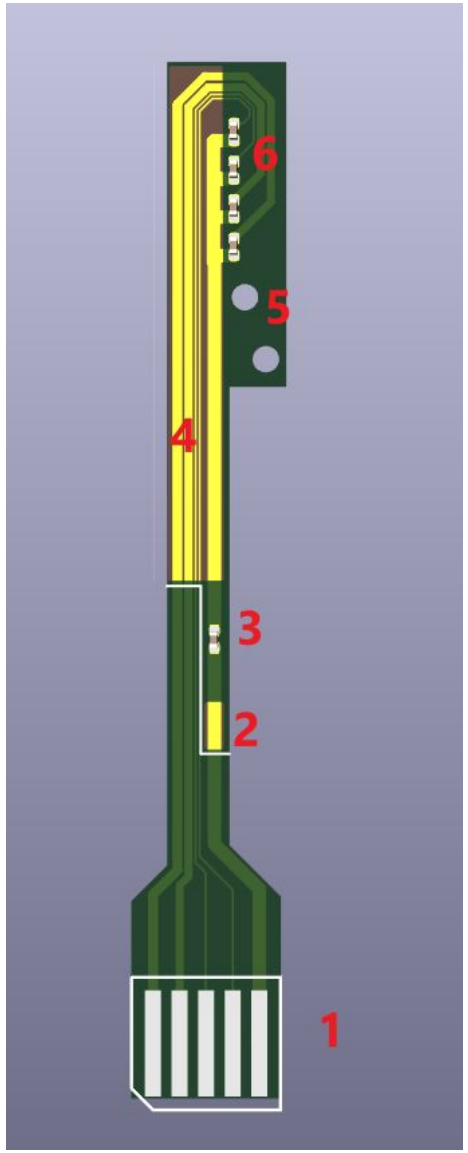
**10. Slow control signals**
**Width/Spacing 55 um/140um.**

**11. Mounting hole**
**NPTH hole, diameter = 1 mm.**

**12. FPC Soldering Pads**
The pads on the bottom edge are used to solder the bridge FPC to main FPC, pad width/spacing (**0.4mm/0.3mm**).

**13. FPC wrapper**
The FPC wrapper is designed to facilitate connecting this FPC to a test PCB with FPC connector such as 0522711779 Molex to facilitate module electrical test. The wrapper will be removed after QA.

# Right Bridge FPC




**1. FPC wrapper.**
The FPC wrapper is designed to facilitate connecting this FPC to a test PCB with FPC connector such 2005280050 Molex | Connectors, Interconnects | DigiKey, to facilitate module electrical tests. The wrapper will be removed afterwards.

**2. Solder pads**
Solder to the GND net on the Main FPC.

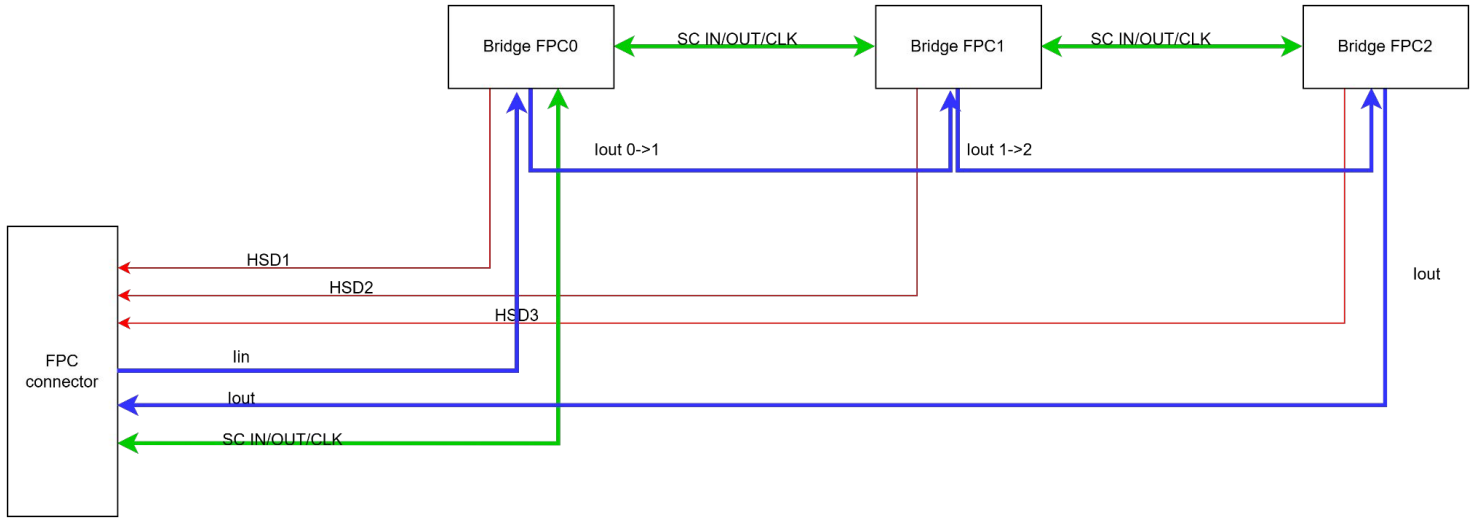
**3. AC coupling Capacitors**
The ground is AC coupled to the ground on the main FPC.

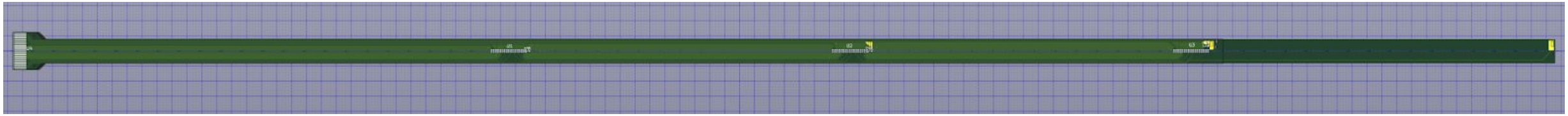
**4. Power/GND Trace:**
From left to right, net names and widths are **GDVDD (15mil), GAVDD (12 mil), GSVDD (3 mil), and PSUB (3mil)**.

**5. Mounting hole:**
NPTH hole, **diameter = 1 mm**.

**6. Decoupling Capacitor:**
All of the resistors are in the 0201 footprint.

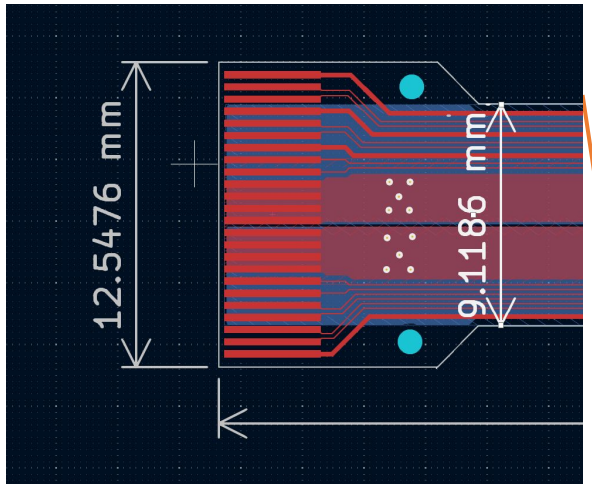
# Main FPC Overview

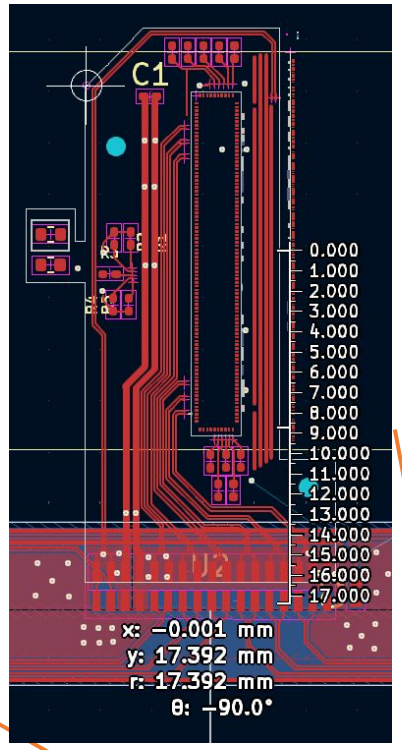


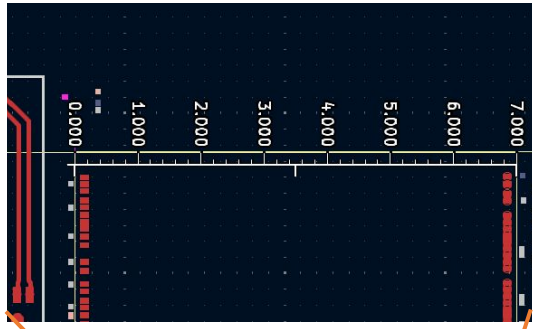




| | Area ($mm^2$) | Trace Area ($mm^2$) | Power net area ($mm^2$) | Metal fill factor |
|---|---|---|---|---|
| Top Layer | 4747.6 | 221.5 | 1875.6 | 0.45 |
| Bottom Layer | 4747.6 | 0 | 3202.2 | 0.68 |

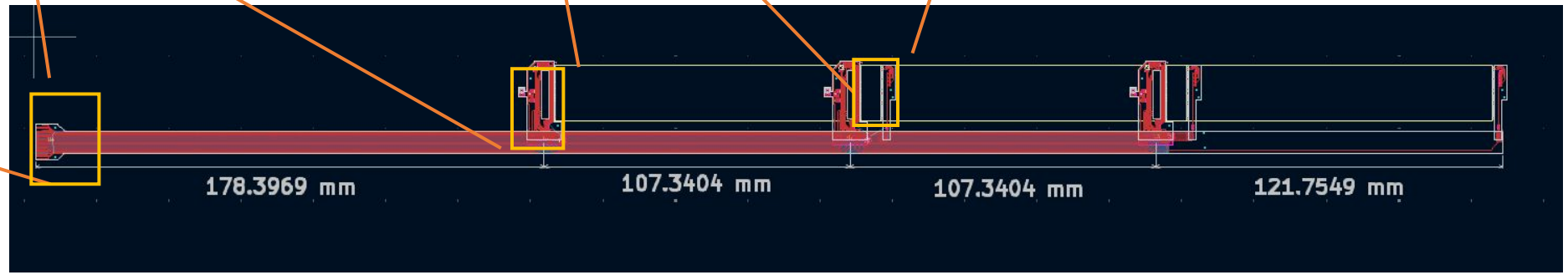
# Main FPC - feature dimensions



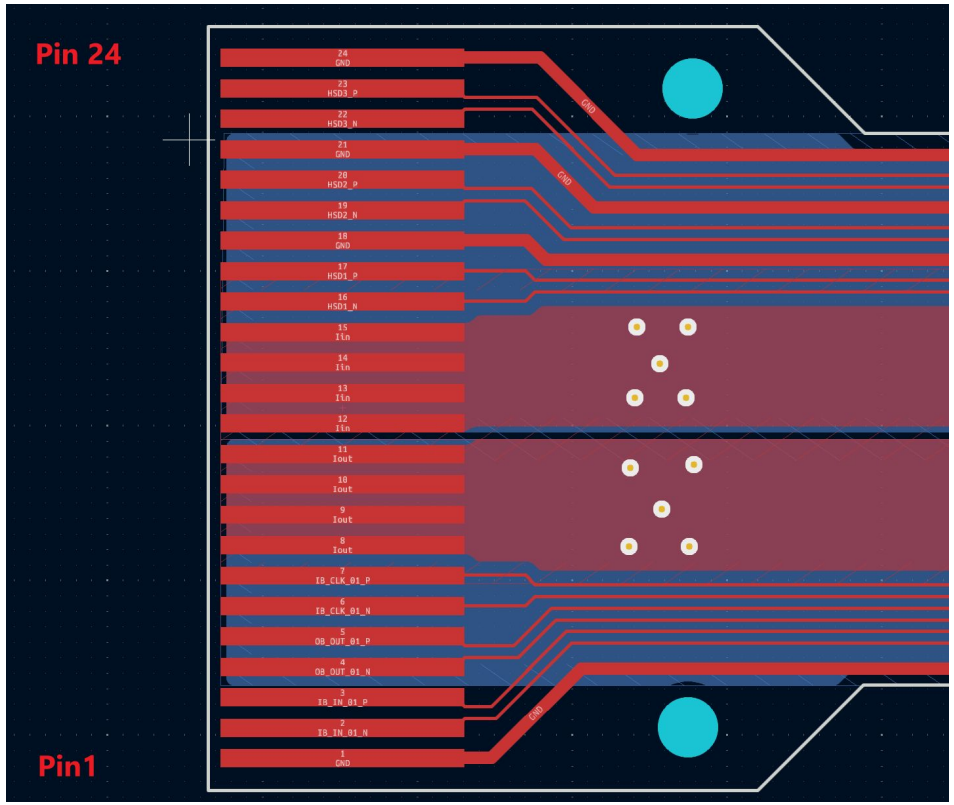




| | |
|---|---|
| Connector end width | 12.5476mm |
| Body width | 9.1186mm |
| Total length | 514.83mm |
| Distance between Center of sensor and Main FPC | 17.392 mm |
| Overlap of RSU | 1mm |
| Area | 4747.6 $mm^2$ |
| Metal Fill factor Top | 0.45 |
| Metal Fill factor Bot | 0.68 |



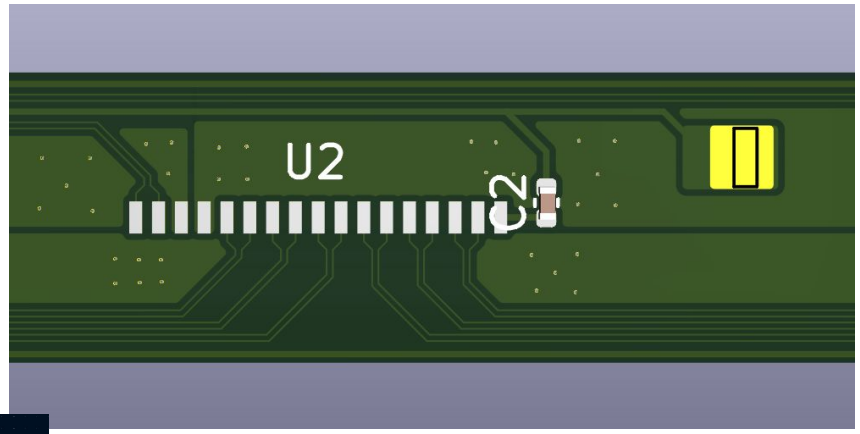
# Main FPC - connector and nets



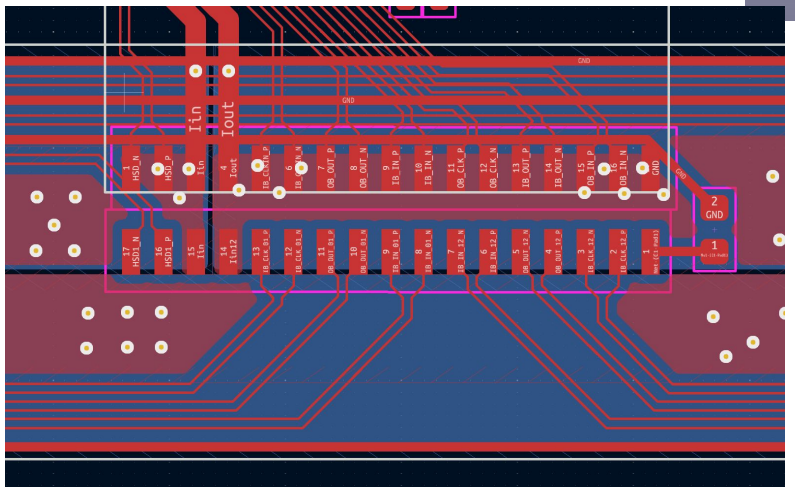

| Pin Number | Description |
|---|---|
| 24,21,18,1 | GND trace, width = 0.2 mm |
| 23,22 | High Speed Data, connect to Bridge FPC2, width/spacing = 3 mil, length = 387 mm. |
| 20,19 | High Speed Data, connect to Bridge FPC1, width/spacing = 3 mil, length = 272 mm. |
| 17,16 | High Speed Data, connect to Bridge FPC0, width/spacing = 3 mil, length = 160 mm. |
| 12-15 | Iin (See following pages for details ) |
| 8-11 | Iout (See following pages for details) |
| 7,6 | SC_CLK, width/spacing = 3mil,length = 162mm |
| 5,4 | SC_OUT, width/spacing = 3mil, length =162 mm |
| 3,2 | SC_IN, width/spacing = 3mil, length = 164 mm |

Note: All GND traces are not interconnected on the main FPC; therefore, common grounding must be established externally (e.g. FIB) if needed.

# Connecting Bridge FPCs to Main FPC

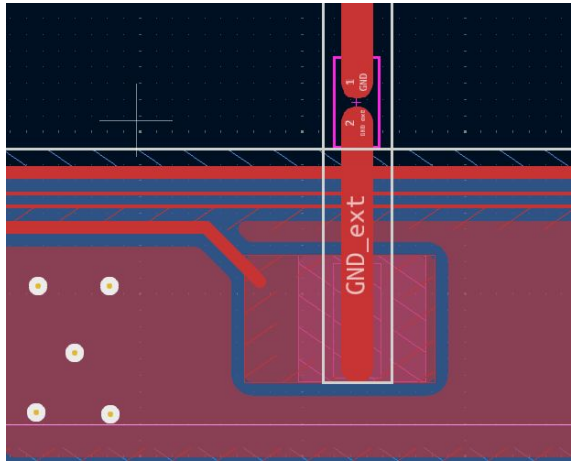



Left Bridge FPC:




The left bridge FPC will be soldered to the main FPC by 17 pairs of pads. **Each pad has width 0.4mm, length 1mm, pitch 0.7mm.**

Right Bridge FPC:




The right bridge FPC will be soldered to the main FPC by 1 pair of pads.

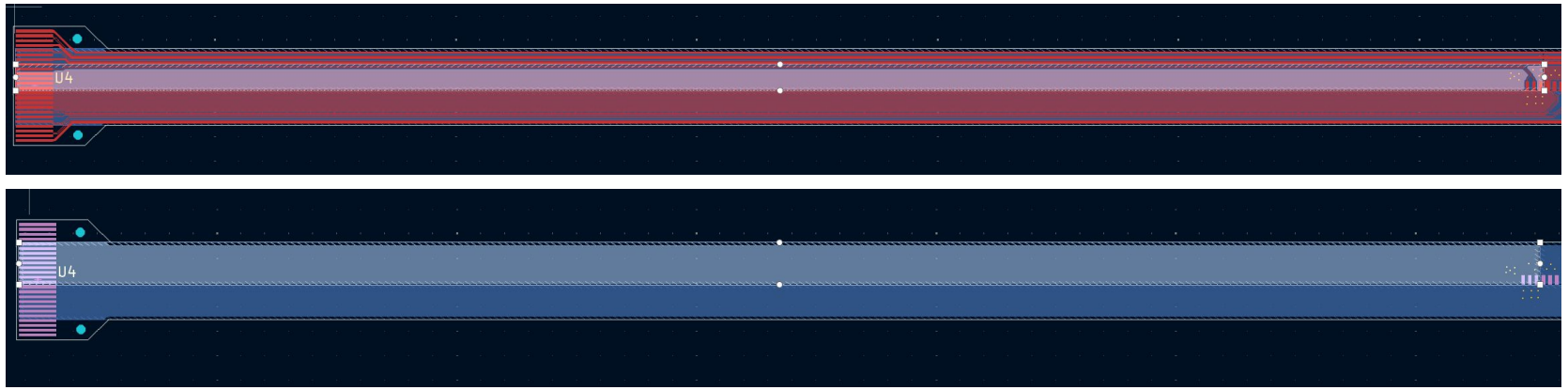
# FPC Cross section

| JLC | LTU |
|---|---|
| Pi: 12.5 um | Pi: 25um |
| Copper: 12 um | Aluminum: 15 um |
| | Pi: 10 um |
| Glue: 15 um | Glue: 5 um |
| Dielectric:25 um | Dielectric:25 um |
| Glue: 15 um | Glue: 5 um |
| Copper: 12 um | Aluminum: 15 um |
| | Pi: 10 um |
| Pi: 12.5 um | |
| Total: 104 um | Total: 125um |

**We plan to produce “mechanical” FPC prototypes with Cu traces by JLCPCB.**

**The power consumption calculations in the following slides are based on the LTU’s Al-based FPC structure.**

# Main FPC - Power consumption Estimation

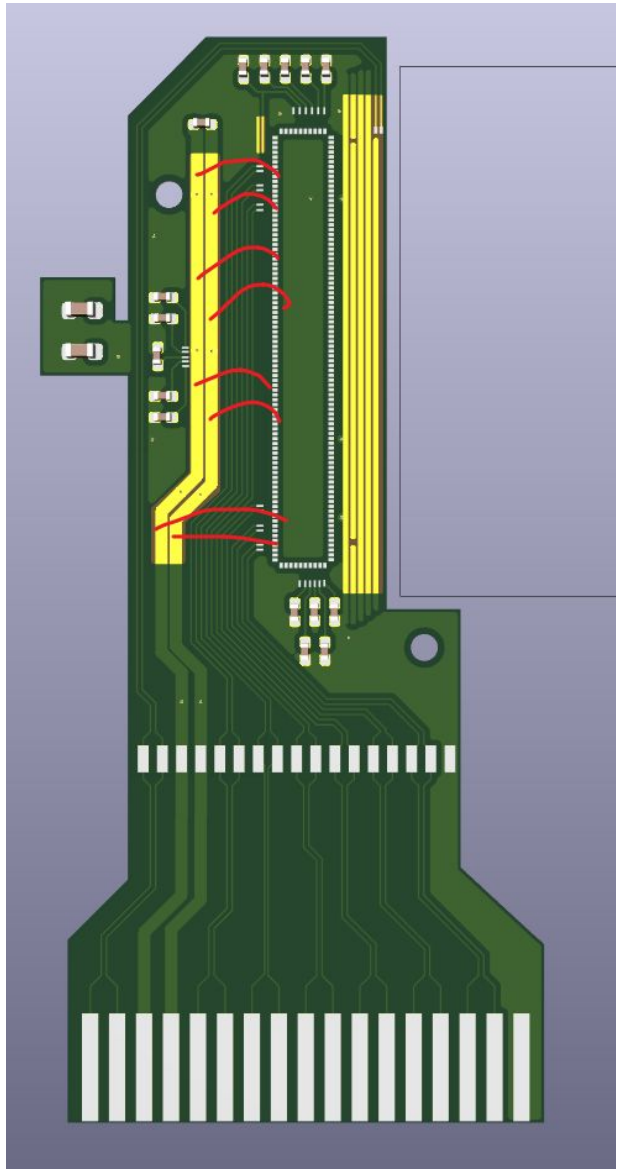



$I_{in01}$ net in the top and bottom layers

| Net | From | To | Material | Resistivity@ 20℃ (ohm·m) | Thickness (m) | length (m) | Width on top (m) | Width on bottom (m) | Resistance Top | Resistance Bottom | Resistance |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{in01}$ | FPC connector | Bridge FPC0 | Aluminum | 2.65E-08 | 1.50E-05 | 0.17 | 0.00196 | 0.00460 | 1.53E-01 | 6.53E-02 | 4.58E-02 |
| $I_{in12}$ | Bridge FPC0 | Bridge FPC1 | Aluminum | 2.65E-08 | 1.50E-05 | 0.107 | 0.00282 | 0.00460 | 6.70E-02 | 4.11E-02 | 2.55E-02 |
| $I_{in23}$ | Bridge FPC1 | Bridge FPC2 | Aluminum | 2.65E-08 | 1.50E-05 | 0.107 | 0.00371 | 0.00460 | 5.10E-02 | 4.11E-02 | 2.27E-02 |
| $I_{out}$ | Bridge FPC2 | FPC connector | Aluminum | 2.65E-08 | 1.50E-05 | 0.387 | 0.00228 | 0.00371 | 3.14E-01 | 1.84E-01 | 1.16E-01 |

**Assume the Iin/Iout current is 1.5 A, The power consumption is estimated as 473 mW.**

# Bridge FPC power consumption Estimation – $I_{in}$/$I_{out}$

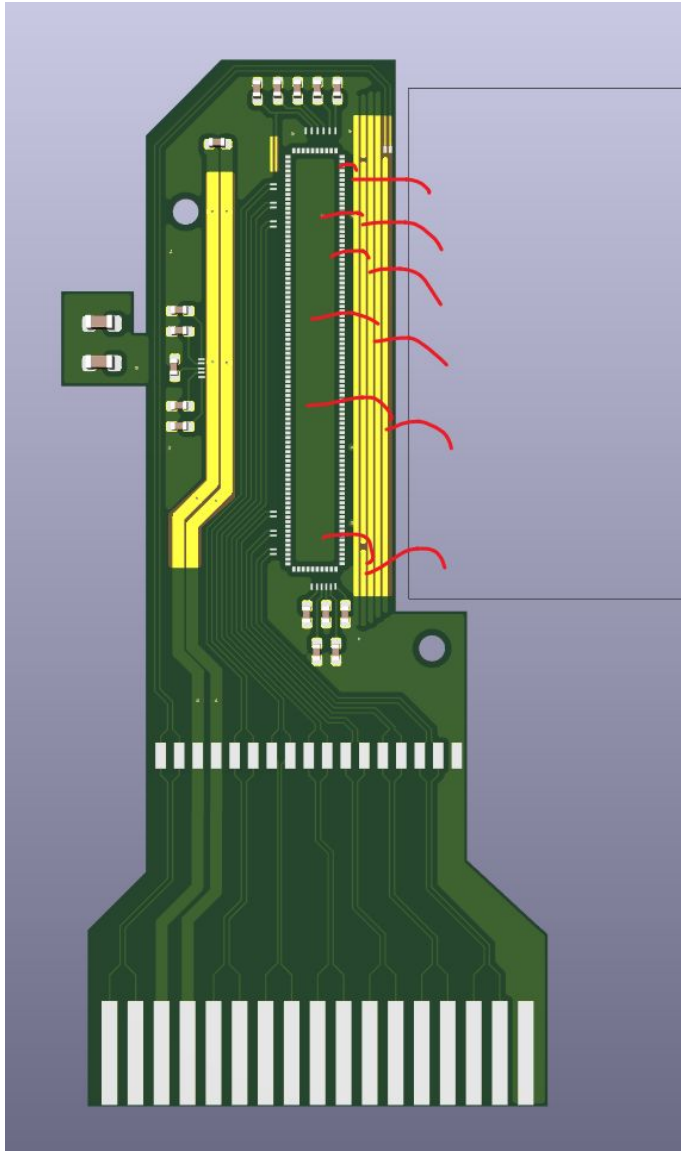


The resistance of Iin/Iout can be divided into two parts: Trace on FPC and bonding wire.
The estimated resistance and the parameters that used in the calculation is shown in the following:

| Trace on FPC | | Bonding wire | |
|---|---|---|---|
| ρ:**Resistivity@20℃ (ohm·m)** | 2.65E-8 | ρ:**Resistivity@20℃ (ohm·m)** | 2.65E-8 |
| **H:Thickness (m)** | 1.50E-5 | **D:Diameter (m)** | 2.54E-5 |
| **W:Width on top (m)** | 0.0003084 (Iin/Iout) | **L:Mean length (m)** | 0.0029(Iin); 0.0023(Iout) |
| **Width on the bottom (m)** | 0.0022(Iin); 0,0027(Iout) | | |
| **L:Mean length (m)** | 0.017(Iin/Iout) | **N:wire number** | 27(Iin); 40 (Iout) |
| **Resistance (ohm)** | 0.0118 (Iin) 0.0098(Iout) | **Resistance (ohm)** | 5.6e-3(Iin);3e-3(Iout) |

**Assume the current is 1.5 A, The power consumption is estimated as 68 mW. The main contribution is from the trace of Iin/Iout on FPC (~49 mW).**

# Bridge FPC power consumption Estimation – Power net



The power consumption of TXVDD/GSVDD/GAVDD/GDVDD can be divided into two parts:1. From AncASIC to power bus; 2. From the power bus to the left edge of LAS (Power loss on the power bus is insignificant, as the current travels only a short distance on the it);

| From AncASIC bonding to power bus | | From power bus to left edge of LAS | |
|---|---|---|---|
| ρ:**Resistivity@20℃(ohm·m)** | 2.65E-8 | ρ:**Resistivity@20℃ (ohm·m)** | 2.65E-8 |
| **D:Diameter (m)** | 2.54E-5 | **D:Diameter (m)** | 2.54E-5 |
| **L(mm):** | 0.8(TXVDD); 1.1(GSVDD); 1.4(GAVDD); 1.7(GDVDD) | **L1(mm):** | 1.9(TXVDD); 1.6(GSVDD); 1.3(GAVDD); 1(GDVDD) |
| **Number of bonding wire:** | 3 (TXVDD); 6(GSVDD); 4(GAVDD); 15(GDVDD) | **Number of bonding wire:** | 6 (TXVDD); 12(GSVDD); 8(GAVDD); 20(GDVDD) |
| **Resistance:** | 1.4e-2(TXVDD);9.6e-3(GSVDD); 1.8e-2(GAVDD);5.9e-3(GDVDD) | **Resistance:** | 1.7e-2(TXVDD);7.0e-3(GSVDD); 8.5e-3(GAVDD);2.6e-3(GDVDD) |

Calculate the operating current for each power based on updated numbers form Chamonix:

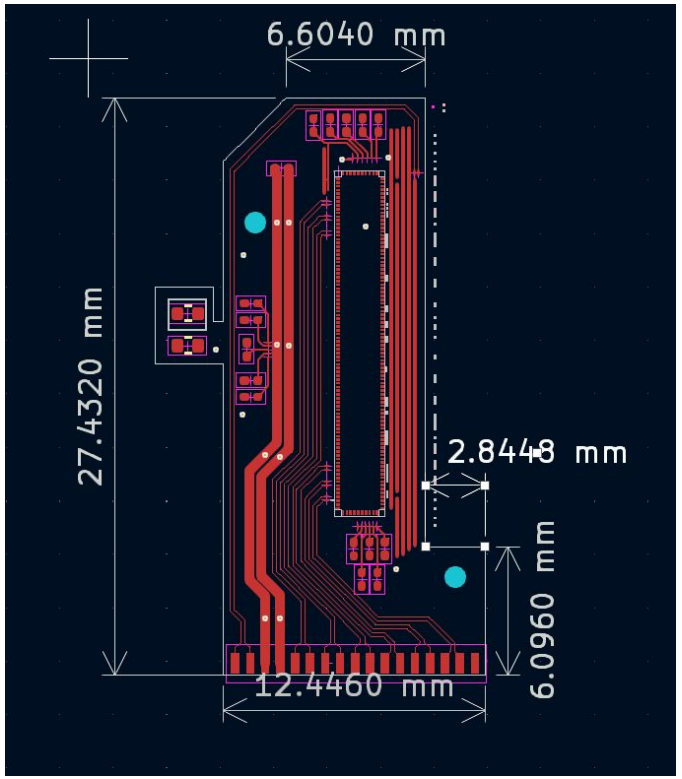
**The power consumption on power net is 6.3 mW**

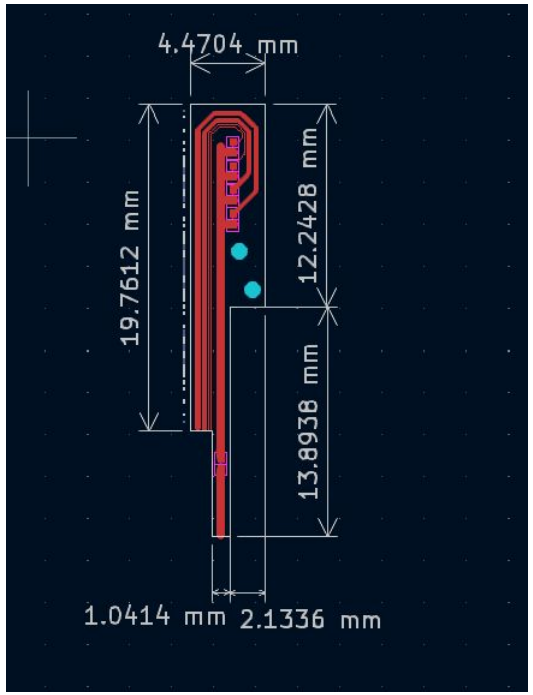
| | Voltage(V) | Typ Power (mW) | | | Max Power (mW) | | |
|---|---|---|---|---|---|---|---|
| | | ESR | Cham | Cham-SC | ESR | Cham | Cham-SC |
| GAVDD | 1.32 | 222 | 222 | 222 | 356 | 356 | 356 |
| GDVDD | 1.32 | 908 | 1052 | 349 | 1148 | 1280 | 560 |
| GSVDD | 1.32 | 52 | 38 | 38 | 78 | 55 | 55 |
| TXVDD | 1.2 | 240 | 71 | 66 | 360 | 100 | 91 |
| Total (LAS) | | 1422 | 1382 | 675 | 1942 | 1791 | 1062 |

# Summary and Outlook

- **FPCs** provide electrical interfaces between EIC-LAS, AncASIC and FIB (lpGBT and VTRX+).
- A first layout design is completed for SVT disk FPC, taking into account the requirements of power and data transmission.
- Plan to produce a first batch of Cu-based mechanical prototypes to check FPC dimensions and inter-connection, with the main goal to facilitate disk module development.
- Will engage with **LTU** to design and produce Al-based FPCs for electrical functionality tests.
  - On-going work by UK and Trieste for bonding and data transmission with LTU FPCs

# Bridge FPC - Feature dimensions

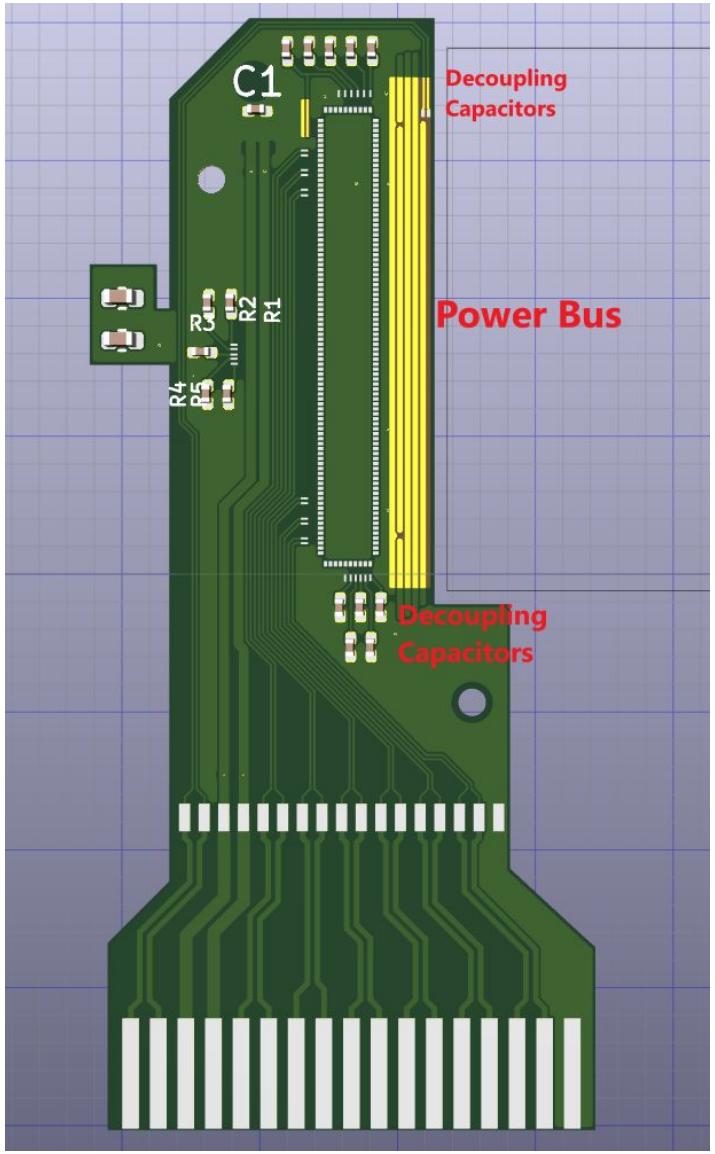


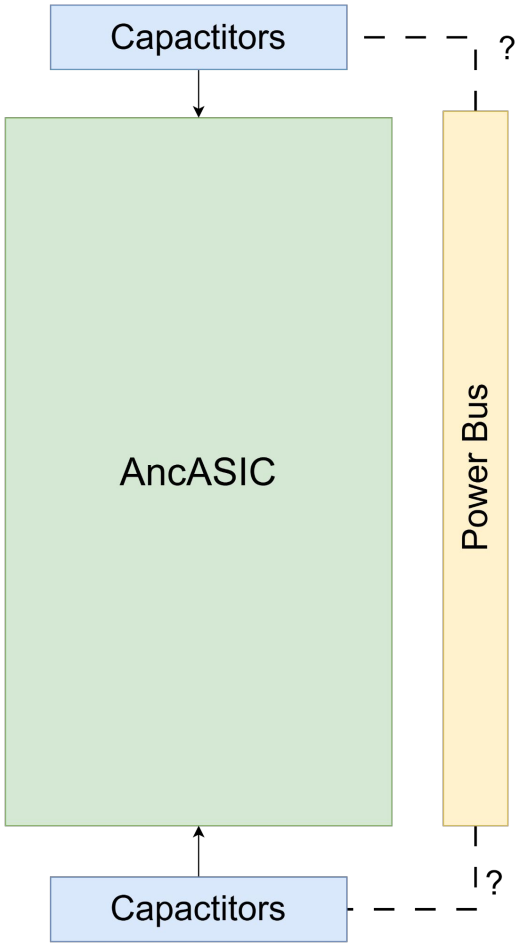




| | Area ($mm^2$) | Metal area ($mm^2$) | Fill factor |
|---|---|---|---|
| Top Layer | 276.2 | 190 | 0.69 |
| Bottom Layer | 276.2 | 260 | 0.94 |

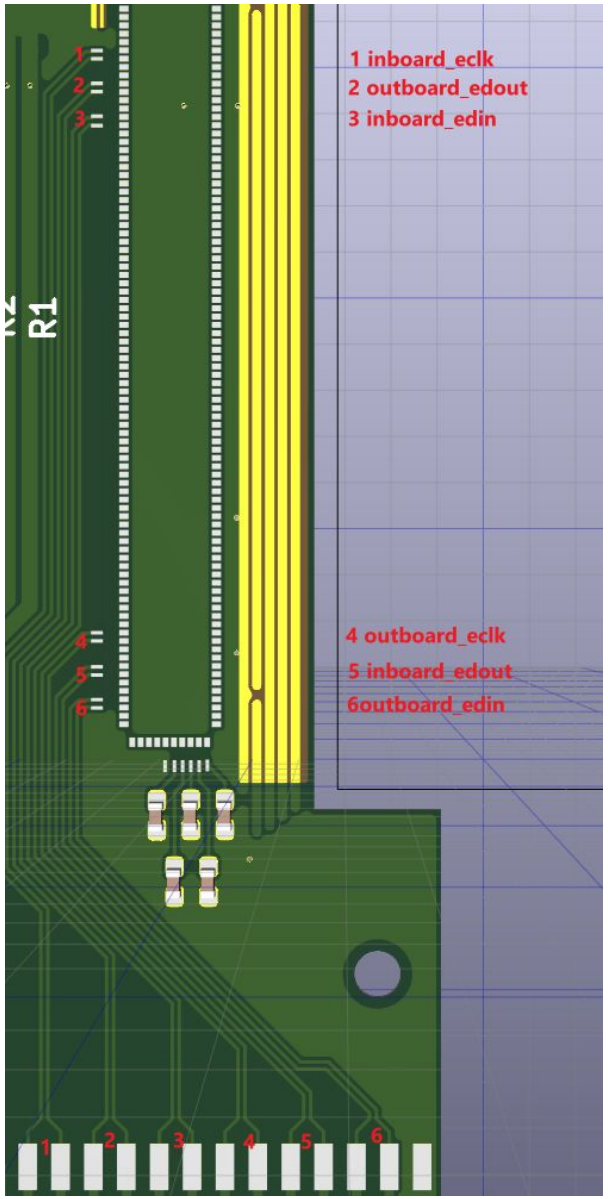
| | Area ($mm^2$) | Metal area ($mm^2$) | Fill factor |
|---|---|---|---|
| Top Layer | 78.9 | 32.9 | 0.42 |
| Bottom Layer | 78.9 | 0 | 0 |

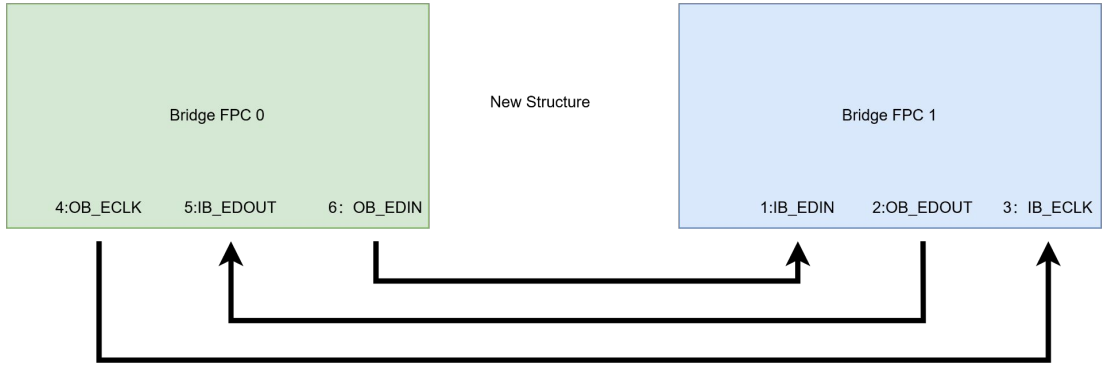
# LV Decoupling Capacitors

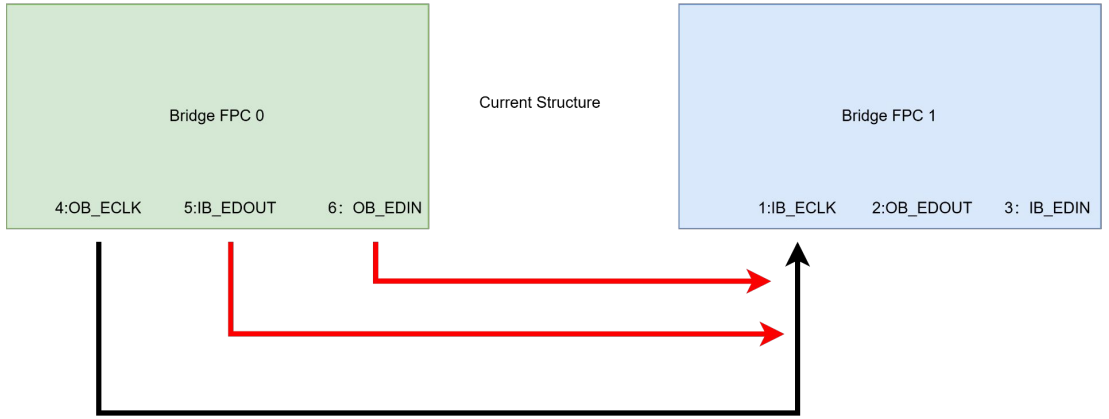



This figure shows the portion of the bridge FPC design related to the AncASIC.
The Power Bus is on the right side of the AncASIC, and the decoupling capacitors are located on the top and bottom sides.
The decoupling capacitors are currently connected only to the pads on the corresponding top and bottom sides of the AncASIC.
The question now is: **whether the Power Bus needs to be directly connected to the decoupling capacitors.**




It's impossible to complete the connections between 4-1,5-2 and 6-3 without any wire crossing.

**A possible solution is swapping the pad positions of pair inboard_eclk/inboard_edin or outboard_eclk/outboard_edin**

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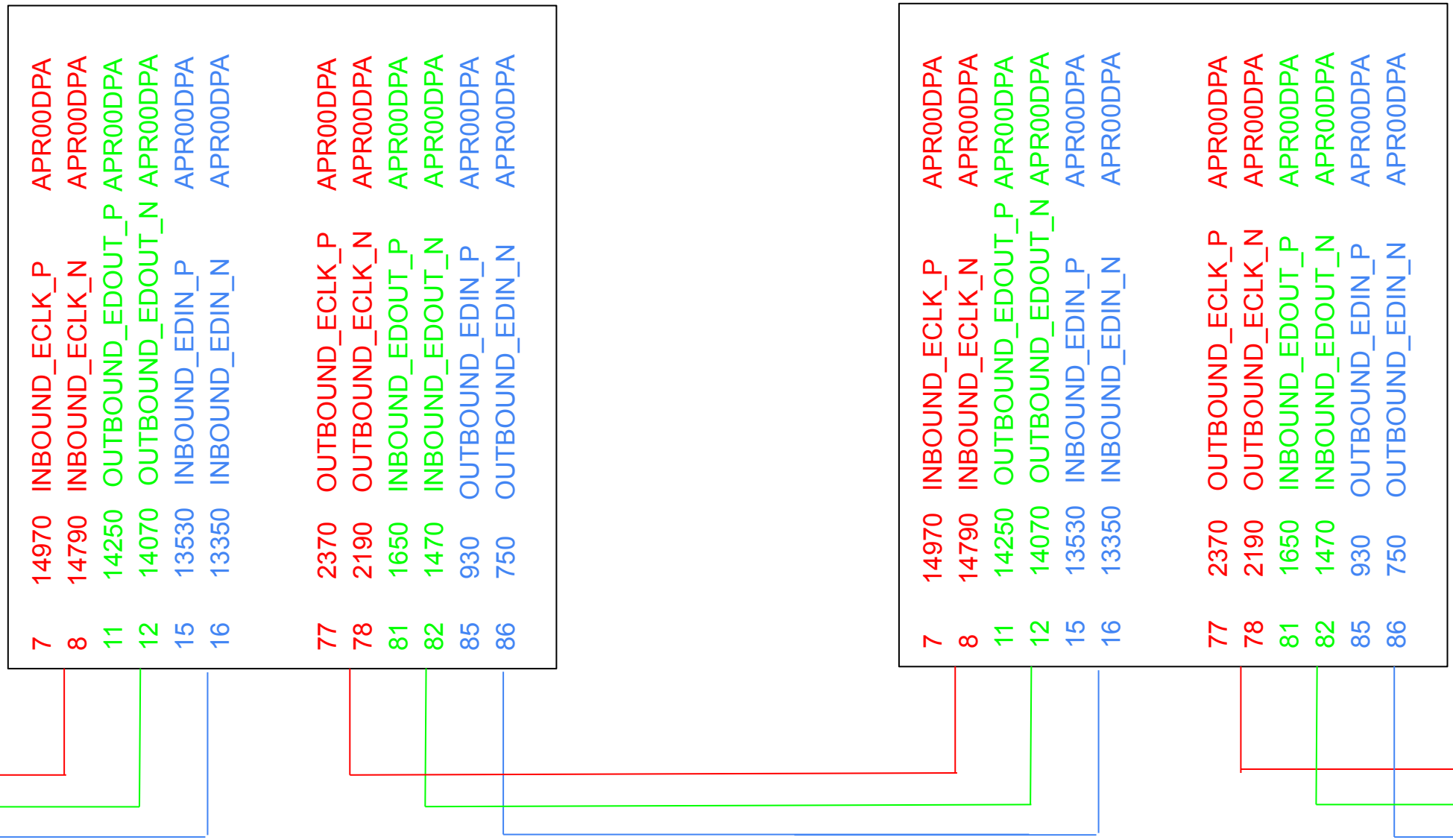
# Current SC Pads on AncASIC



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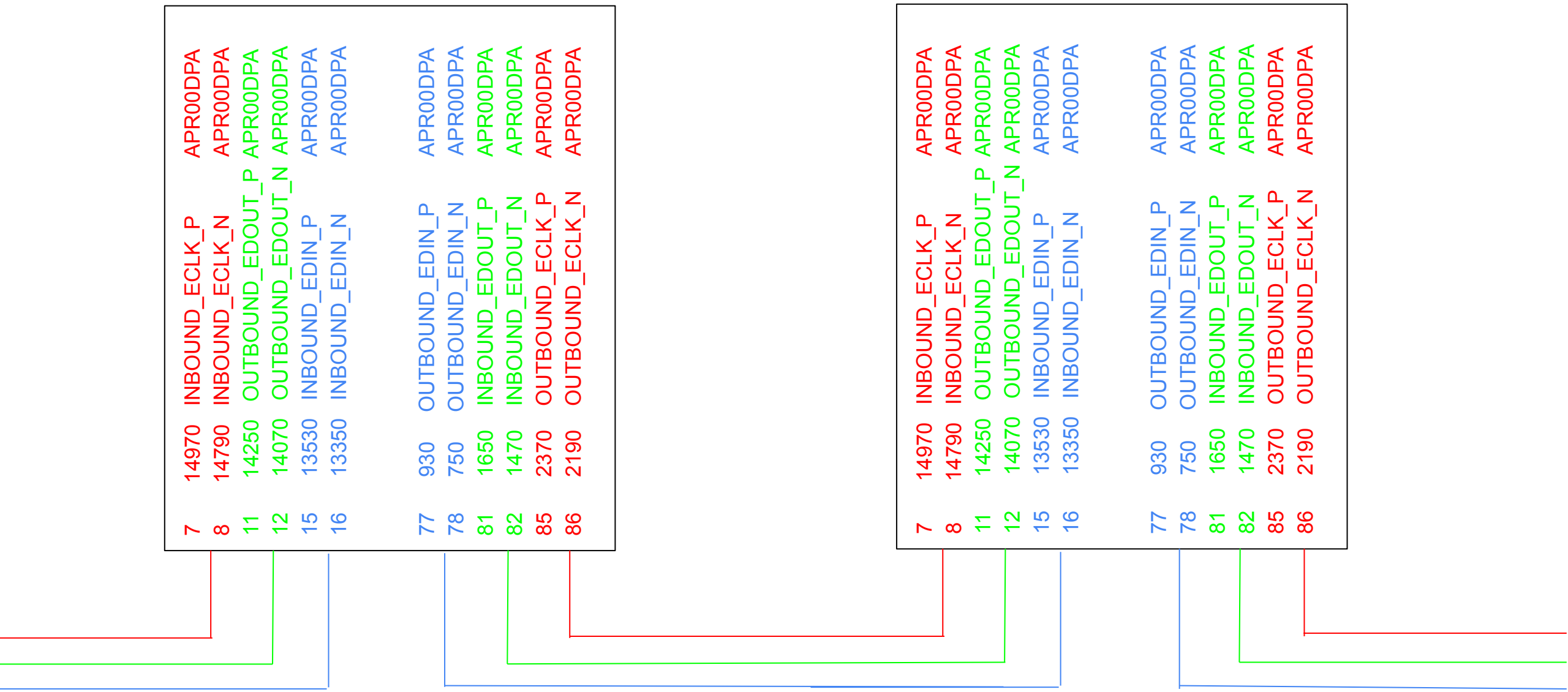
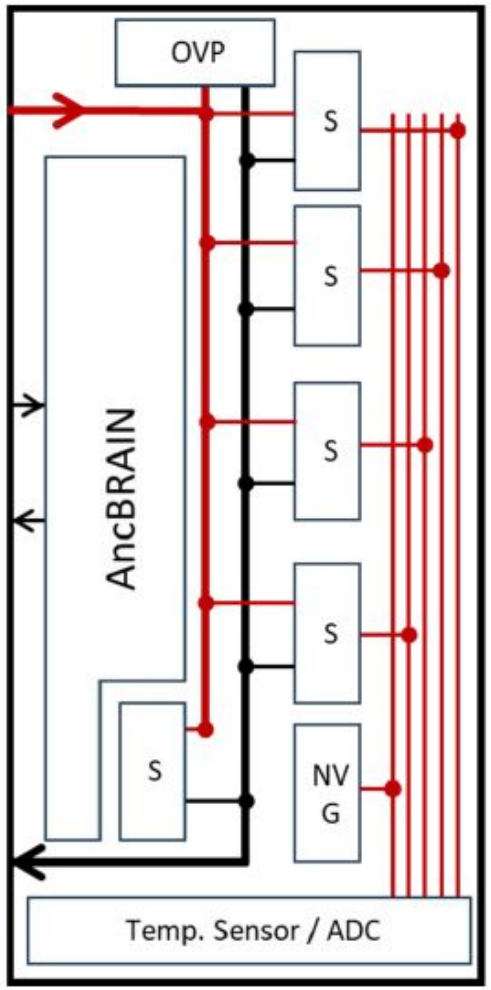
# Modified SC Pads on AncASIC



# Sanity check on the “LAS side” of B-FPC




LEC

GSVDD/GSVSS

GAVDD/GAVSS

GDVDD/GDVSS

TXVDD/TXVSS

PSUB

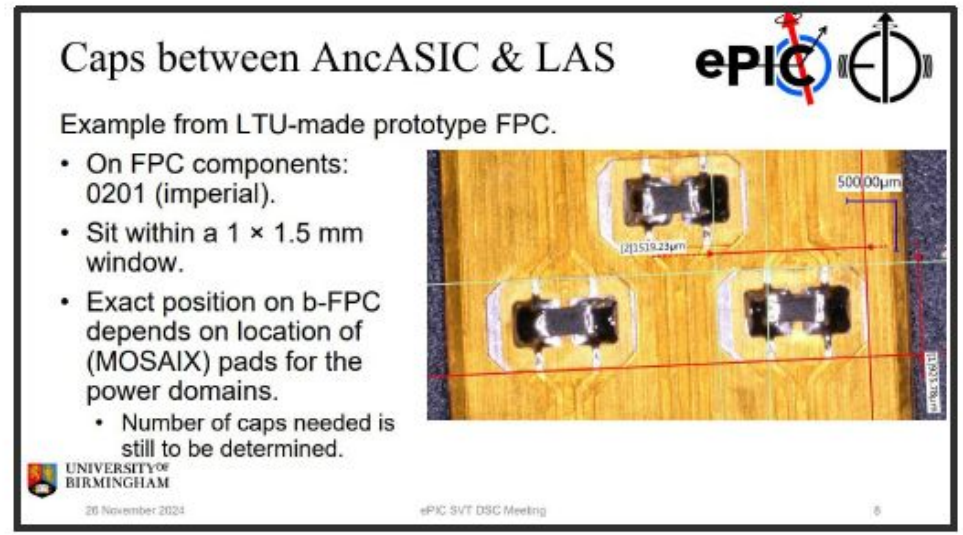
HS DATA

CTRL,CLK, ETC

LEC: 152 pads, size: 144*91 um2;

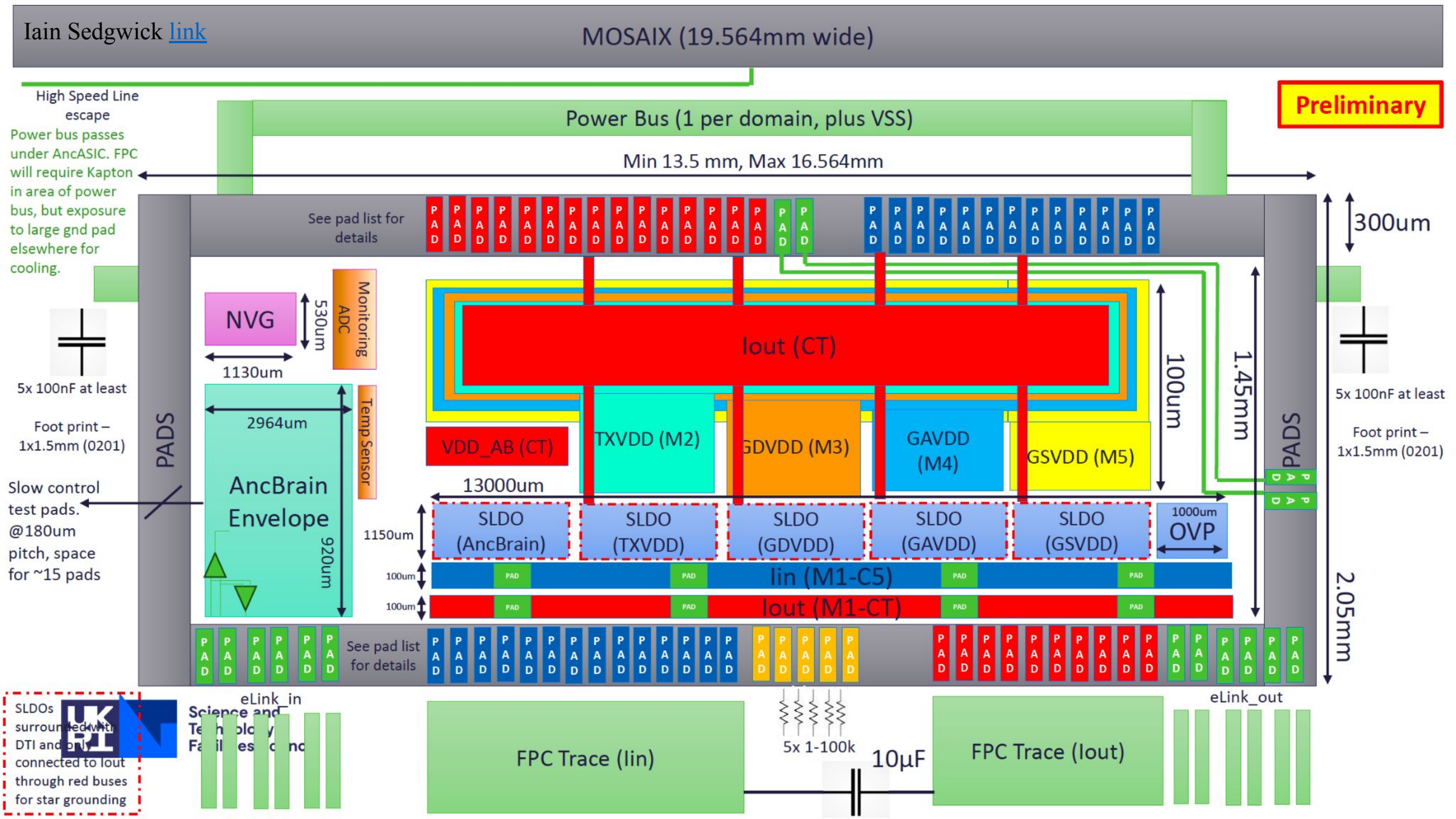
~ symmetric pad distribution:
1 to 76; 77 to 152;

Q: GSVSS, GAVSS, GDSS, TXVSS, PSUB have common ground?




Science and Technology Facilities Council

Iain Sedgwick [link]



# ePIC SVT Disk Architecture

**ePIC SVT - disk and barrel power and readout architecture**
Sichtermann, Glover, Silber

| Rev | Date | Author | Description |
|---|---|---|---|
| v1 | 2025-10-09 | Joe Silber (LBNL) | imported original diagram from Ernst, added details on sizes, counts, and connection interfaces |
| v2 | 2025-10-15 | Joe Silber (LBNL) | visual cleanup, approx dims on furcation tubes, power wire pairs, and CB-FIB ribbon |
| v3 | 2025-10-16 | Joe Silber (LBNL) | incorporated comments from Nikki on barrel vs disk variations; made MFPC and bridge connections more visually clear |
| vx | | | in-progress – added ref links |
| | | | |
| | | | |

**Nomenclature**

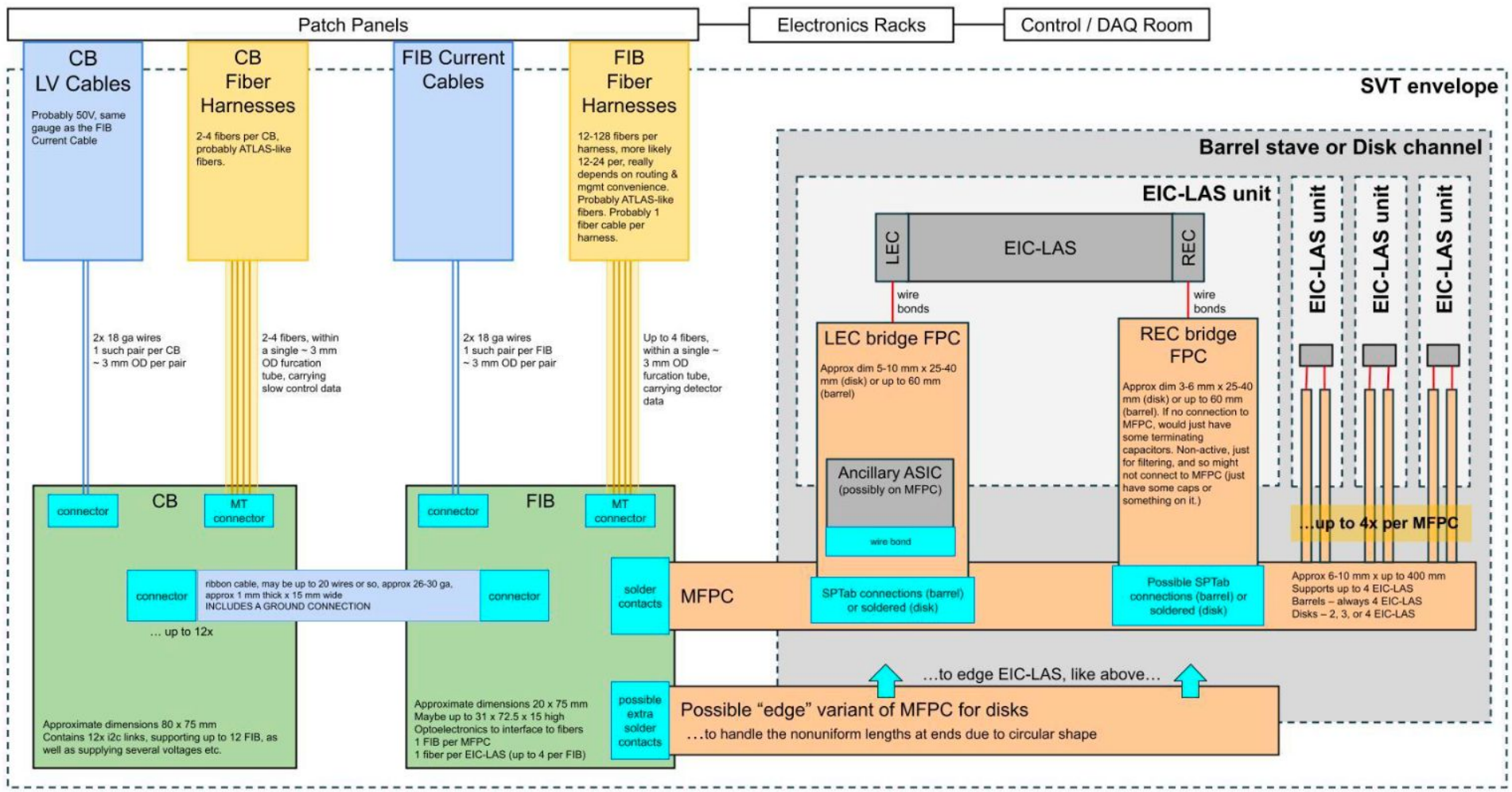
FPC … Flexible Printed Circuit
CB … Control Board
FIB … FPC Interface Board
LV … Low Voltage
MFPC … Main FPC
BFPC … Bridge FPC
SPTab … bonded overlapping Al/Kapton

**Notes**

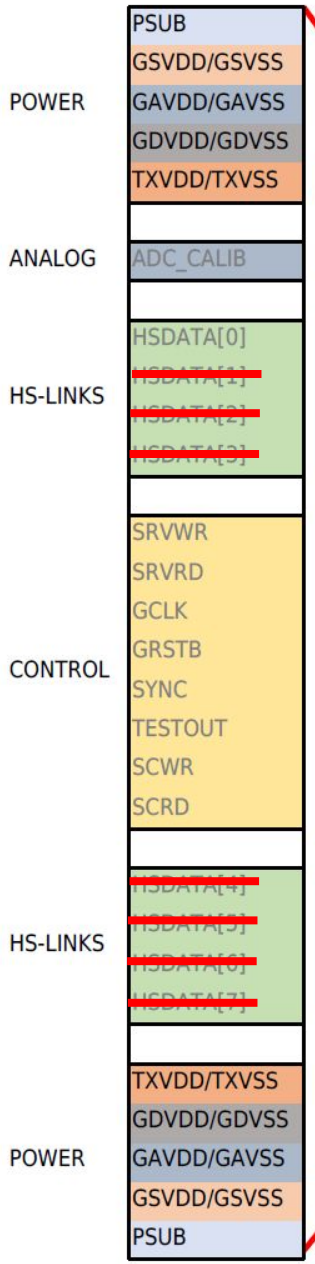
1. Not to scale.
2. Color-coding consistency not guaranteed.

**References**

1. module drawing from Nikki 2025-08-22

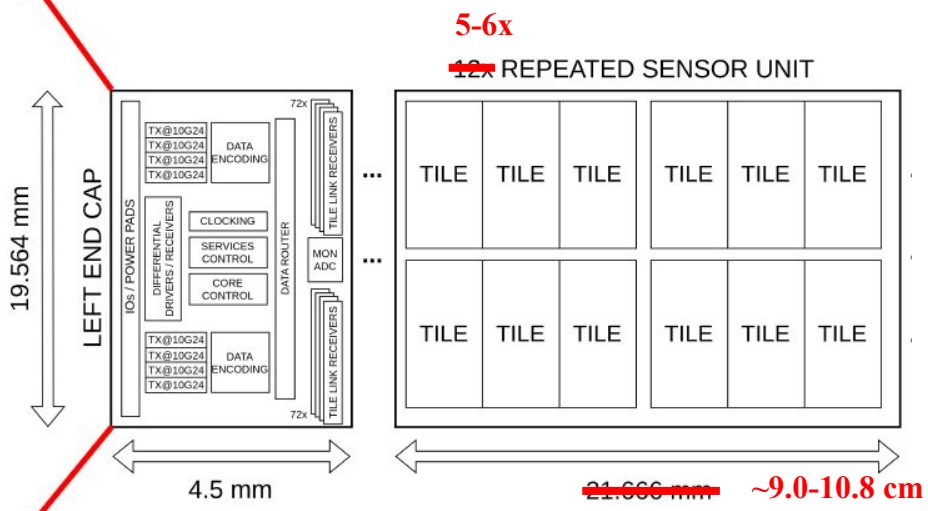


# EIC-LAS




| Supply | Typ (mA) | Max (mA) |
|---|---|---|
| PSUB (-1.2V) | | |
| GSVDD/GSVSS (1.32V/0V) | 40 | 60 |
| GAVDD/GSVSS (1.32V/0V) | 170 | 270 |
| GDVDD/GDVSS (1.32V/0V) | 526 | 816 |
| TXVDD/TXSVSS (1.2V/0V) | 200 | 300 |

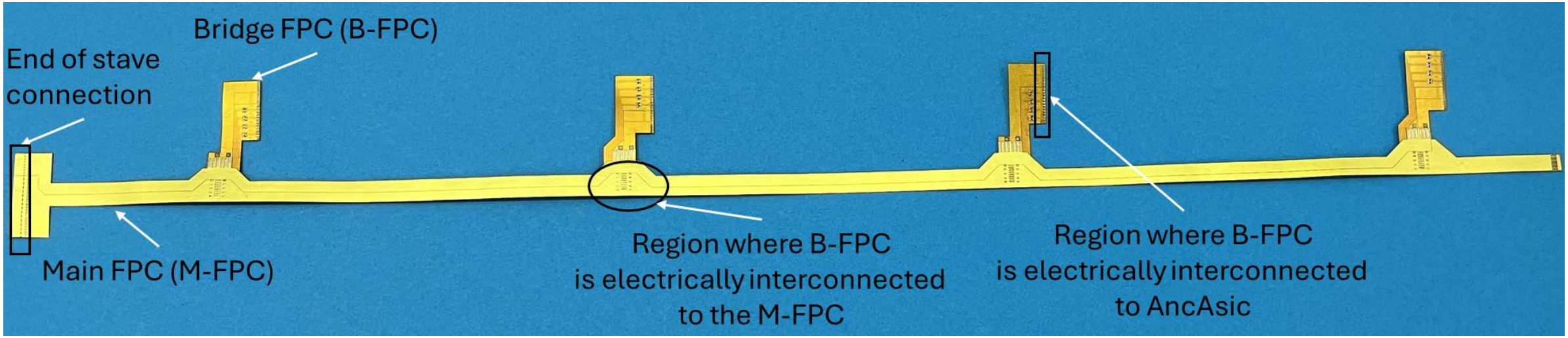
| Signal | Frequency |
|---|---|
| GCLK | 80/160 MHz |
| SYNC | N/A |
| GRSTB | N/A |
| SRVWR/RD | 5 Mbps |
| SCWR/RD | 5 Mbps |
| HSDATA[0…7] | 5.12/10.24 Gbps |




```
GSVDD/GSVSS  : Global Services domain (1.2V/0V), always-on, used for on-chip services
GAVDD/GAVSS  : Global Analog domain (1.2V/0V)
GDVDD/GDVSS  : Global Digital domain (1.2V/0V)
TXVDD/TXVSS  : Serializer domain (1.8V/0V), only used for serializers
PSUB         : Substrate bias (-1.2V .. 0V), used for substrate biasing
Control pads : Powered by the services domain
```

1.2V/0V

# STFC-LTU FPC Prototypes





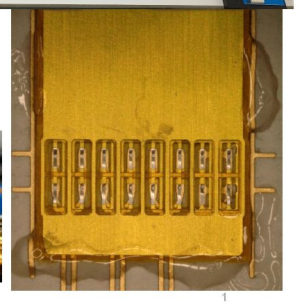
LTU FPC

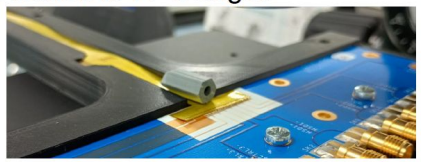
| Components | Thickness (um) | Material | X0(cm) | X0(%) |
|---|---|---|---|---|
| Metal layers | 15 + 15*0.69 | Aluminum | 8.897 | 0.028 |
| Dielectric | 10+10+25+25 | Polyimide | 28.57 | 0.023 |
| glue | 15 | TBC | 39.07 | 0.004 |
| Total | | | | 0.055 |

# spTAB vs wire-bonding on LTU FPCs


## M-FPC prototype 2

- New FPC installed using an update jig from Oxford.
- Nylon stand-offs used as weights to aid alignment of FPC.
- UV-cure glue-dots used to hold FPC flat and aligned during bonding.
- Additional glue added to FPC edges post-bonding.





Prototype 1 trials reported in March

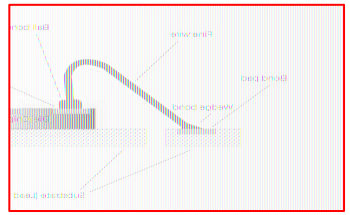


## Summary

- 2nd FPC prototype has been bonded.
- Bonded went well.
- No (obvious) damage seen from a visual inspection.
- Basic electrical continuity confirmed @ Birmingham
- Sent to Daresbury Lab for further testing.



James Julian Glover link



## Parameter matrix & 15 µm overtravel

Parameter Matrix

| | Glued on PCB | | | Thicker Diffuser | | | Thinner Diffuser | | | Glued on PCB | | | Thicker Diffuser | | | Thinner Diffuser | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Single Layer | | | Single Layer | | | Single Layer | | | Multi Layer | | | Multi Layer | | | Multi Layer | | |
| Parameters | No of Wires | Mean | Std Dev | No of Wires | Mean | Std Dev | No of Wires | Mean | Std Dev | No of Wires | Mean | Std Dev | No of Wires | Mean | Std Dev | No of Wires | Mean | Std Dev |
| 22US% 22CN | 20 | 11.18 | 0.69 | 17 | 7.3 | 1.18 | 17 | 9.88 | 1.63 | 19 | 10.73 | 1.77 | 19 | 11.11 | 2.24 | 15 | 11.65 | 0.49 |
| 25US% 22CN | 20 | 11.46 | 0.18 | 17 | 6.83 | 1.79 | 18 | 10.83 | 1.4 | 20 | 10.45 | 1.32 | 20 | 11.78 | 0.43 | 20 | 12.12 | 0.34 |
| 25US% 25CN | 19 | 11.26 | 0.59 | Failed | | | 20 | 8.53 | 1.61 | 19 | 11.04 | 0.67 | 20 | 11.1 | 0.79 | 20 | 11.95 | 0.47 |
| 28US% 25CN | 20 | 11.21 | 0.62 | | | | 20 | 9.74 | 2.15 | 19 | 11.03 | 0.25 | 20 | 11.95 | 0.34 | 20 | 11.96 | 0.73 |
| 28US% 28CN | 20 | 11.33 | 0.36 | | | | 12 | 6.61 | 1.84 | 20 | 11.04 | 0.88 | 20 | 11.11 | 1.09 | 20 | 11.77 | 1 |
| 36US% 28CN | 20 | 11.04 | 0.8 | | | | 17 | 7.96 | 2.94 | 20 | 11.06 | 0.69 | 20 | 11.87 | 0.53 | 20 | 11.43 | 1.41 |
| 36US% 30CN | 16 | 10.49 | 0.82 | | | | 17 | 5.89 | 2.1 | 20 | 11.03 | 0.49 | 20 | 11.87 | 0.68 | 20 | 10.99 | 1.38 |
| 32US% 30CN | 20 | 10.96 | 0.65 | | | | 13 | 5.66 | 1.95 | 20 | 10.8 | 0.82 | 20 | 12.07 | 0.58 | 20 | 12.16 | 0.75 |
| 32US% 32CN | 20 | 10.66 | 0.77 | | | | 6 | 5.68 | 1.32 | 20 | 9.45 | 1.2 | 20 | 11.18 | 1.39 | 20 | 11.04 | 1.99 |

15 µm Overtravel

| | Glued on PCB | | | Thicker Diffuser | | | Thinner Diffuser | | | Glued on PCB | | | Thicker Diffuser | | | Thinner Diffuser | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Single Layer | | | Single Layer | | | Single Layer | | | Multi Layer | | | Multi Layer | | | Multi Layer | | |
| Parameters | No of Wires | Mean | Std Dev | No of Wires | Mean | Std Dev | No of Wires | Mean | Std Dev | No of Wires | Mean | Std Dev | No of Wires | Mean | Std Dev | No of Wires | Mean | Std Dev |
| 25US% 22CN | 20 | 11.21 | 0.47 | Failed | | | 18 | 10.67 | 1.03 | 20 | 11.48 | 0.45 | 17 | 11.27 | 1.19 | 19 | 11.99 | 0.86 |
| 25US% 25CN | 20 | 10.89 | 0.88 | 20 | 8.09 | 1.69 | 20 | 9.42 | 1.45 | 20 | 10.96 | 1.09 | 20 | 11.93 | 0.22 | 20 | 10.63 | 1.55 |
| 28US% 25CN | 20 | 11.34 | 0.39 | 18 | 8.97 | 1.1 | 17 | 9.24 | 2.1 | 20 | 11.34 | 0.65 | 20 | 11.94 | 0.63 | 20 | 12.06 | 0.55 |
| 28US% 28CN | 20 | 10.79 | 0.94 | 11 | 3.8 | 1.09 | 15 | 8.27 | 1.54 | 20 | 11.09 | 0.43 | 17 | 10.96 | 1.58 | 20 | 11.89 | 0.9 |
| 36US% 28CN | 20 | 11.06 | 0.82 | Failed | | | 15 | 8.58 | 2.33 | 19 | 11.09 | 0.64 | Failed | | | 20 | 11.23 | 1.28 |
| 36US% 30CN | 20 | 11.3 | 0.65 | | | | Failed | | | 18 | 10.82 | 0.76 | | | | 17 | 9.4 | 1.57 |
| 32US% 30CN | 20 | 11.25 | 0.38 | | | | | | | 20 | 11.08 | 0.66 | | | | 11 | 10.74 | 1.33 |



## Summary

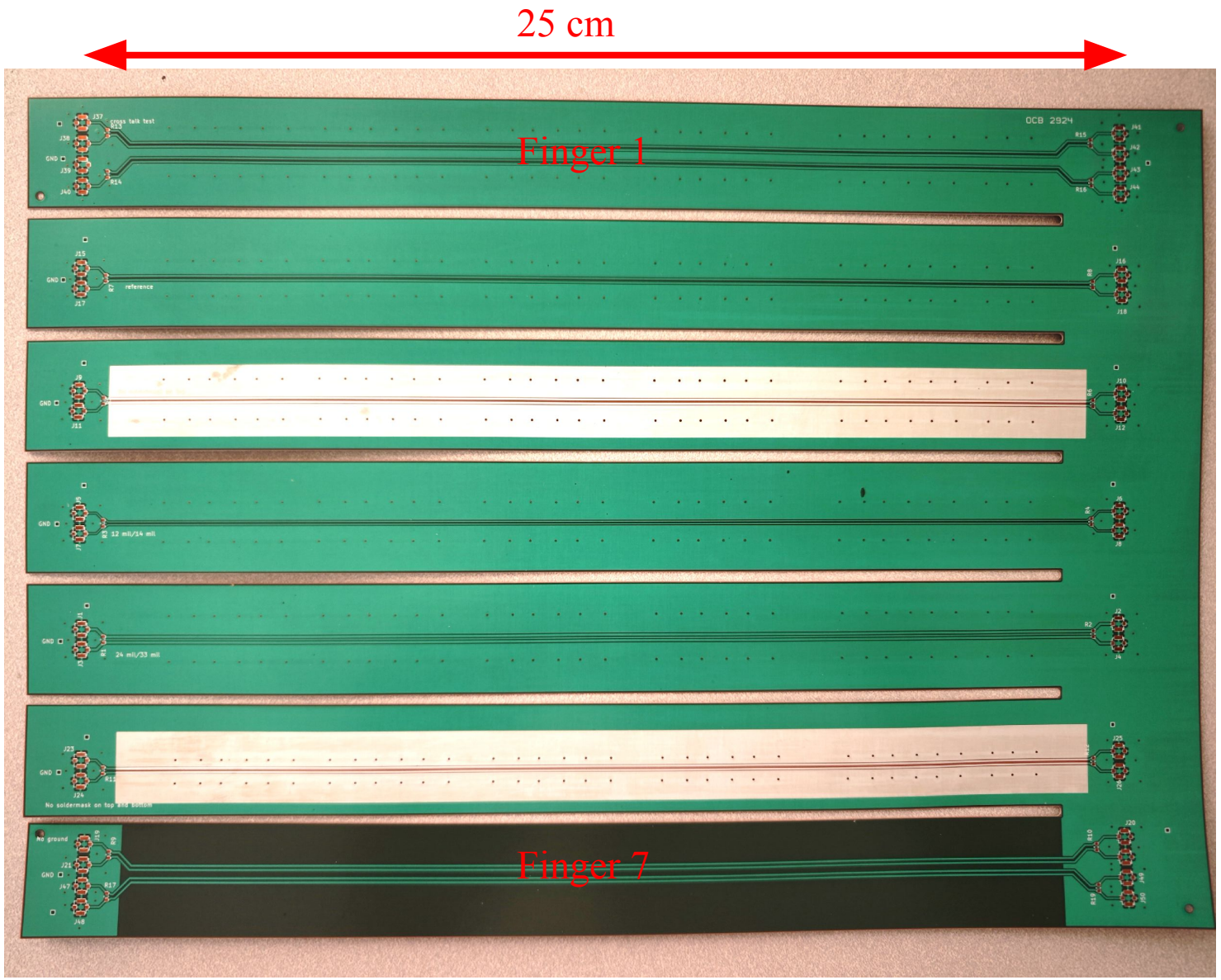
- Bonding quality was superior when foils were glued to a PCB, likely due to the added mechanical stability
- The thinner diffuser significantly improved vacuum-assisted bonding, though some stability challenges remain
- Multi-layer foils consistently offered easier and more reliable bonding, regardless of method
- The study demonstrated that acceptable mean strength and standard deviation values can be achieved

- Next steps:
  - Investigate further improvements for single-layer foils under vacuum. Any suggestions are welcome
    - Consider adjusting touchdown force or tail length
  - Plan comparative tests with alternative wire materials



Jian Liu link

# LBL-OMNI FPC Prototypes



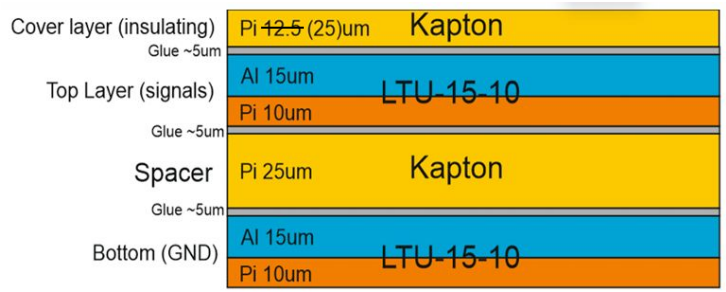

**12 FPCs, 2 for each of the following:**

- Different metals: Al, Cu
- Different dielectric: FR4, polyimide, EM 528K

**Each FPC has 7 fingers with different layouts:**

1. 2 pairs of differential lines with GND
2. 1 pair of differential line with width/space of 18mil/22mil
3. No soldermask on top
4. 12 mil/14 mil
5. 24 mil/33mil
6. No soldermask on top or bottom
7. 2 pairs of differential lines without GND on top

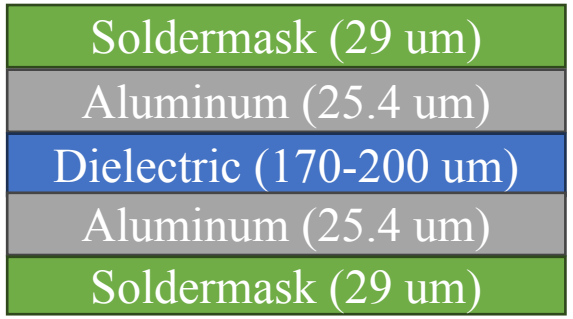
# OMNI




Fraction 69%

Fraction 100 %

Cross section of LTU FPC




Top (Signals), Fraction74%

Bottom (GND), Fraction 100%

Cross section of OMNI

| | LTU FPC | | | | OMNI FPC in 2nd set | | | |
|---|---|---|---|---|---|---|---|---|
| Components | Thickness (um) | Material | X0(cm) | X0(%) | Thickness (um) | Material | X0(cm) | X0(%) |
| Metal layers | 15 + 15*0.69 | Aluminum | 8.897 | 0.028 | 25.4+25.4*0.74 | Aluminum | 8.897 | 0.05 |
| Dielectric | 10+10+25+25 | Polyimide | 28.57 | 0.023 | 58 + (170~200) | Soldermask Ink + Arlon 528K | 28.57 | 0.08~0.09 |
| glue | 15 | TBC | 39.07 | 0.004 | | | | |
| Total | | | | 0.055 | | | | 0.13-0.14 |

The average material budget over the full area of a module/stave/disk may be within specs

# LTU

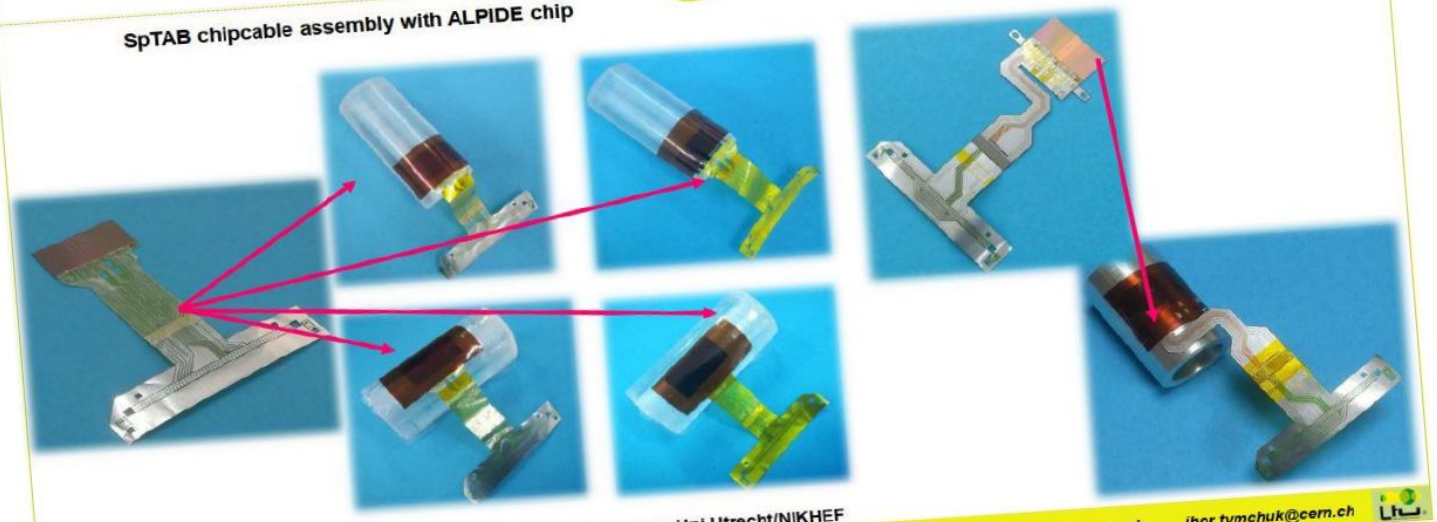


## 3-D (volumetric) approach realized by LTU's FPCs: ALICE ITS3 prototypes

18

SpTAB chipcable assembly with ALPIDE chip

SpTAB single-ALPIDE prototype



Note: activity performed in close cooperation with CERN, Uni Bergen, Uni Utrecht/NIKHEF

viatcheslav.borshchov@cern.ch, ihor.tymchuk@cern.ch



### 4.8.3 Fall-back options

#### Sp-TAB technique

The Single-point Tape Automated Bonding (SpTAB) technique has been considered as an alternative option to interconnect the ITS3. The main features of this technique and approach are:

- adhesiveless aluminum-polyimide thin single-layered and multi-layered flexible printed circuits to interconnect the chip to the external data and power transmission buses,
- conductive aluminum layer thicknesses ranging from 15 to 100 µm to realize low-mass interconnection elements;
- SpTAB direct connections of ribbon aluminium leads to chip pads providing uniform, highly reliable and mechanically stable monometallic joints;
- welded joint encapsulation after SpTAB;
- possibility to perform quick repair weld joints during manufacture of the pixel module;
- possibility of using standard industrial automated equipment for basic assembly processes (welding, gluing and encapsulating welded joints).

The SpTAB technique allows interconnection of the curved chip to the flexible circuit as well as for bending the pre-interconnected assembly. Using thin single layered circuits for sensor-to-bus interconnections allows electrical functional testing to be performed before final mounting on support structures or further assembly. The approach described has been used to create and characterise single-chip test assemblies using ALPIDE chips (see Fig. 4.59). In order to

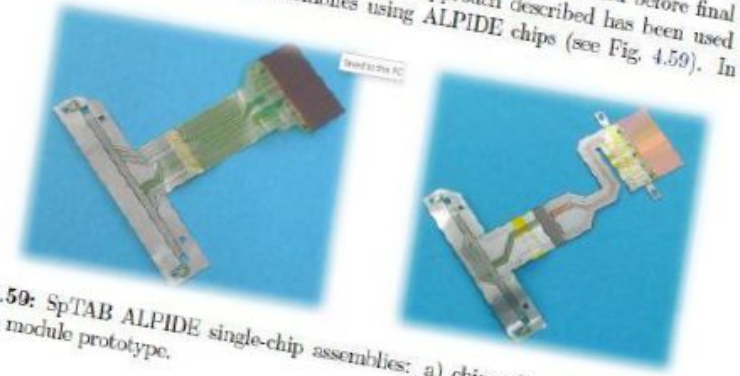
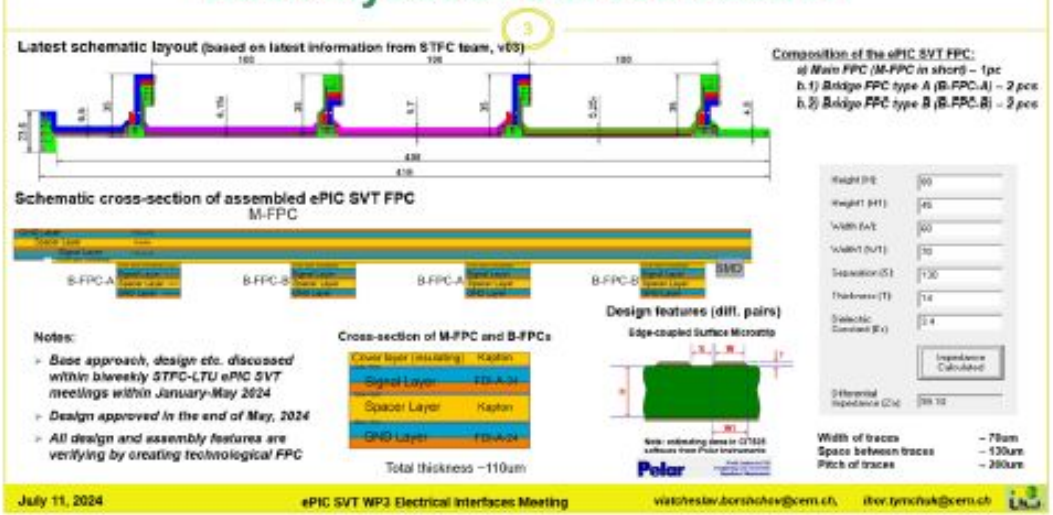


**Figure 4.59:** SpTAB ALPIDE single-chip assemblies: a) chip cable with chip assembly; b) single-chip module prototype.

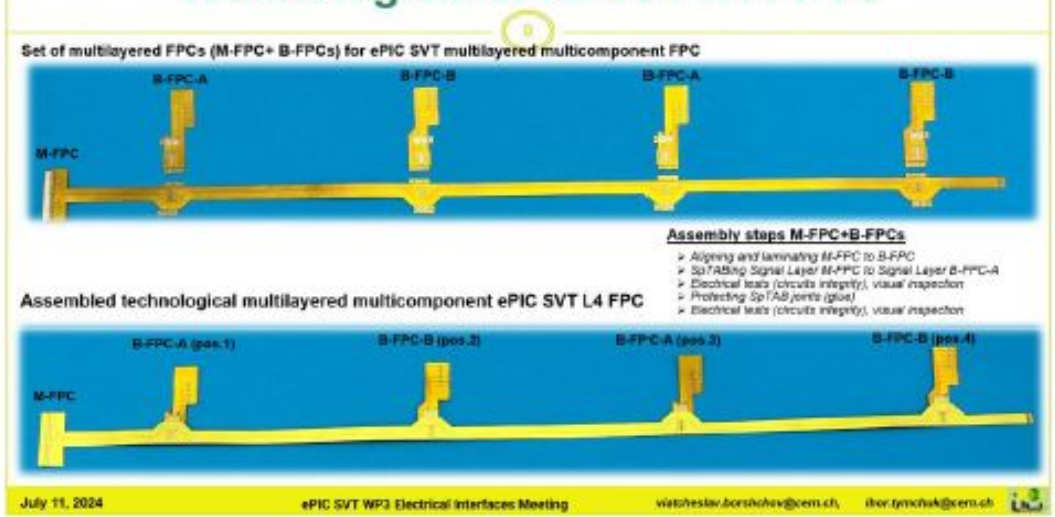
# Base approach and features (reminder)



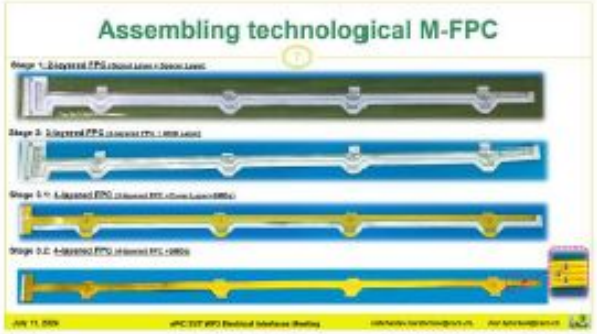
## Base layout and cross-section



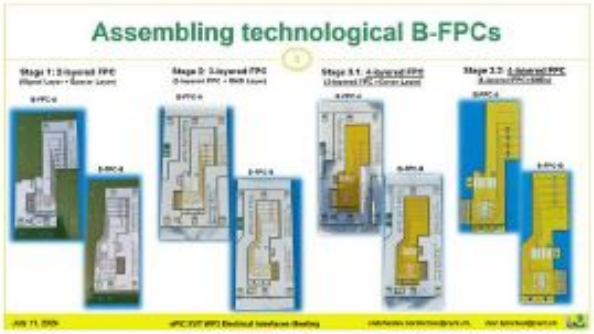

## Technological ePIC SVT L4 FPCs




## Assembling technological M-FPC

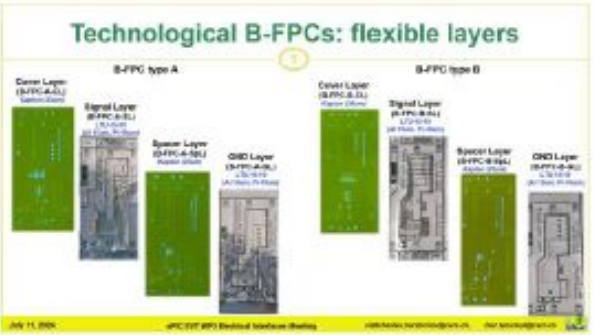


## Assembling technological B-FPCs



## Technological M-FPC: flexible layers

## Technological B-FPCs: flexible layers



# OMNI vs LTU



**Pros:**

- OMNI can add small pieces of copper at the soldering positions on the FPC, making soldering possible;
- OMNI supports vias between different layers of the FPC
- 10.24Gbps IBERT test results from prototype produced by OMNI at a length of 25 cm are promising;

**Cons:**

- Dielectric (Al) thickness is around 230-260 (25.4) um, in comparison to LTU's 70 (15) um, leading to 0.13~0.14% $X_0$ compared to LTU 0.055% $X_0$;
- The minimum trace width and space are 152.4/152.4 um, which are larger than LTU's (70 um/130 um);
- The prototypes received so far are not very flexible, and may break when bent to a radius of 4 mm.
- Can't do spTAB

# Material Budget



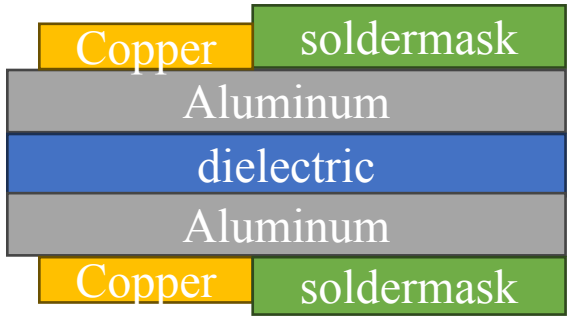



Table : Structure of EM 528K Al-FPC

| Layer | Material | Thickness [um] | X0 [cm] | Fraction | X0(%) |
|---|---|---|---|---|---|
| Soldermask | Not sure | 29.2 | 28.57 (TBC) | 0.995 | 0.0102 |
| Copper | Copper | 29.2 | 1.436 | 0.005 | 0.0010 |
| Aluminum | Aluminum | 25.4 | 8.897 | 0.97 | 0.0277 |
| Dielectric | **EM 528K** | 175.3 | 28.57 (TBC) | 1 | 0.0613 |
| Aluminum | Aluminum | 25.4 | 8.897 | 0.97 | 0.0277 |
| Copper | Copper | 29.2 | 1.436 | 0.005 | 0.0010 |
| soldermask | Not Sure | 29.2 | 28.57 (TBC) | 0.995 | 0.0102 |
| | | | | | 0.1392 |

The parameters of soldermask and EM 528K are considered as Isola.
The estimated material budget of EM528K,FR4 and Isola are 0.1392%, 0.1876% and 0.1574%, respectively.