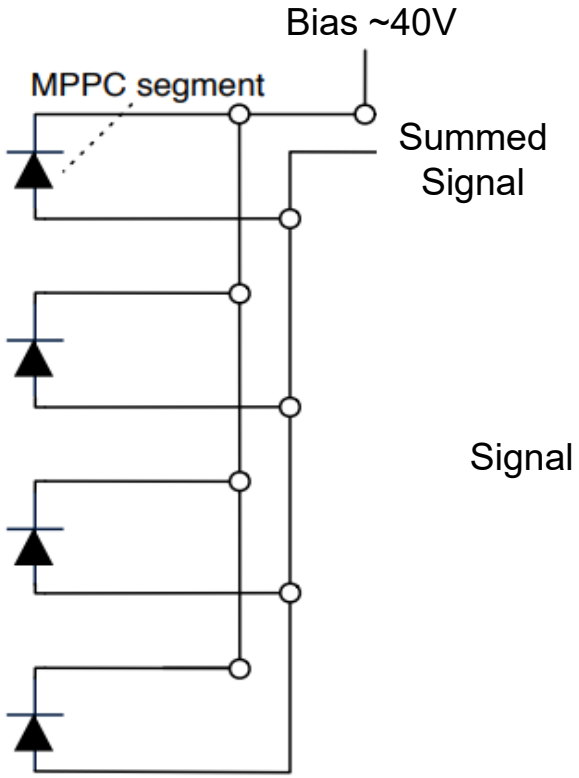
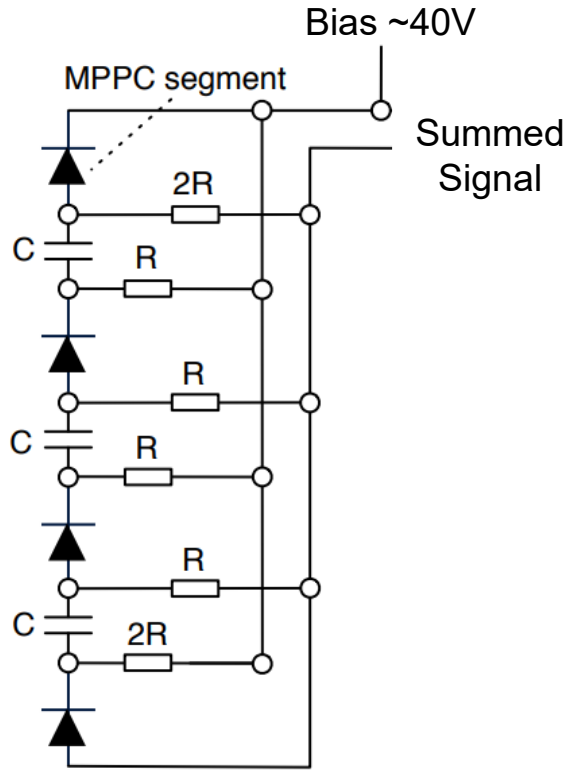
Signal summation: Parallel vs Hybrid



(a) Parallel

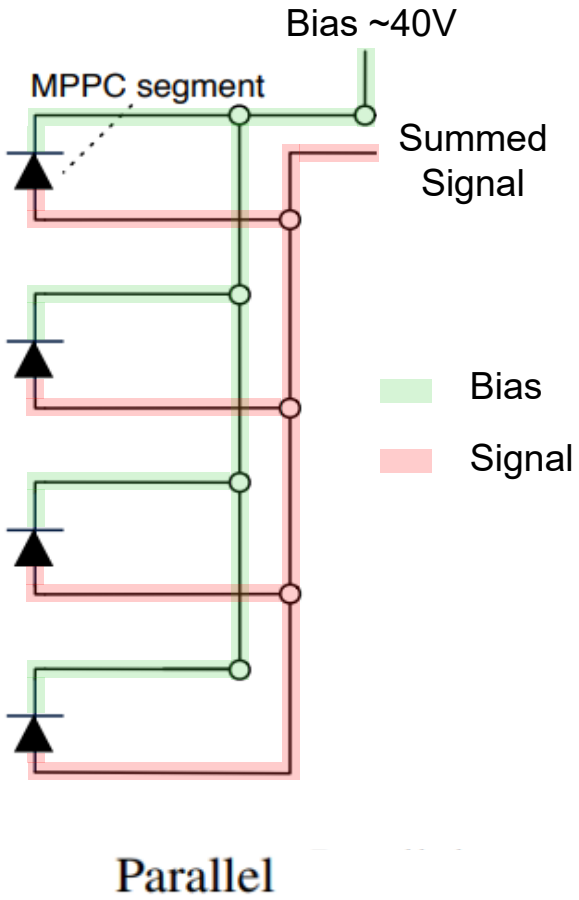
- **Broader pulse** due to added SiPM capacitance



(c) Hybrid

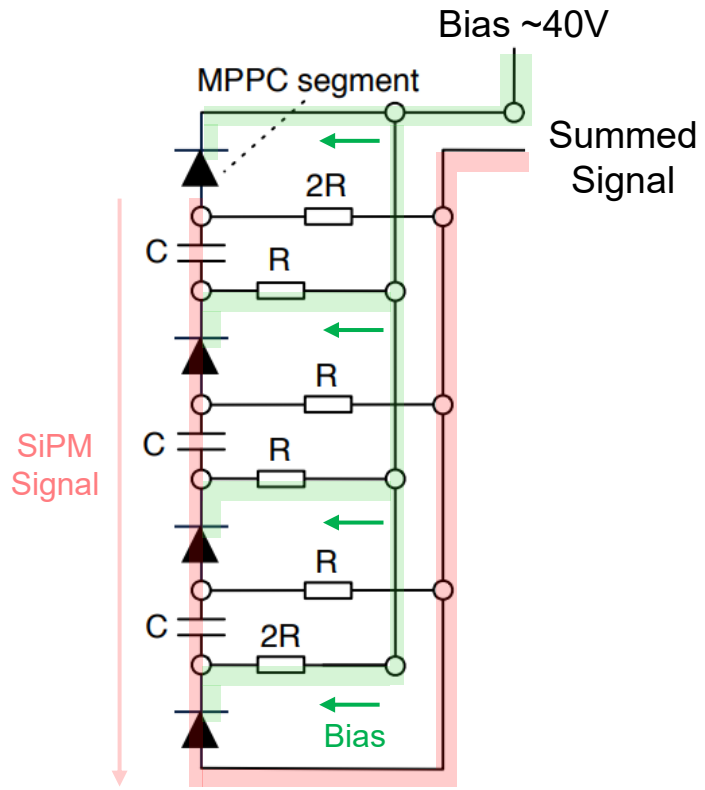
- Bias is applied in parallel, while signals are summed in series
- Narrower than parallel, but **large channel-to-channel amplitude variation**

Signal summation: Parallel vs Hybrid



Parallel

- **Broader pulse** due to added SiPM capacitance

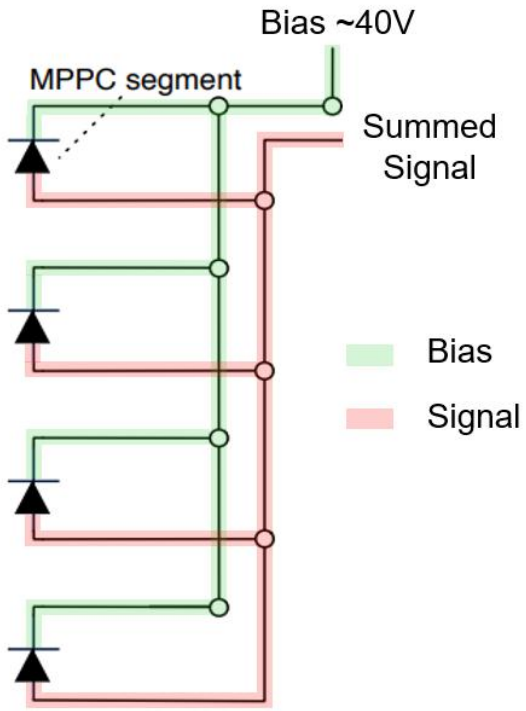


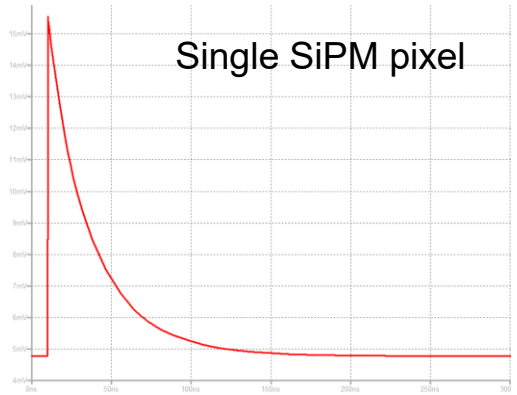
Hybrid

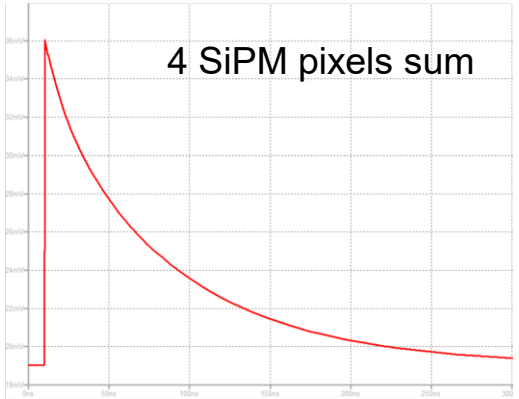
- Bias is applied in parallel, while signals are summed in series
- Narrower than parallel, but **large channel-to-channel amplitude variation**

Parallel vs Hybrid: Simulation

Parallel summation

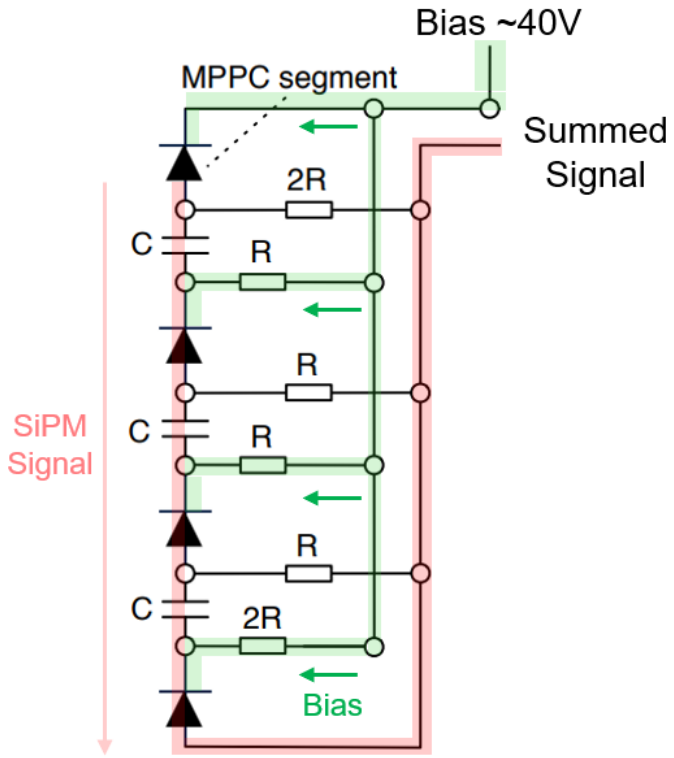


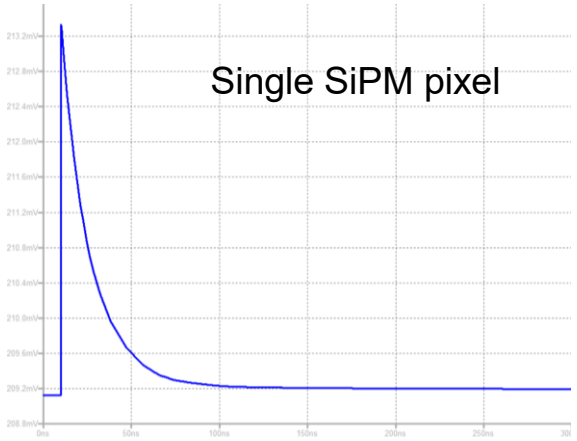


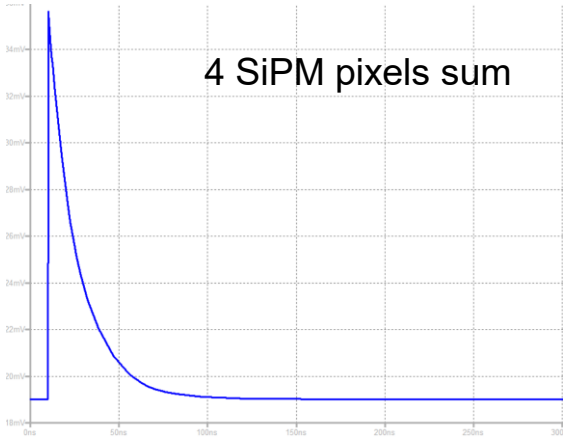


Parallel capacitance → **Broader** pulse

Hybrid summation

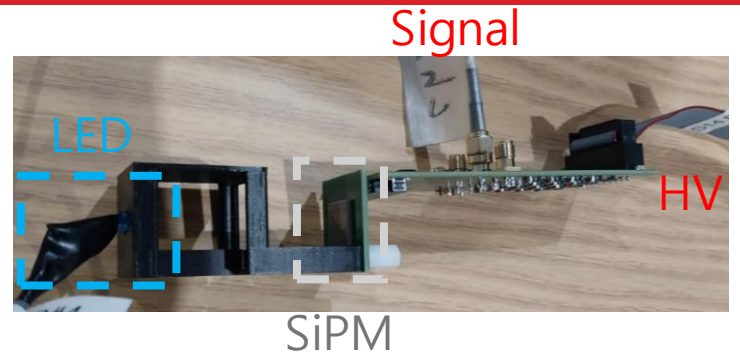






Testing on real hardware

Setup



Shortage of H2GCROC boards leading to insufficient SiPM HV channels

→ use DAC to add ΔV to a common HV

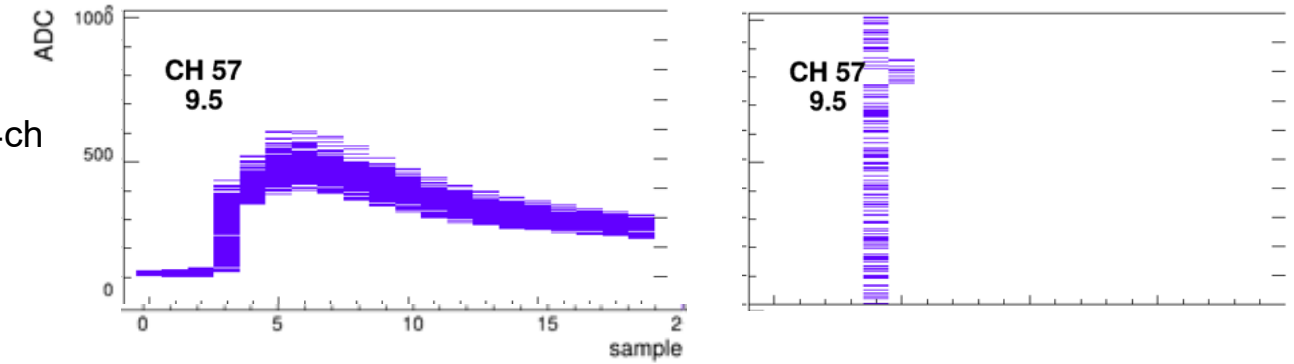
→ bias 16 SiPM channels with a **single HV channel** from the power module

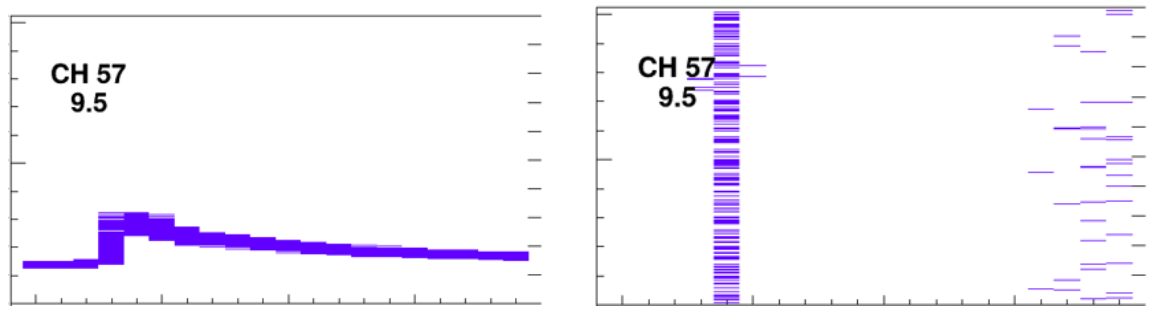
Board test

Parallel

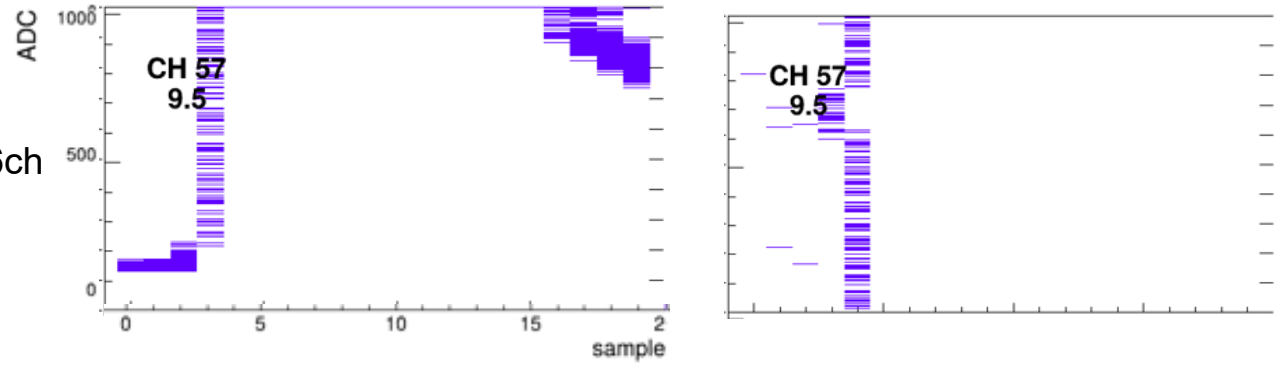
Hybrid

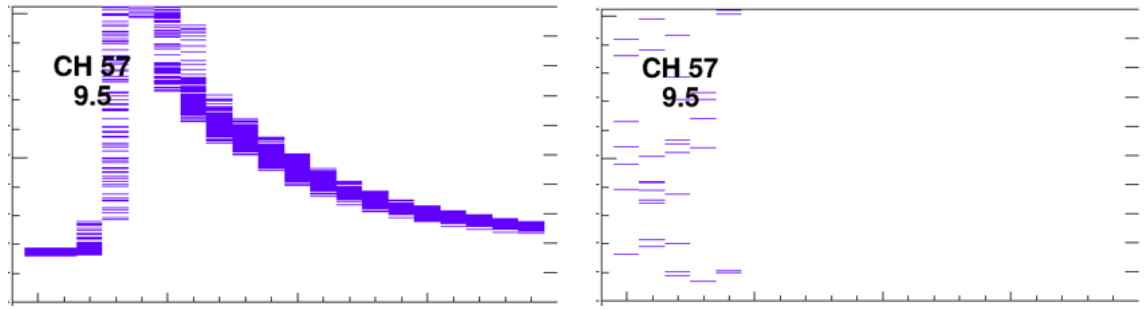
4ch





16ch





- Hybrid has a narrower signal width
- However, what issues arise from smaller signals and large channel-to-channel gain variations?