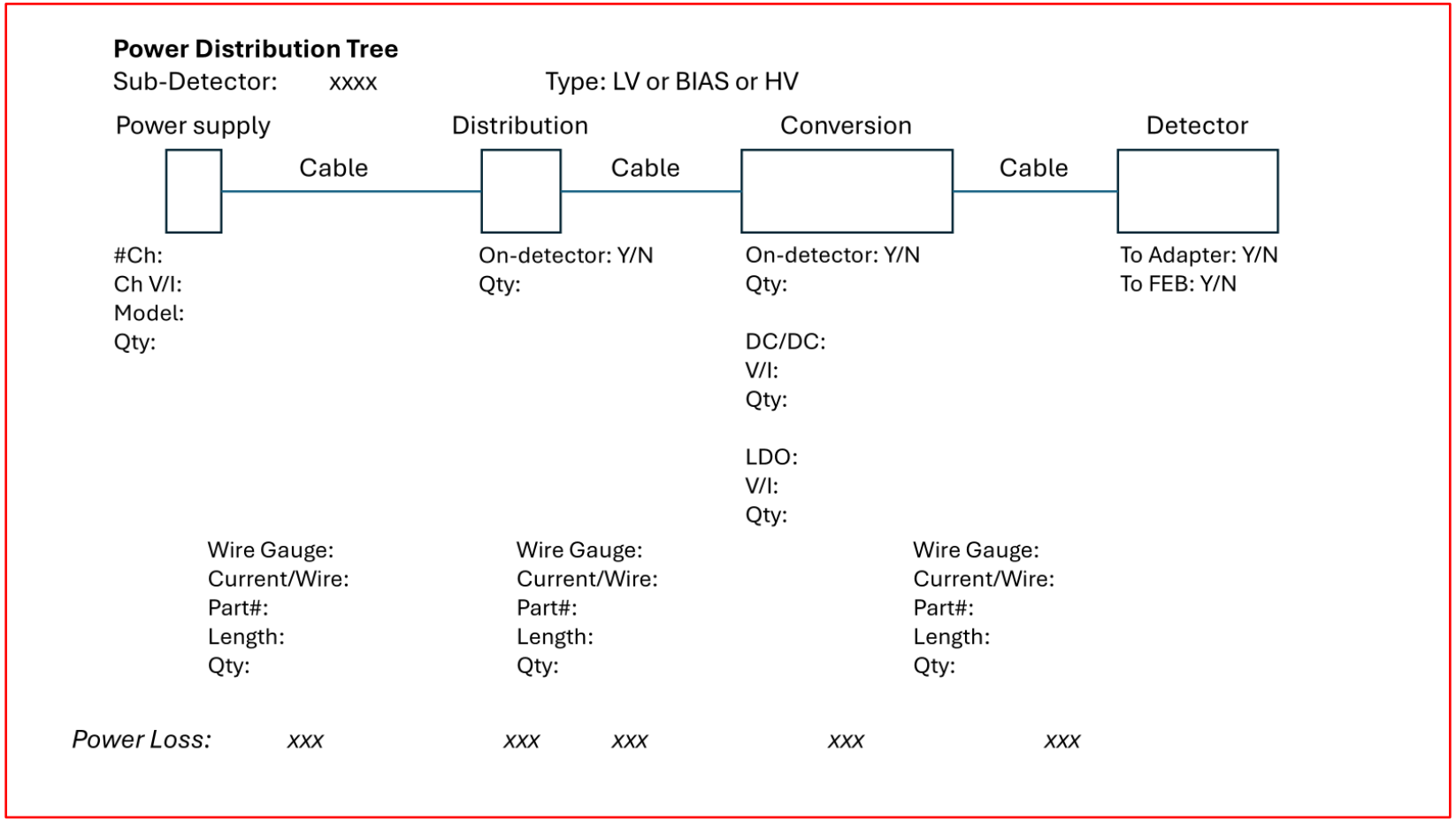
Power scheme for pfRICH

Takao for Raymond and Alexander

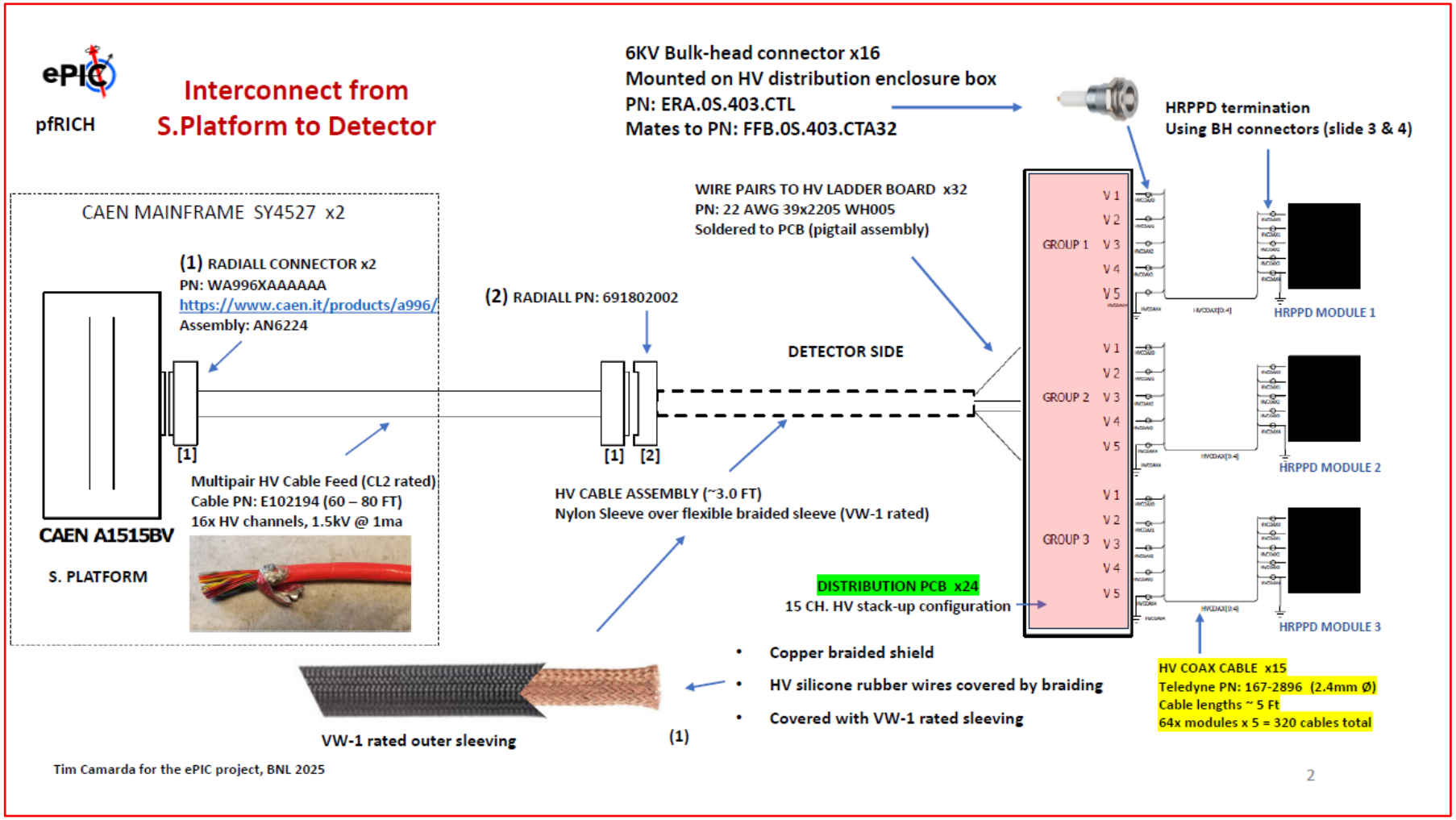
Power distribution info requested

- Template provided by Fernando



HV side

- Tim's design on the HV system



Power Distribution Tree

Sub-Detector: pfRICH Type: HV

#Ch: 340 (=5*68)
Ch V/I: 0.2mA
Model: CAEN A1515BV
Qty: 23

On-detector: Y/N
Custom board
Qty: 23

To Adapter: Y/N
To FEB: Y/N
To: Backplane

- ~200mW per HRPPD module
- ~14W for whole pfRICH

Wire Gauge: 15 pairs of 26
Current/Wire: 0.2mA (for two wires, others are zero)
Part#: E102194
Length: 80 ft
Qty: 23

Wire Gauge: 68 * 5 of 26
Current/Wire: 0.1mA (for two wires, others are zero)
Part#: 167-2896
Length: 5ft
Qty: 340

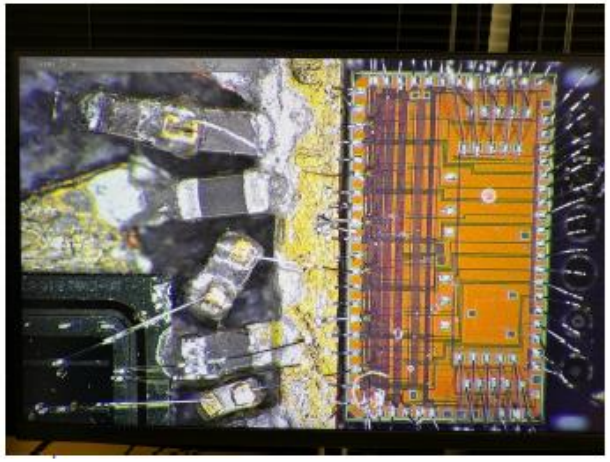
Power Loss: $3.6 * 1.0^{-5} W$ *$2.3 * 1.0^{-6} W$* *xxx* *xxx*

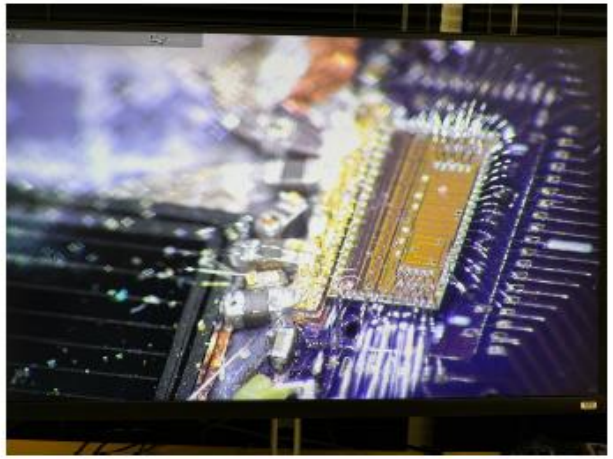
FCFD chip for readout ASIC

The current chip has 6 channels of Analog-amp and CFD output (No ADC/TDC)

Test board (left) and chips (right) to be wire-bonded at the IO at BNL.

Picture of FCFD chips from Artur (FNAL)





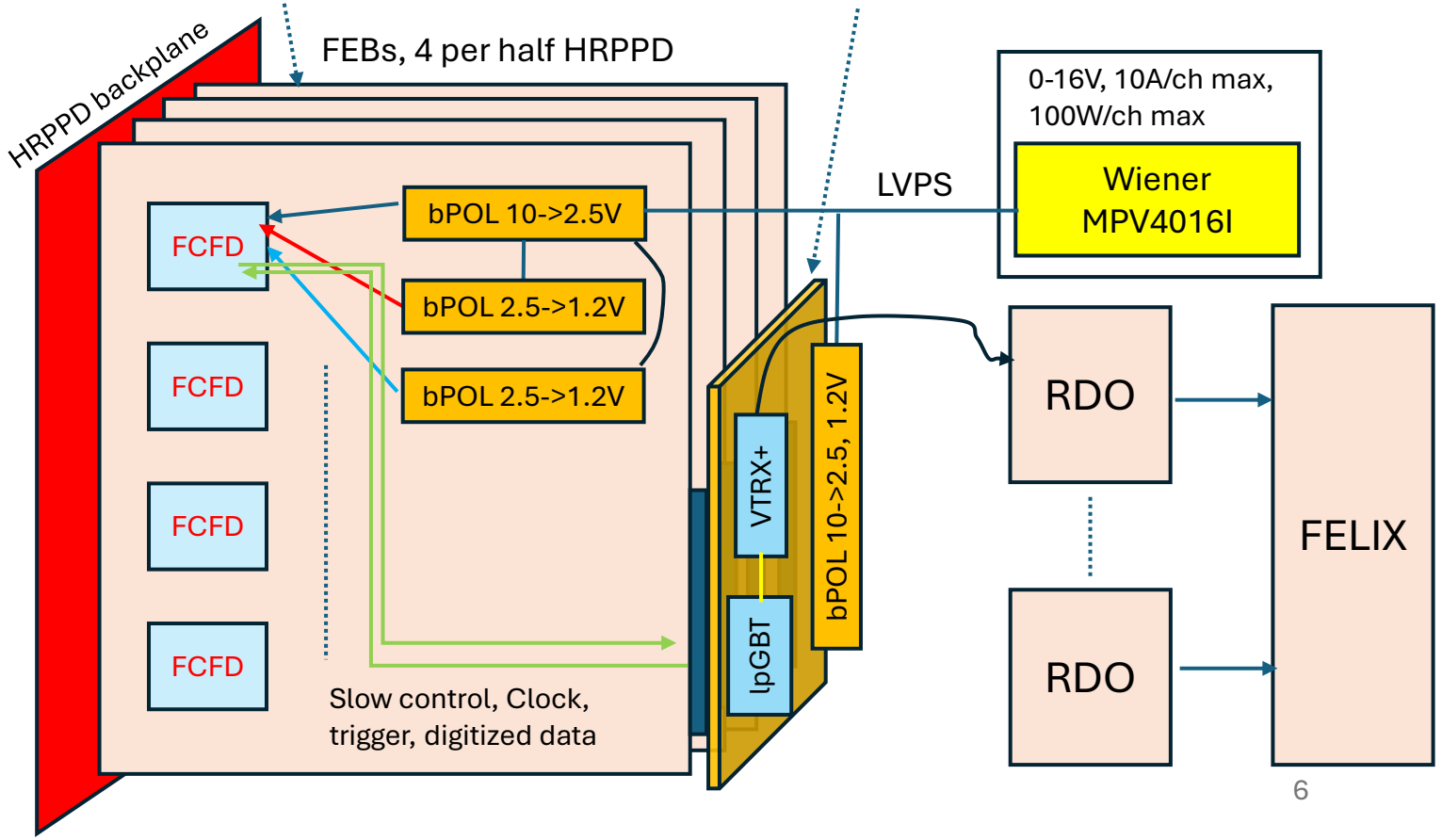
Possible readout scheme and LV power-dist

bPOL12 and bPOL2V5 efficiencies are uniformly applied to get total, which is obviously overestimate

- MPV4016I (Wiener) : 4ch per module. 0-16V output, 100W/ch max, 10A max.
  - 2.1*8+1.6*2=23 W per HRPPD module.
  - Three HRPPD modules can share a PS channel (consistent with HV granularity).
  - Some bPOLs (DC-DC) may be replaced with LDOs.
  - I_{max}: 4A for bPOL12 and 3A for bPOL2V5.
- Current designed FDFC and FEB idea
  - 32ch input, 100fC max. ADC/TDC: 5 bits
  - Assuming 4 FDFCs on a FEB (TBD)
  - 320Mbps data rate (one e-link)
  - elinks can be daisy-chained over chips
- Father board (FB) with a set of lpGBT and VTRX+ can handle four FEBs
  - Alexander showed this plan already in the collaboration meeting in 2023.
- Bandwidth of lpGBT+VTRX+
  - Max rate for lpGBT with FEC10 encoding is 7.68Gbps. With FEC5: 8.96Gbps
  - 4 FEB (half HRPPD): ~100MHz (BC) * 512 ch * 10bits (ADC+TDC) * 1% = 5.12 Gbps

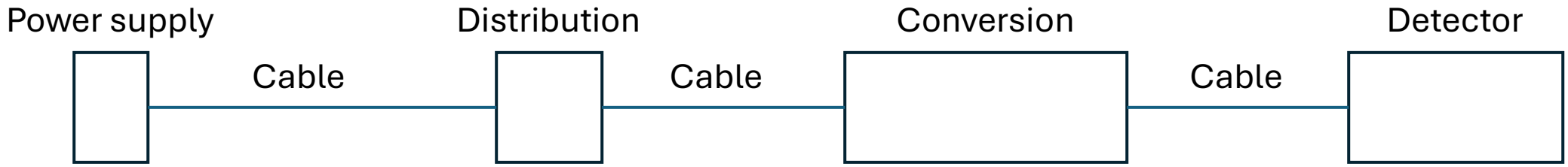
Parts	Per unit	QTY
FCFD	330mW	4
bPOL12	~75% eff	1 per line
bPOL2V5	~86% eff	1 per line
Total	~2.1W	per FEB

Parts	Per unit	QTY
lpGBT	750mW	1
VTRX+	300mW	1
bPOL12, 2V5	~75%,~86% eff	1 per line
Total	~1.6W	Per FB



Power Distribution Tree

Sub-Detector: pfRICH Type: LV



#Ch: 4
Ch V/I: 12V/10A
Model: Wiener MPV4016I
Qty: 6

On-detector: Y/N
Qty:68
12AWG to pigtail

On-detector: Y/N
Qty: same as FEB

DC/DC: bPOL12, 2V5
V/I: 2.5, 1.2
Qty: 1768

LDO: N/A

To Adapter: Y/N
To FEB: Y/N

Work in progress

Wire Gauge: 12AWG?
Current/Wire: 3A
Part#:
Length: 80ft
Qty: 68

Wire Gauge: Pigtail (20AWG?)
Current/Wire: 0.25A?
Part#:
Length: 5ft
Qty: 680

Wire Gauge:
Current/Wire:
Part#:
Length:
Qty:

Power Loss: *xxx* *xxx* *xxx* *xxx* *xxx*

Plan and TODO (Random list)

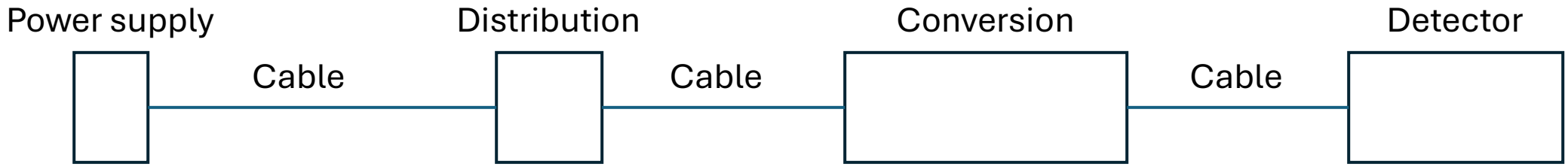
- Must check items for FCFD-variant chip design
  - What is max Q?
    - e.g. 2 p.e. & $5*10^6$ gain =1.6pC
  - ADC/TDC 5bits enough?
  - Is the occupancy about 1%?
    - 320Mbps data link from a FCFD needs the occupancy lower than 1%
    - 32ch * 10 bits *100MHz * 1% occupancy = 320Mbps (without header)
  - Do we want wire-bonding type package, or BGA?
    - BGA should be much easier to deal with. We could ask this.

- TODO for next months
  - Get FDFC cards ready for CERN beam test. (one or two cards)
  - Readout scheme should be fixed soon
    - Make a list of custom parts (ASICs, bPOL, lpGBT, VTRX+) and their QTY needed for pfRICH.
    - This is rather urgent.
  - Make sure that we ask for enough LV modules.
  - Make mock-up of the FEBs/FB and cabling, to figure out if we can integrate them by hands.
  - Make initial cooling scheme for FEBs/FB
  - Make sure that we get HV cables with round connectors from sPHENIX (as long as possible)

Backup

Power Distribution Tree

Sub-Detector: xxxx Type: LV or BIAS or HV



#Ch:
Ch V/I:
Model:
Qty:

On-detector: Y/N
Qty:

On-detector: Y/N
Qty:

DC/DC:
V/I:
Qty:

LDO:
V/I:
Qty:

To Adapter: Y/N
To FEB: Y/N

Wire Gauge:
Current/Wire:
Part#:
Length:
Qty:

Wire Gauge:
Current/Wire:
Part#:
Length:
Qty:

Wire Gauge:
Current/Wire:
Part#:
Length:
Qty:

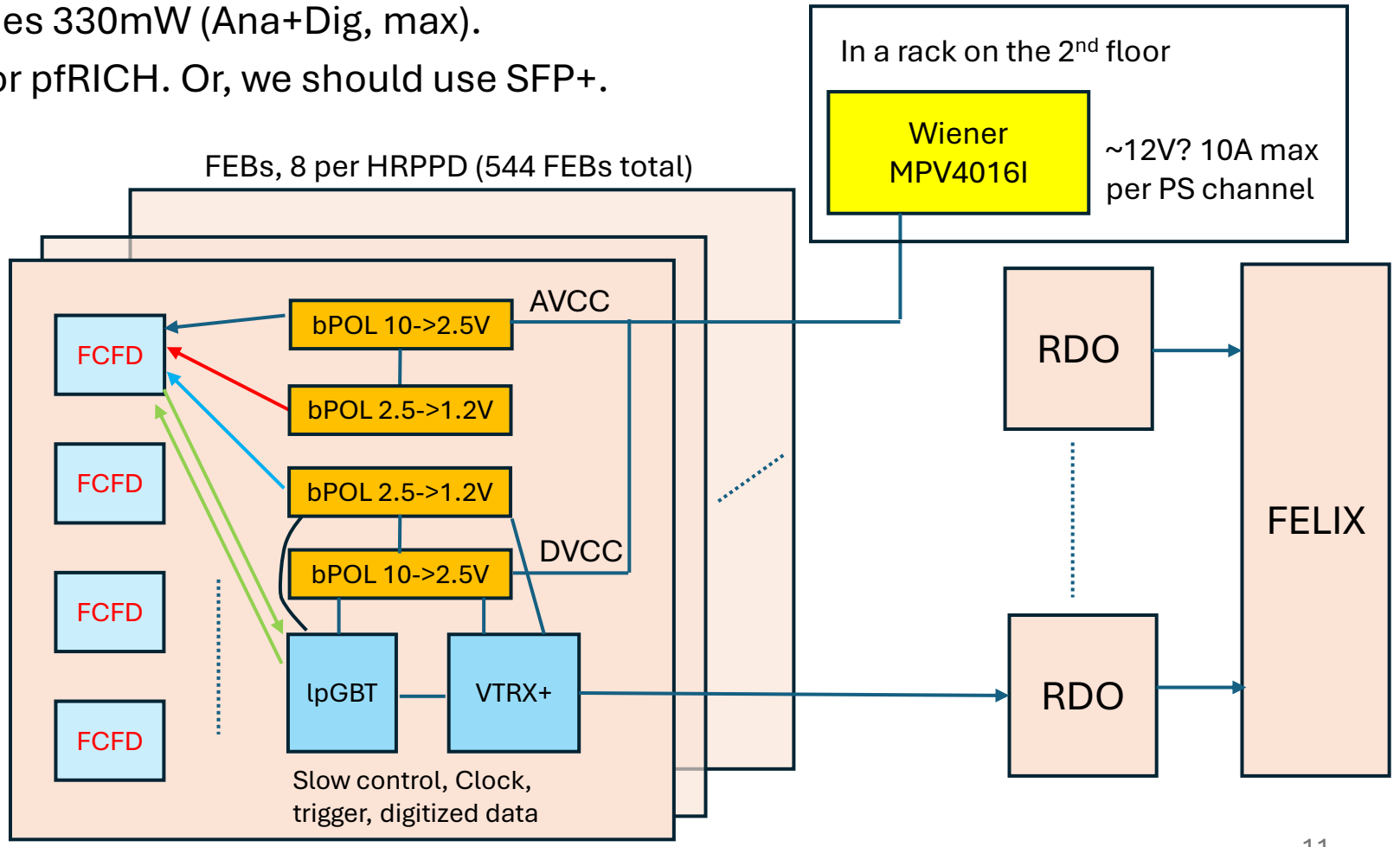
Power Loss: *xxx* *xxx* *xxx* *xxx* *xxx*

LV power-dist scheme (going to FEBs)

- Slow Control through RDO->VTRX+
- MPV4016I (Wiener PS) : 4ch per module. 0-16V output, 100W/ch max, 10A max.
  - Three HRPPD modules (8*3 FEBs) share a PS channel? Or, we split per module.
- A FCFD chip with 32ch consumes 330mW (Ana+Dig, max).
- We need 544 VTRX+ modules for pfRICH. Or, we should use SFP+.

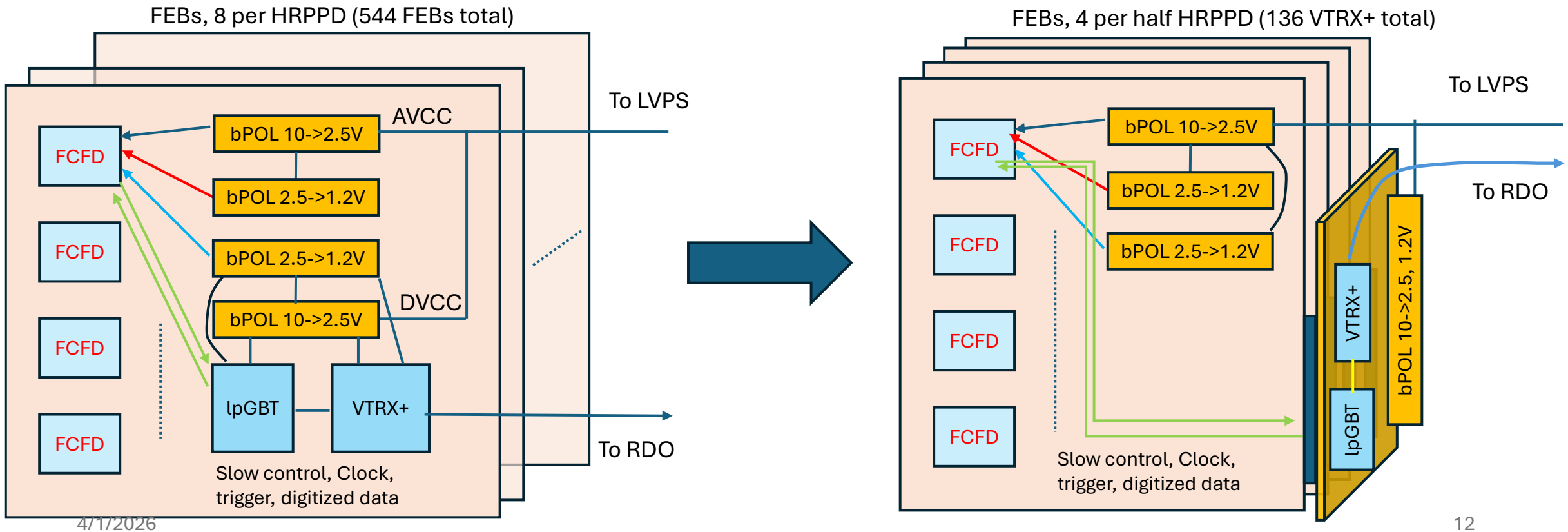
Parts	Per unit	QTY
FCFD	330mW	4
lpGBT	750mW	1
VTRX+	300mW	1
bPOL12	~75% eff	1 per line
bPOL2V5	~86% eff	1 per line
Total	~3.7W	per FEB

- bPOL12 and bPOL2V5 efficiencies are uniformly applied to get total, which is obviously overestimate
- Separating AVCC and DVCC maybe overkill for FDFC.



Another option for lpGBT + VTRX+

- We could make a ”father board” with one lpGBT+VTRX+ that connects to 4 or 8 FEBs
  - Data from 4 or 8 FEBs can be transferred to the father card without line drivers, etc.
  - This will save power by ~1.6W (max) for each FEB. Maybe one PS channel can drive 4 FEBs.
- It depends on the data rate from the FCFD chips and lpGBT+VTRX+ bandwidth
  - 4 FEB case (half HRPPD): ~100MHz (BC) * 512 ch * (5bit (ADC) + 5bit(TDC)) * 1% occupancy = 5.1 Gbps
  - Max bandwidth for lpGBT+VTRX+ is 10.2 Gbps.



Power for chips, lpGBT, VTRX+ (LDO cases)

- Individual channel
  - PreAmp+Discr: 3.8mW (1.5mA for 2.5V, 3.2mA for 1.2V) (max)
  - TDC+ADC: 0.2mW → 0.16mA for 1.2V
  - Supporting circuitry: 0.2 mW → 0.16mA for 1.2V
  - Global Circuitry is per-chip basis.
- 32ch chip
  - PreAmp+Dicr: 122mW (49mA for 2.5V, 102mA for 1.2V)
  - TDC+ADC: 6.4mA -> 5.3mA for 1.2V
  - Supporting circuitry: 6.4mW -> 5.3mA for 1.2V
  - Global Circuitry: 160mA for 1.2V
- Current
  - Min-Max I for 1.2V: 171mA - 273mA
  - Min-Max I for 2.5V: 0mA – 49mA (anti-correlate with 1.2V)
- Wattage
  - Min-Max W with single 2.9V power: 0.64W – 0.79W/chip
  - Min-Max W with 2.9V and 1.7V powers: 0.43W - 0.47W/chip
- Other Component
  - lpGBT: 700mW (@10Gbps. 1.2<V<1.32 only → 540mA?)
  - VTRX+: 306mW for 4TX+1RX (max).
- One-card power
  - chip only: 1.9W (two V) - 3.2W (one V)
  - whole: +(0.99W+0.43W, two V), +(1.7W+0.74W, one V)
- Per module power: 27W - 45W
- bPOL spec
  - bPOL 12, max Iout is 4A, eff is 75% (10V to 2.5V)
  - bPOL 2.5, max Iout is 3A, eff is 86% (2.5V to 1.2V)

- Target power per channel:

Circuit Component	Power per Channel [mW]	Power per ASIC[mW]
Preamp + Discr (low-*high power*)	2.1 - 3.8	269 - 486
TDC+ADC	0.2	26
Supporting Circuitry	0.2	26
Global Circuitry		*200**
Total (*high power*)		521 - 738

Assumptions : FCFD is 128 channels

*** Based on ETROC, may be an overestimate**