Power tree for ePIC MPGDs

Irakli Mandjavidze

Irfu, CEA Saclay
Gif-sur-Yvette, 91191
France

eDAQ WG
16/Apr/2026

Reminder of ePIC MPGDs

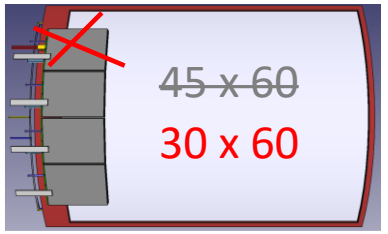
- Cylindrical Micromegas Barrel Layer : CyMBaL : ~35k channels
  → 48 tiles of 1024 channels each

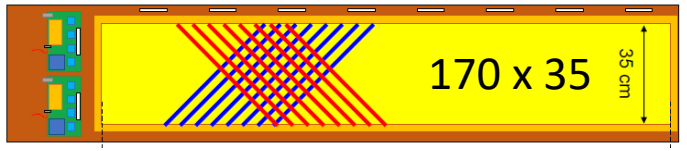
- µRWELL Barrel Outer Tracker : µRWell-BOT : ~100k channels
  → 24 modules of 4 096 U-V strips each

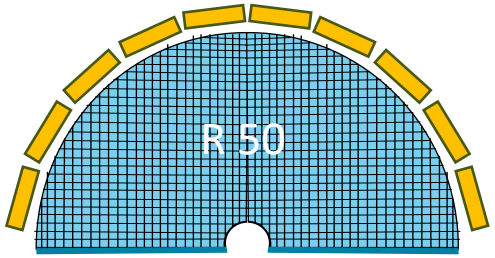
- µRWell End Cap Tracker : µRWell-ECT : ~30k channels
  → 8 half-disks of 4 000 X-Y strips each

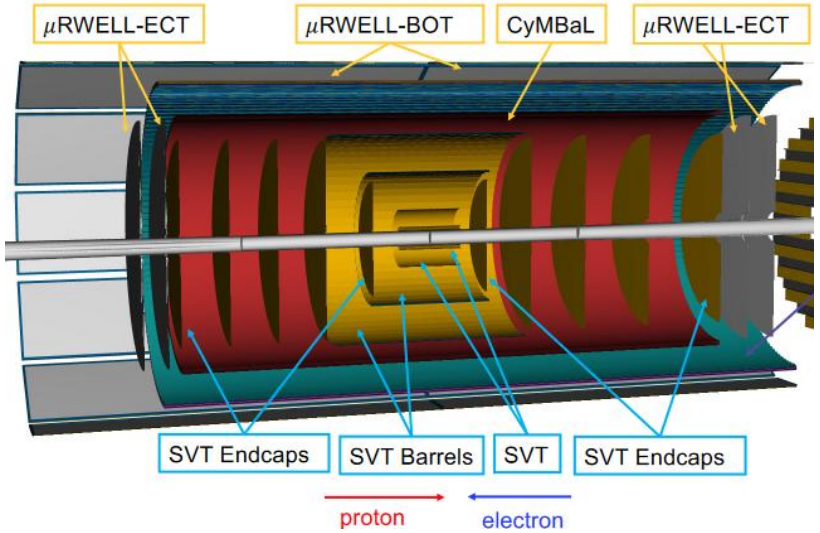
- ~165k-channel heterogeneous system
  → Micromegas, µRWell, barrel, endcap, curved, planar, circular

- Common approach to acquire data from different types of ePIC MPGDs
  → Use same frontend ASIC
    - Salsa – under development
  → Share frontend design between groups
    - Adapt form factor if needed





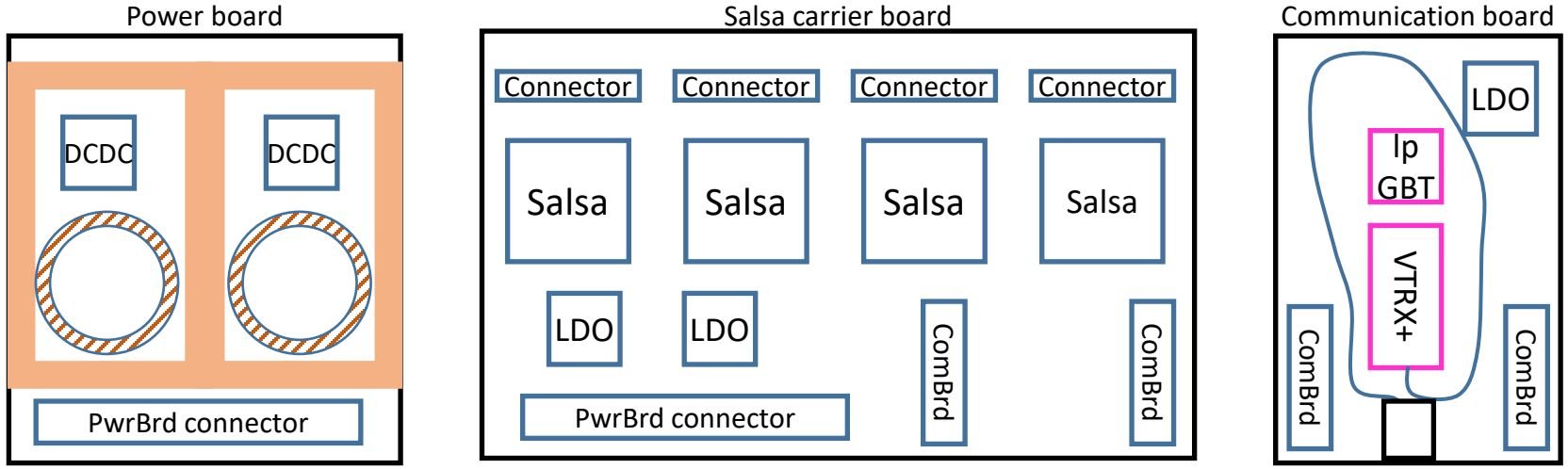




Outlook

- The power chain is as follows
  - → LV power supply – cable plant – DCDC power board – Salsa carrier and communication boards
  - → The last actors in the power chain are LDO regulators producing clean power for ASICs
    - Salsa, lpGBT, VTRX+
  - → Salsa requires high current 1.2V
  - → lpGBT requires low current 1.2V
  - → VTRX+ requires low current 2.5V and 1.2V

For illustration only : just to show frontend component types

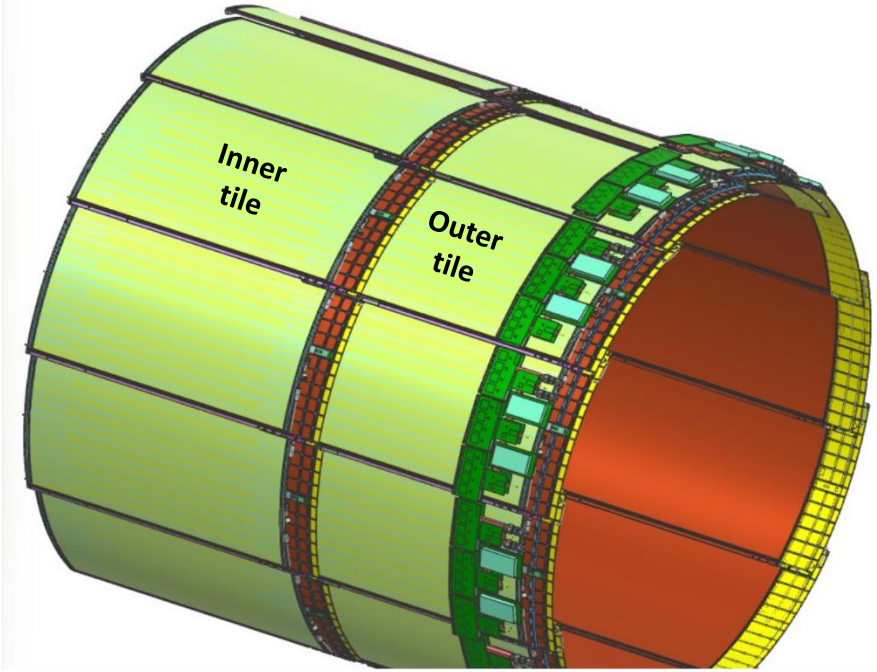


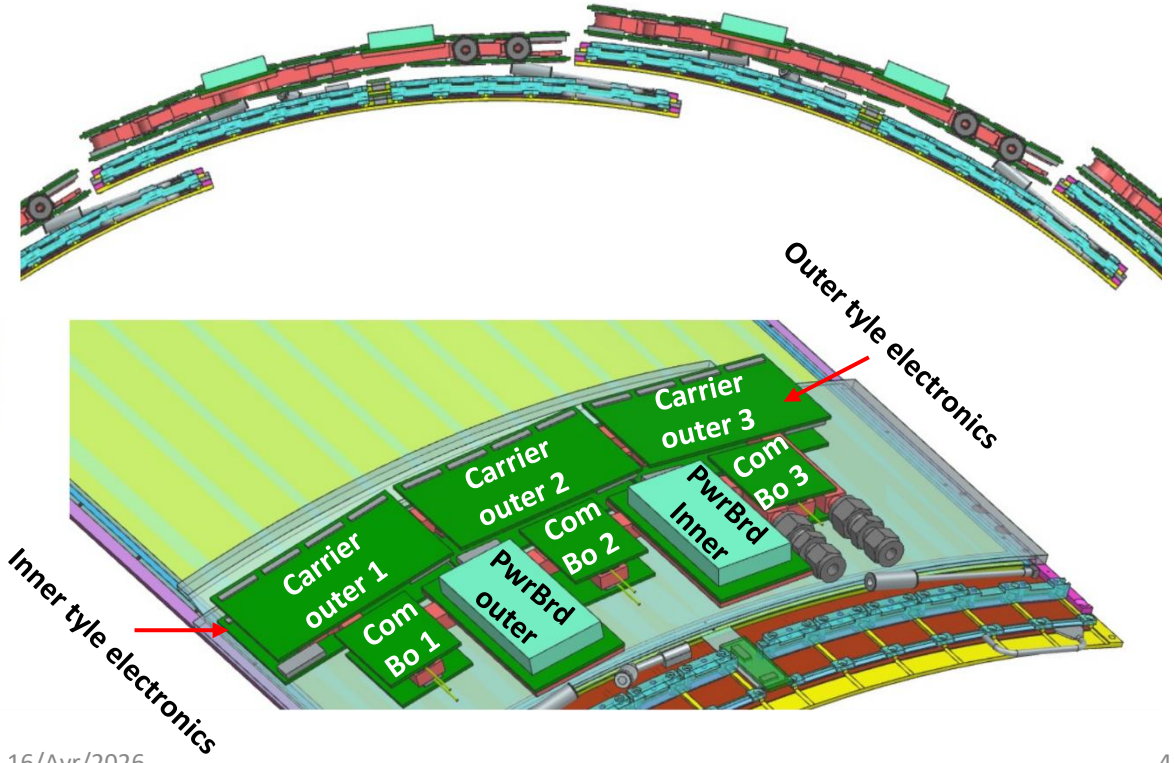
- Review 2 powering scenarios
  - → Shown on CyMBaL frontend case

Targeted integration of detector tyles and readout electronics

- Detector tile readout
  - → 3 pairs of Salsa carrier and communication ComBo boards per detector tile
    - 3 x 256 = 768 channels
  - → Shared power board
    - Wired connection with every pair

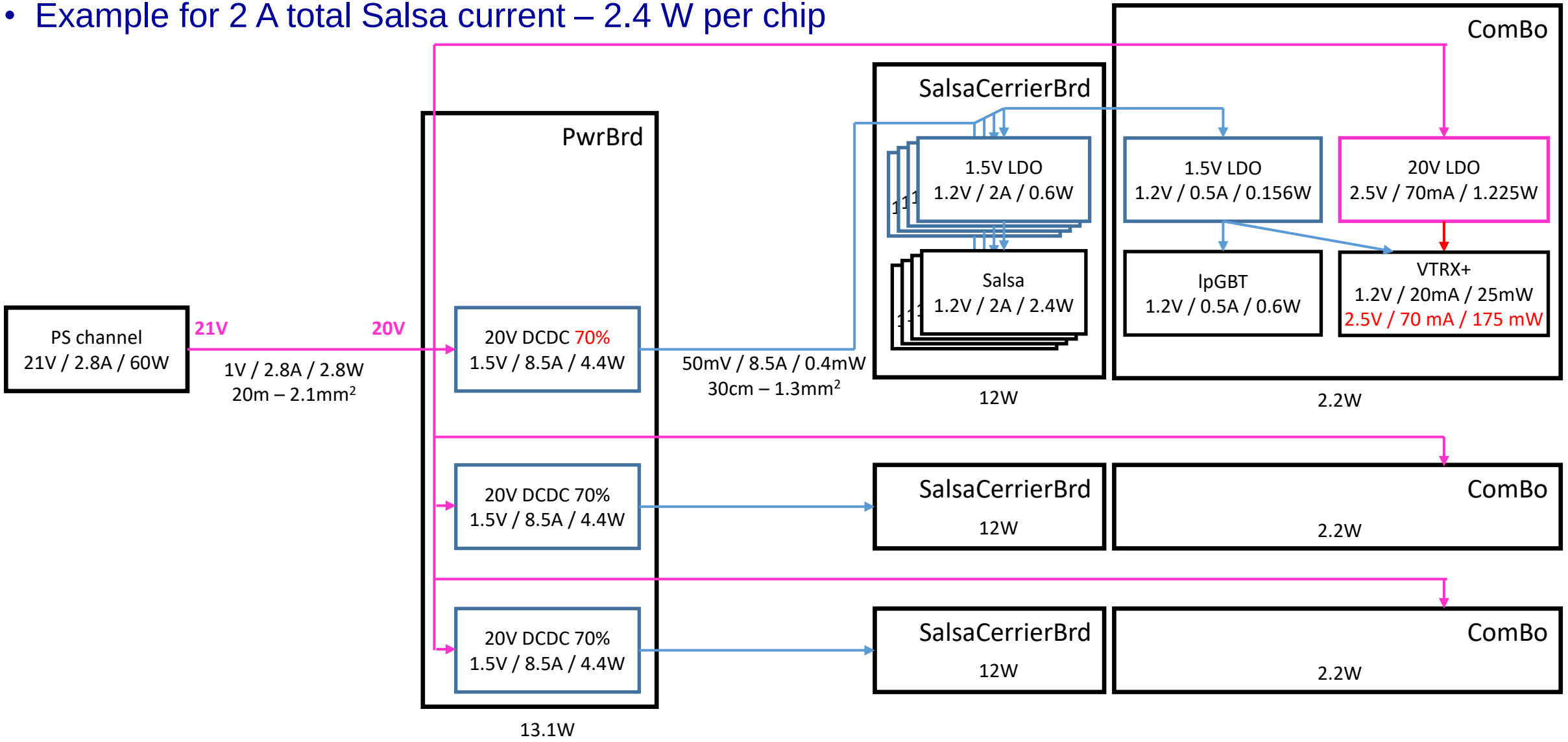
- Superimposed readout electronics of inner and outer longitudinal tiles
  - → Common cooling infrastructure





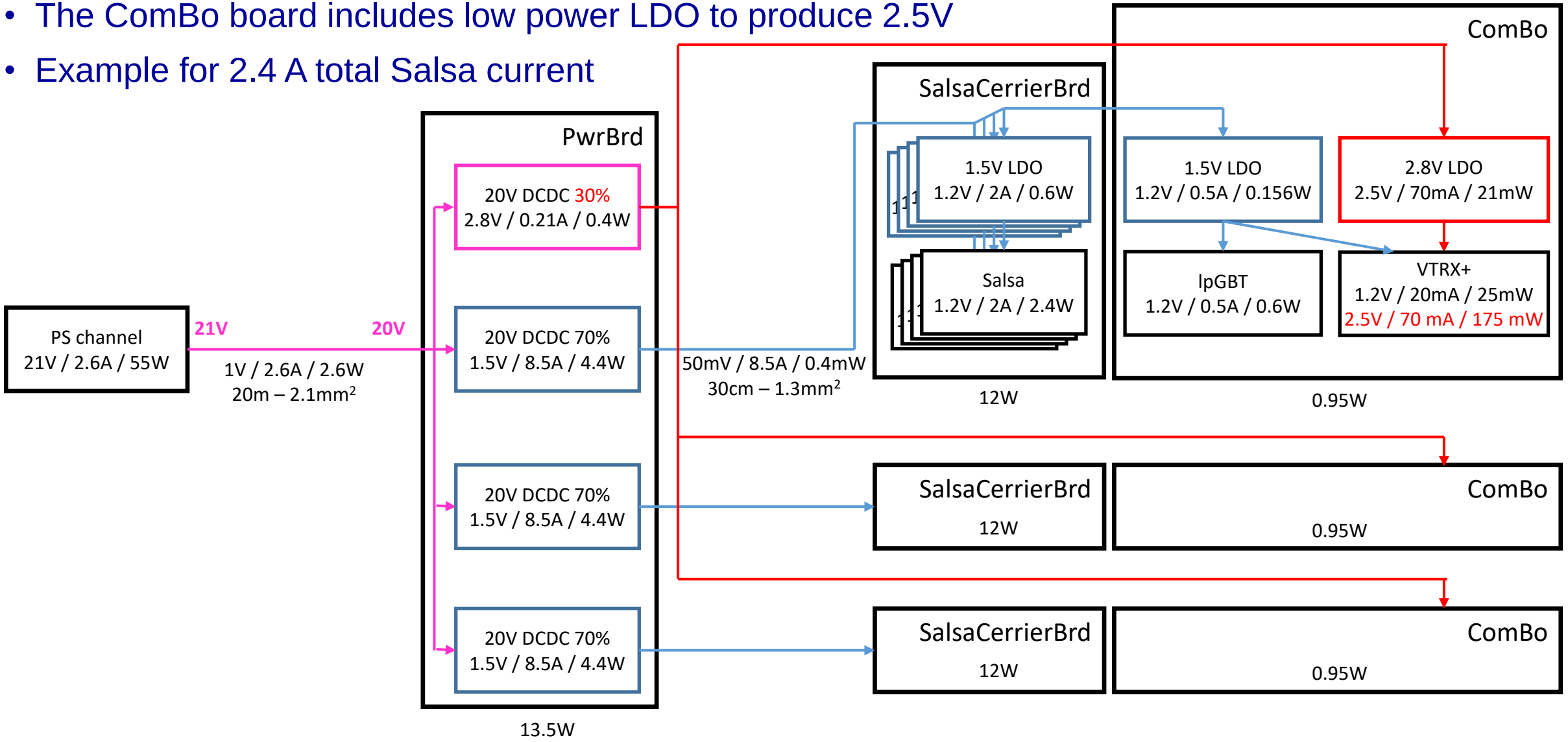
CyMBaL tyle power distribution

- Shared power board for the 3 FEBs of a tile
- Example for 2 A total Salsa current – 2.4 W per chip

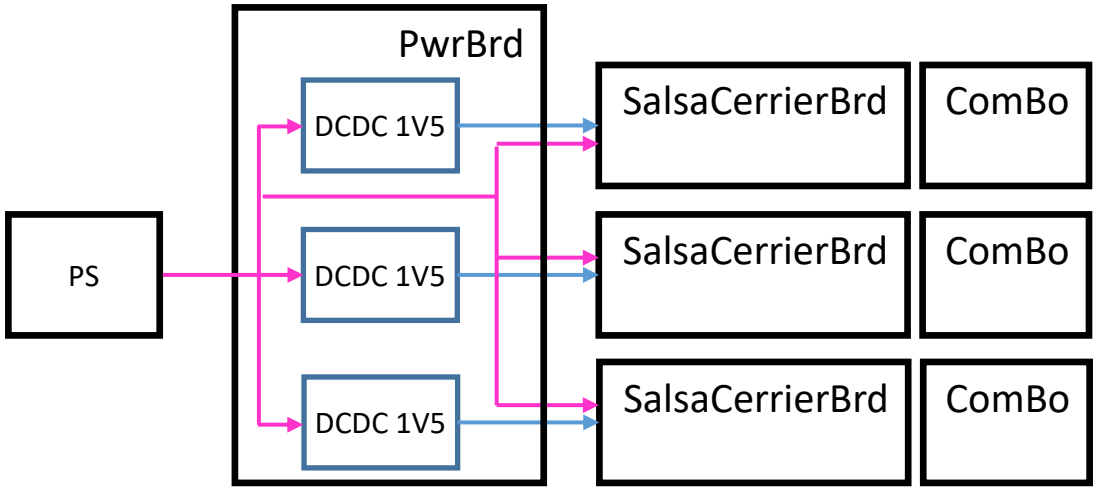


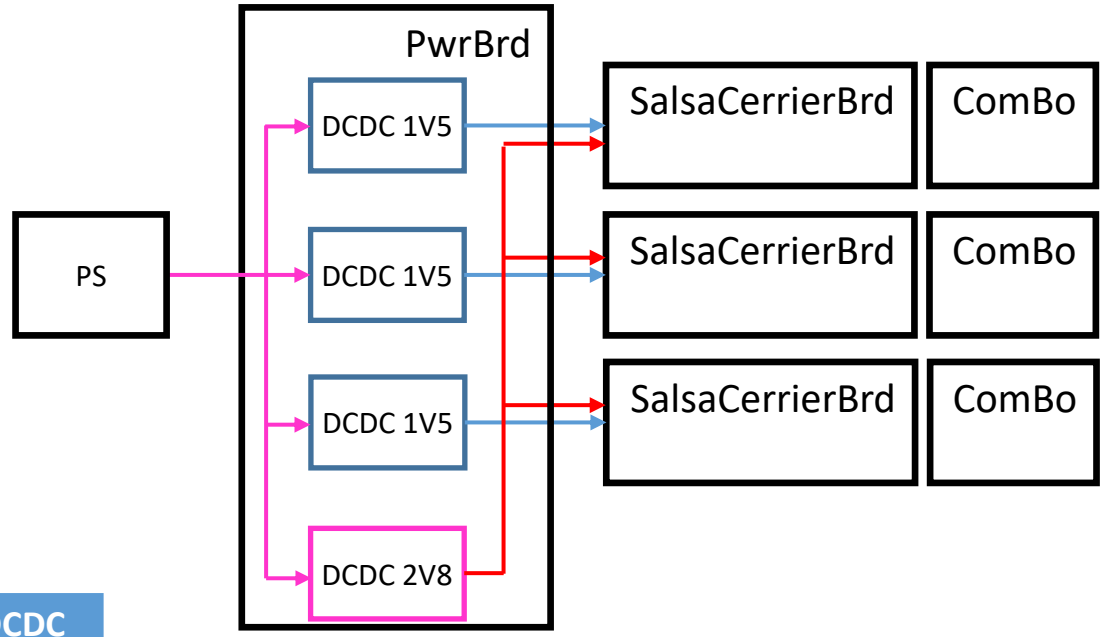
Power distribution : Shared power board with 2.8V DCDC

- Shared power board includes 4th shared DCDC converter for 2.8V
- The ComBo board includes low power LDO to produce 2.5V
- Example for 2.4 A total Salsa current



Comparison

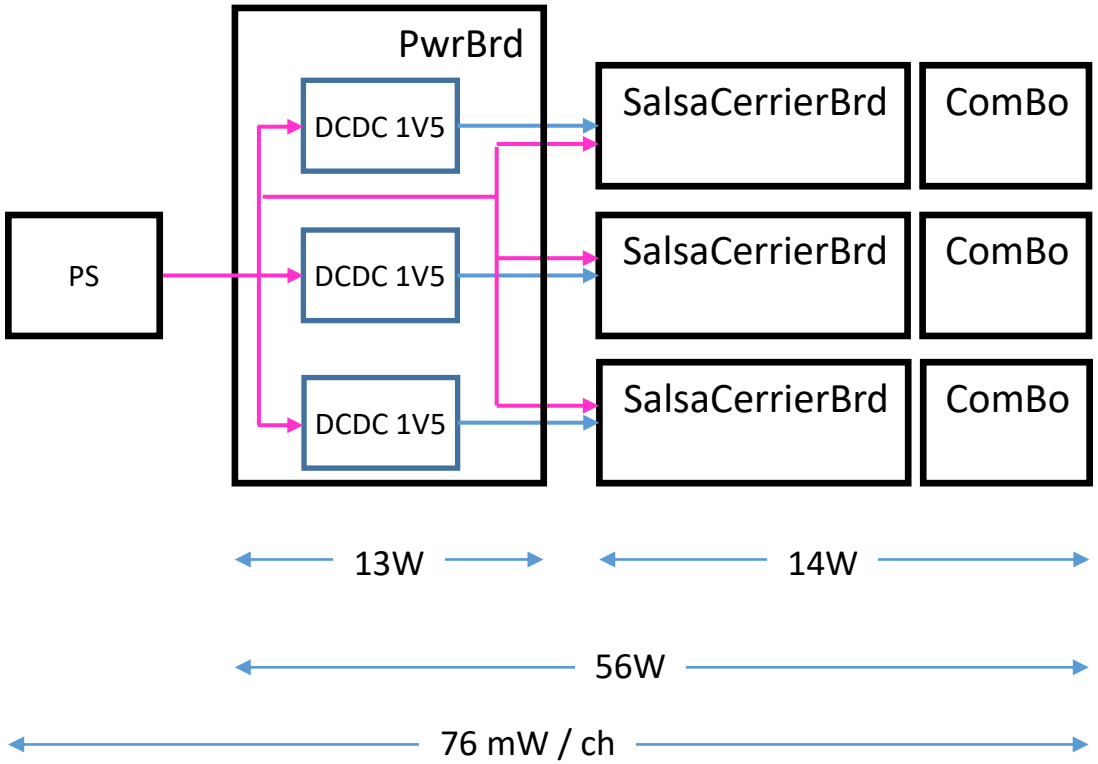


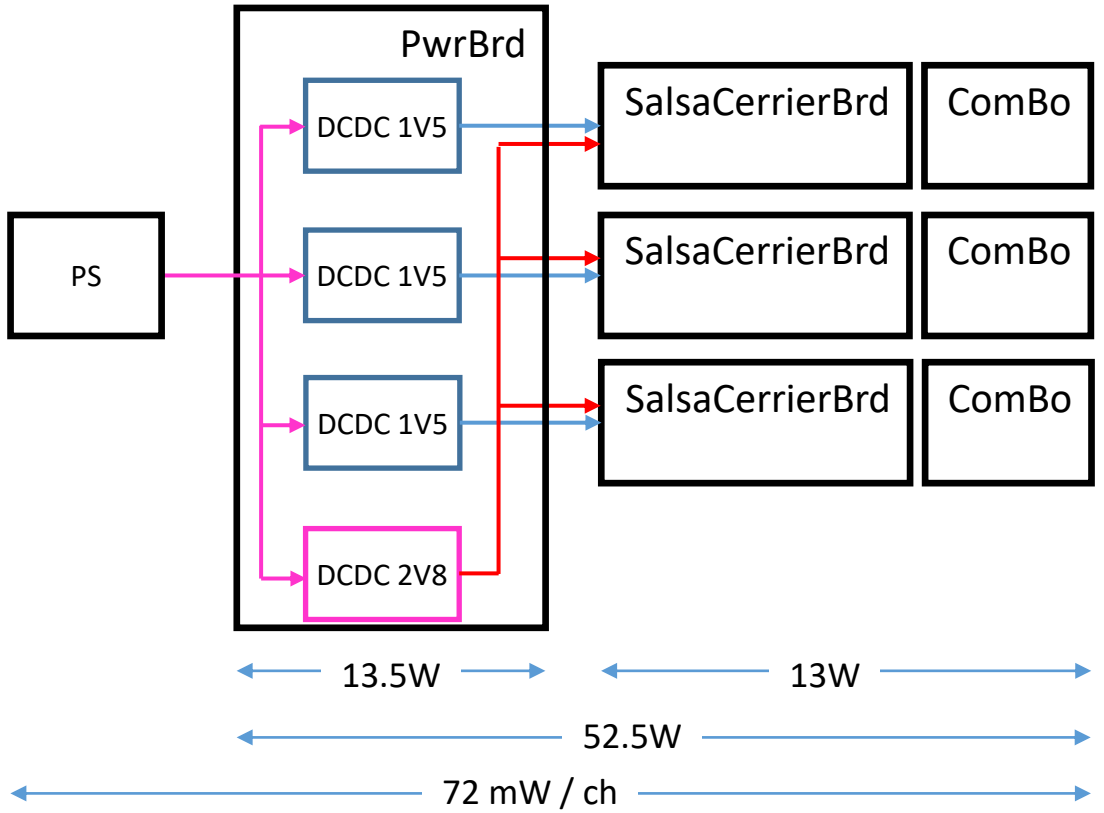


	W/o 2.8V DCDC		W/ 2.8V DCDC	
	Power	Pwr/ch	Power	Pwr/ch
	W	mW	W	mW
Salsa	2.4	37.5	2.4	37.5
Salsa carrier	12.0	46.9	12.0	46.9
Salsa carrier + ComBo	14.2	55.5	13	50.6
Power board	13.1		13.5	
3 x (Salsa carrier + ComBo) + PwrBrd	55.7	72.5	52.5	68.3
Power supply	58.4	76.0	55	71.6

Comparison

- Is it worth to have 4th shared DCDC converter as a source of 2.5V ?
- Comparison is given for Salsa current of 2A

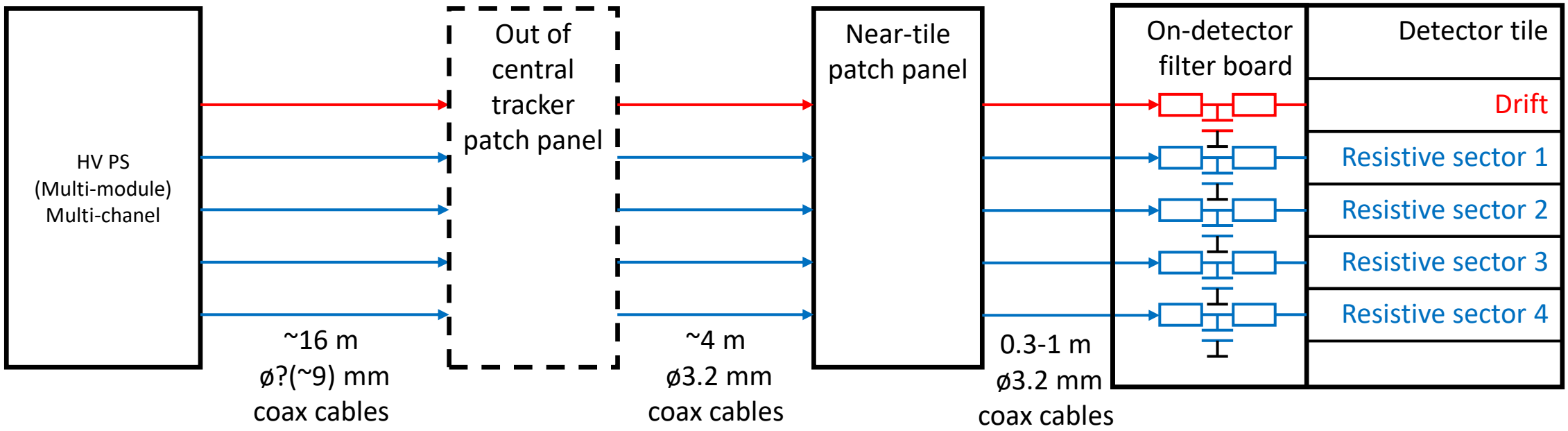




- Comparable power consumption and heat dissipation wise
- Scheme on the left seems easier to implement

CyMBaL HV power distribution

- 5 HV power lines per detector tile
  - → 4 independent resistive segments at O(+500V)
  - → 1 drift electrode at O(-1 000V)
  - → Limits -1.5 kV, +1kV, 100 µA



- Reminder : 48 detector tiles
  - → Groups of 24 tiles powered from electron and ion sides

Caveats

- Power consumption of Salsa is being estimated
  → 2A per chip is at high end

- DCDC performance is not very well known
  → 20V min input voltage is assumed but might be lower
  → 70% efficiency is assumed at 8A current – might be (slightly) better or worse

  → Sharing of experience in this domain is more than welcome to come out with an optimal solution

- The current estimations indicate upper limits of LV power consumption
  → Ongoing work
  → Reminder : 656 MPGD FEBs in total
    - CyMBaL – 144; µRwell-BOT – 384; µRWell-ECT – 128

- Grounding scheme to be drawn
  → Follow common ePIC recommendations