Power Tree for pfRICH

- HV (HRPPD)
- LV (for Frontend electronics)

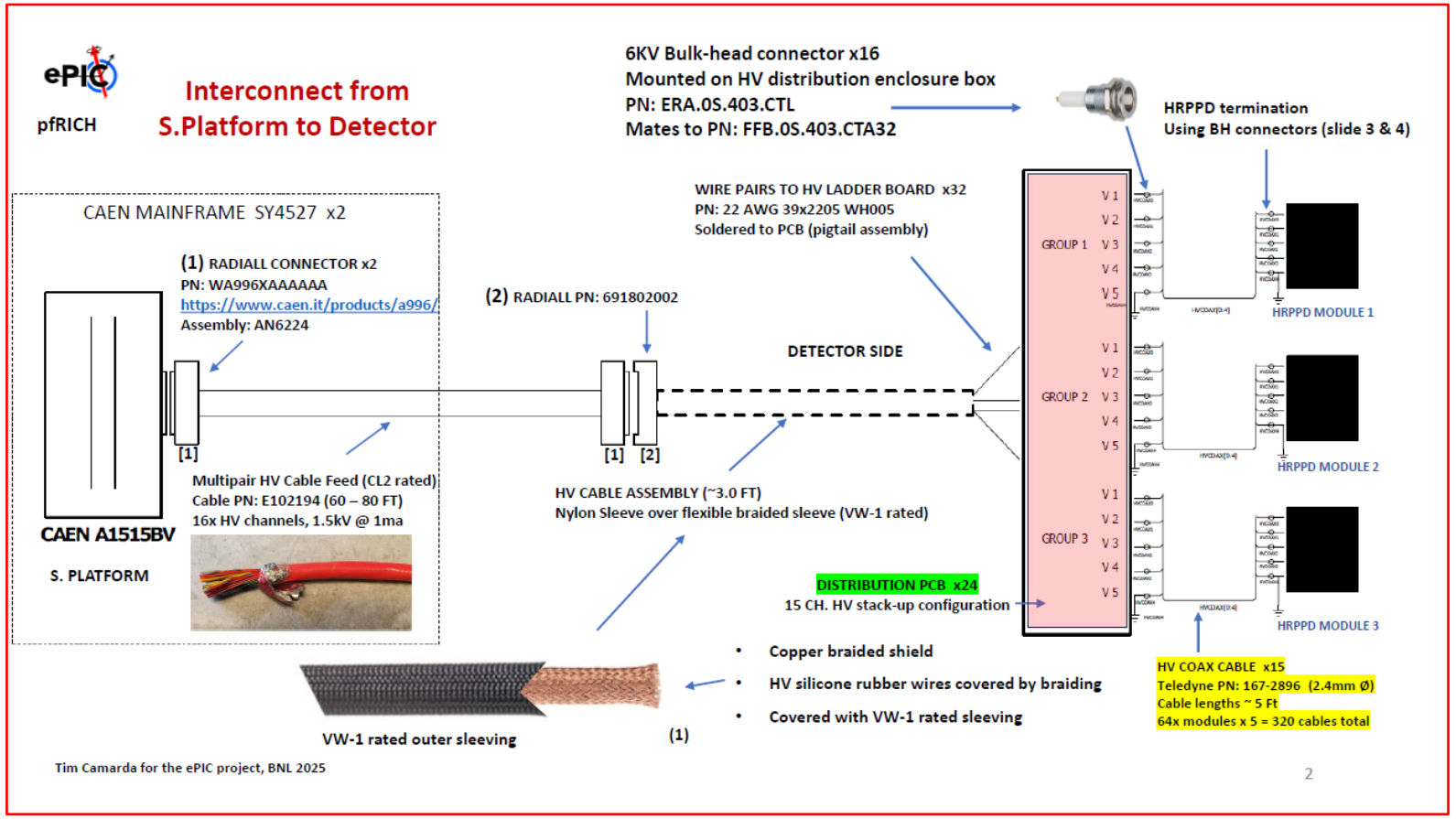
Takao Sakaguchi for

Raymond Dawson and Alexander Kiselev

HV (for HRPPD)

- Tim Camarda's design on the HV system
- One HRPPD has two MCPs (Entry MCP and Exit MCP).
  - Resistance of an MCP is 6 to 7 MOhm.
- 800-900V Bias voltage is applied to each MCP
  - One HRPPD consumes ~200mW.

From Tim's slide



Power Distribution Tree

Sub-Detector: pfRICH Type: HV

#Ch: 340 (=5*68)
Ch V/I: 0.2mA
Model: CAEN A1515BV
Qty: 23

On-detector: Y/N
Custom board
Qty: 23

To Adapter: Y/N
To FEB: Y/N
To: Backplane

- ~200mW per HRPPD module
- ~14W for whole pfRICH

Wire Gauge: 15 pairs of 26
Current/Wire: 0.2mA (for two wires, others are zero)
Part#: E102194
Length: 80 ft
Qty: 23

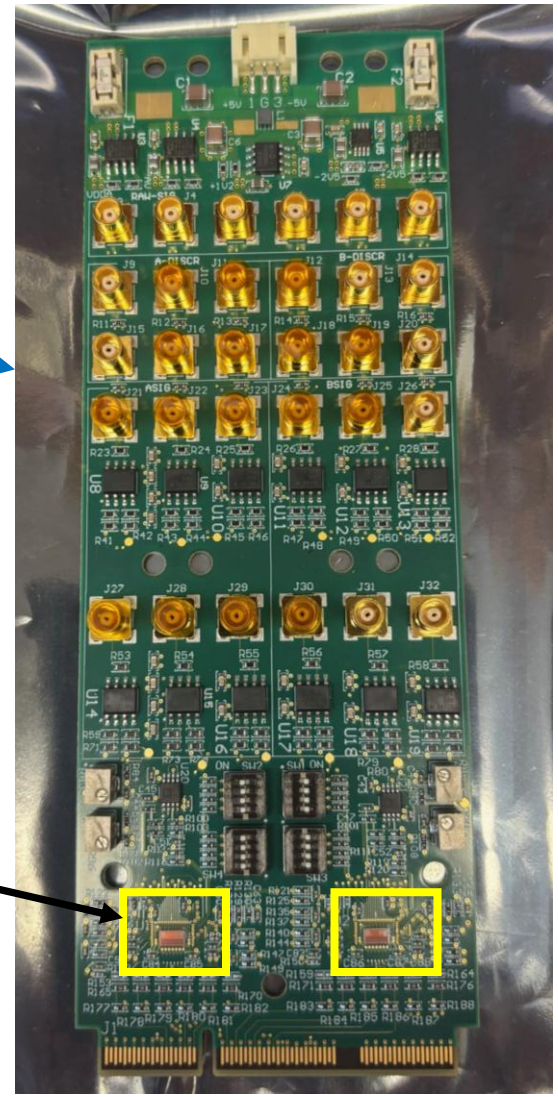
Wire Gauge: 68 * 5 of 26
Current/Wire: 0.1mA (for two wires, others are zero)
Part#: 167-2896
Length: 5ft
Qty: 340

*Power Loss: 3.6 * 1.0^{-5}W* *2.3 * 1.0^{-6} W* *xxx* *xxx*

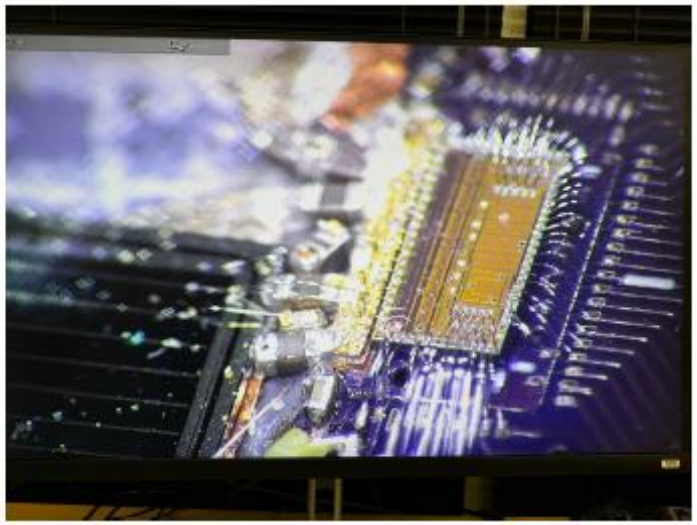
FCFD chip for readout ASIC

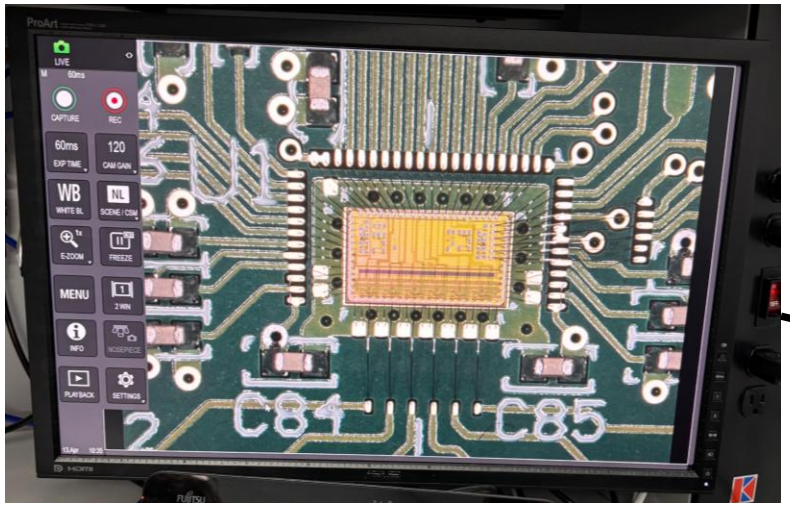
The current chip has 6 channels of Analog-amp and CFD output (No ADC/TAC)

Test board with chips wire-bonded at the IO at BNL.



Picture of FCFD chips from Artur (FNAL)





Power consumption of a 32ch-FCFD

- FCFD now goes for 32ch/chip.
- Artur said the following table for power estimate is still valid at this time.
- Scaling numbers to 32 ch:
  - Analog 32ch: * 3.8mW * 32 = 120mW
  - TPC+ADC 32ch: 32ch *0.2mW = 6mW
  - Supporting Circuitry 32ch: 32ch*0.2mW = 6mW
  - Global circuitry: 1per chip = 200mW
- Total power per chip will be: 330mW
- From pfRICH's viewpoint, the FCFD variants would only have different preamp gain (and number of elinks depending on data rate)

From Artur's slide

- Target power per channel:

Circuit Component	Power per Channel [mW]	Power per ASIC[mW]
Preamp + Discr (low-*high power*)	2.1 - 3.8	269 - 486
TDC+ADC	0.2	26
Supporting Circuitry	0.2	26
Global Circuitry		*200**
Total (*high power*)		521 - 738

Assumptions : FCFD is 128 channels

*** Based on ETROC, may be an overestimate**

Readout scheme idea and LV powers

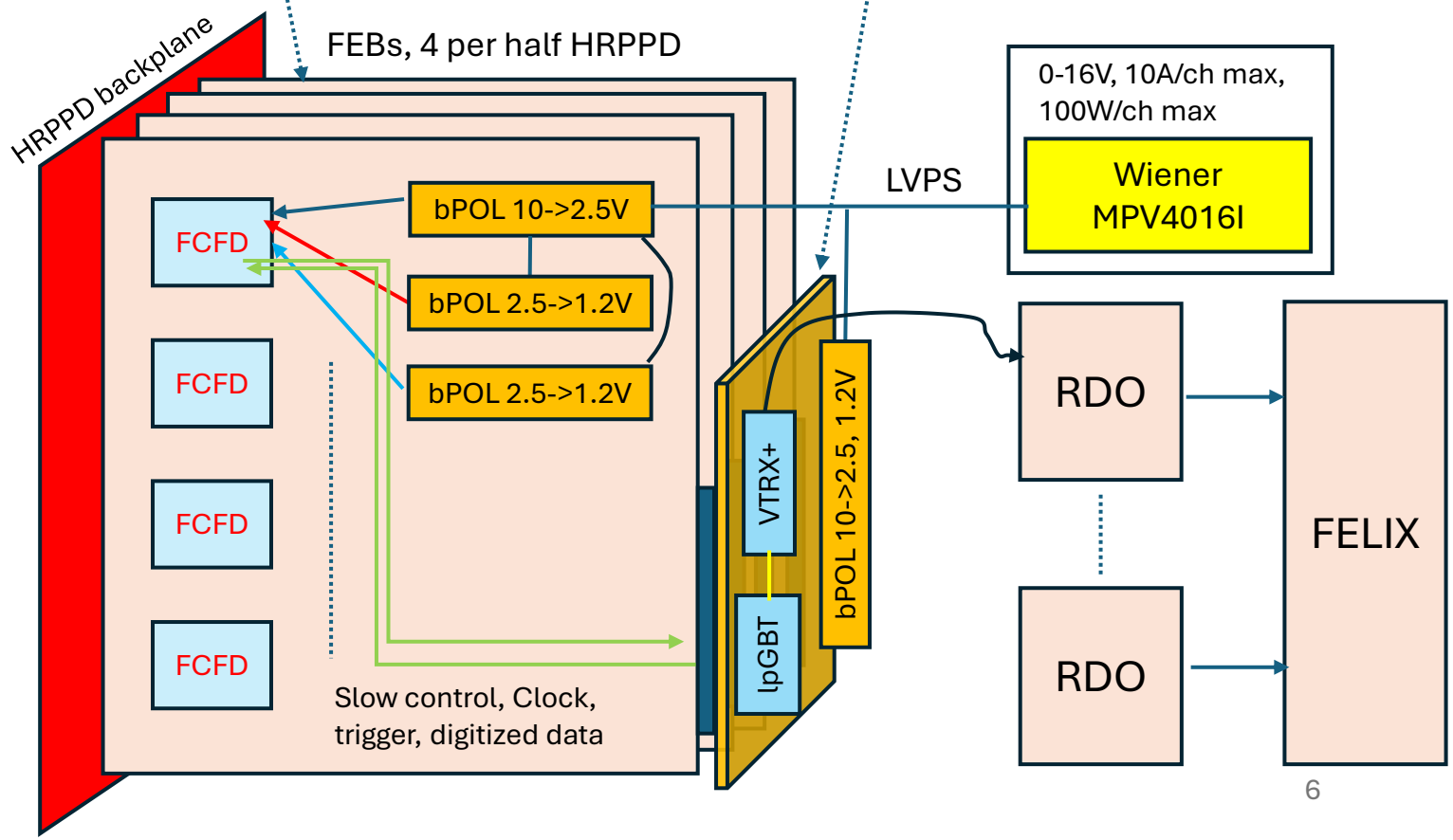
- Idea on FCFD, FEB, and FB.
  - Assuming four FCFDs per FEB.
  - 320Mbps data rate (one e-link)
  - Father board (FB) with a set of lpGBT and VTRX+ can handle four FEBs
  - Alexander showed this plan already in the collaboration meeting in 2023.

- 2.1*8+1.6*2 = 20 W per HRPPD.
  - MPV4016I (Wiener) : 4ch per module. 0-16V output, 100W/ch max, 10A max.
  - Three HRPPD modules can share a PS channel (consistent with HV granularity).
  - I_{max}: 4A for bPOL12 and 3A for bPOL2V5.
  - bPOL12 and bPOL2V5 efficiencies are uniformly applied, which is obviously overestimate.

- Bandwidth of lpGBT + VTRX+
  - Max rate for lpGBT with FEC10 encoding is 7.68Gbps.
  - 4 FEB (half HRPPD): ~100MHz * 512 ch * 10bits (ADC+TDC) * 1% = 5.12 Gbps

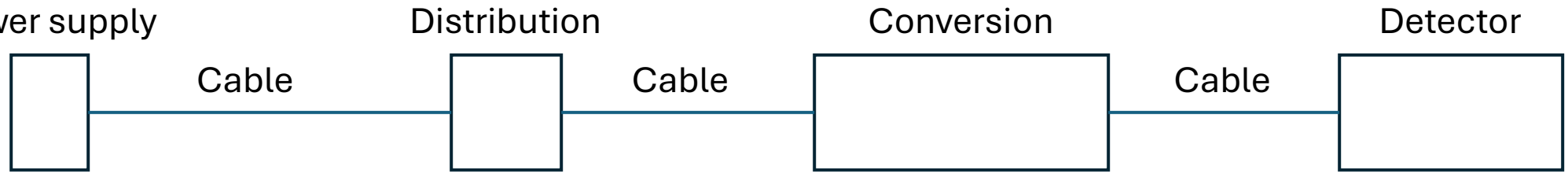
Parts	Per unit	QTY
FCFD	330mW	4
bPOL12	~75% eff	1 per line
bPOL2V5	~86% eff	1 per line
Total	~2.1W	per FEB

Parts	Per unit	QTY
lpGBT	750mW	1
VTRX+	300mW	1
bPOL12, 2V5	~75%,~86% eff	1 per line
Total	~1.6W	Per FB



Power Distribution Tree

Sub-Detector: pfRICH Type: LV



#Ch: 4
Ch V/I: 12V/10A
Model: Wiener MPV4016I
Qty: 6

On-detector: Y/N
Qty:68
12AWG to pigtail

On-detector: Y/N
Qty: same as FEB

DC/DC: bPOL12, 2V5
V/I: 2.5, 1.2
Qty: 1768

LDO: N/A

To Adapter: Y/N
To FEB: Y/N

Work in progress

Wire Gauge: 12AWG?
Current/Wire: 3A
Part#:
Length: 80ft
Qty: 68

Wire Gauge: Pigtail (20AWG?)
Current/Wire: 0.25A?
Part#:
Length: 5ft
Qty: 680

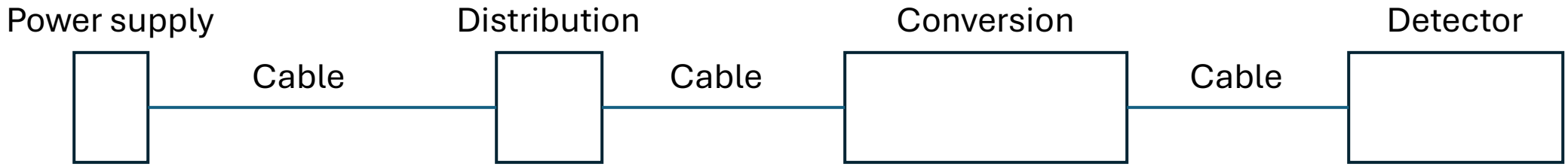
Wire Gauge:
Current/Wire:
Part#:
Length:
Qty:

Power Loss: *xxx* *xxx* *xxx* *xxx* *xxx*

Backup

Power Distribution Tree

Sub-Detector: xxxx Type: LV or BIAS or HV



#Ch:
Ch V/I:
Model:
Qty:

On-detector: Y/N
Qty:

On-detector: Y/N
Qty:

DC/DC:
V/I:
Qty:

LDO:
V/I:
Qty:

To Adapter: Y/N
To FEB: Y/N

Wire Gauge:
Current/Wire:
Part#:
Length:
Qty:

Wire Gauge:
Current/Wire:
Part#:
Length:
Qty:

Wire Gauge:
Current/Wire:
Part#:
Length:
Qty:

Power Loss: *xxx* *xxx* *xxx* *xxx* *xxx*

Plan and TODO (Random list)

- Must check items for FCFD-variant chip design
  - What is max Q?
    - e.g. 2 p.e. & $5*10^6$ gain =1.6pC
  - ADC/TDC 5bits enough?
  - Is the occupancy about 1%?
    - 320Mbps data link from a FCFD needs the occupancy lower than 1%
    - 32ch * 10 bits *100MHz * 1% occupancy = 320Mbps (without header)
  - Do we want wire-bonding type package, or BGA?
    - BGA should be much easier to deal with. We could ask this.

- TODO for next months
  - Get FDFC cards ready for CERN beam test. (one or two cards)
  - Readout scheme should be fixed soon
    - Make a list of custom parts (ASICs, bPOL, lpGBT, VTRX+) and their QTY needed for pfRICH.
    - This is rather urgent.
  - Make sure that we ask for enough LV modules.
  - Make mock-up of the FEBs/FB and cabling, to figure out if we can integrate them by hands.
  - Make initial cooling scheme for FEBs/FB