9MHz System Performance & Update

Salvatore Polizzo

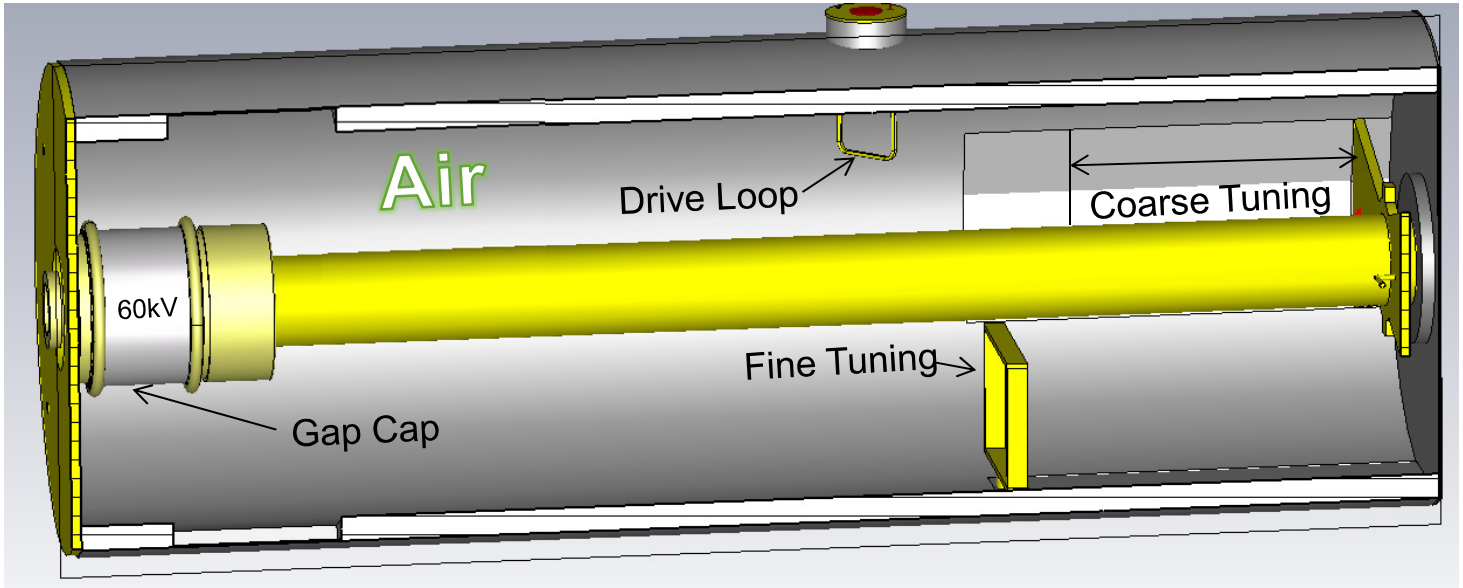
FY17 RHIC Retreat

8/8/17

Presentation Overview

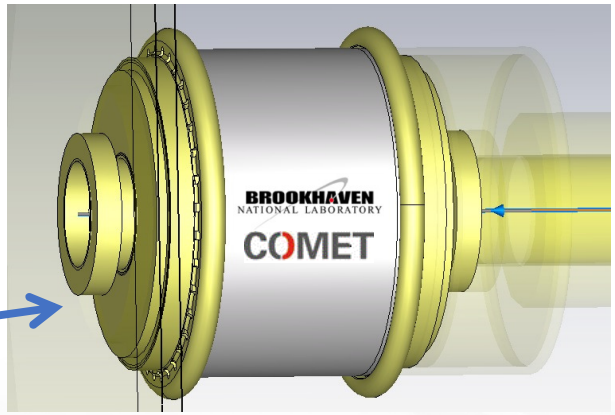
- New 9MHz Systems
  - Cavity Design Basics (Visual Overview)
  - FY17 Performance Review (Polarized Proton Operation Mode)
  - Current Efforts (Extending the high end voltage margin)
  - Conclusions

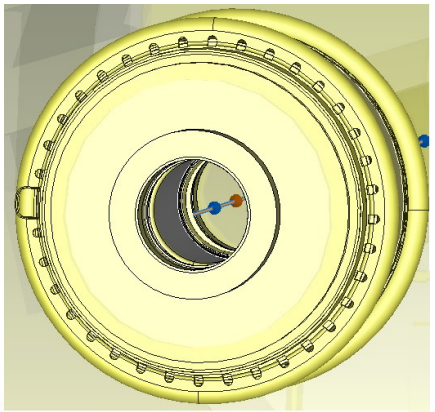
9MHz Cavity Design Overview



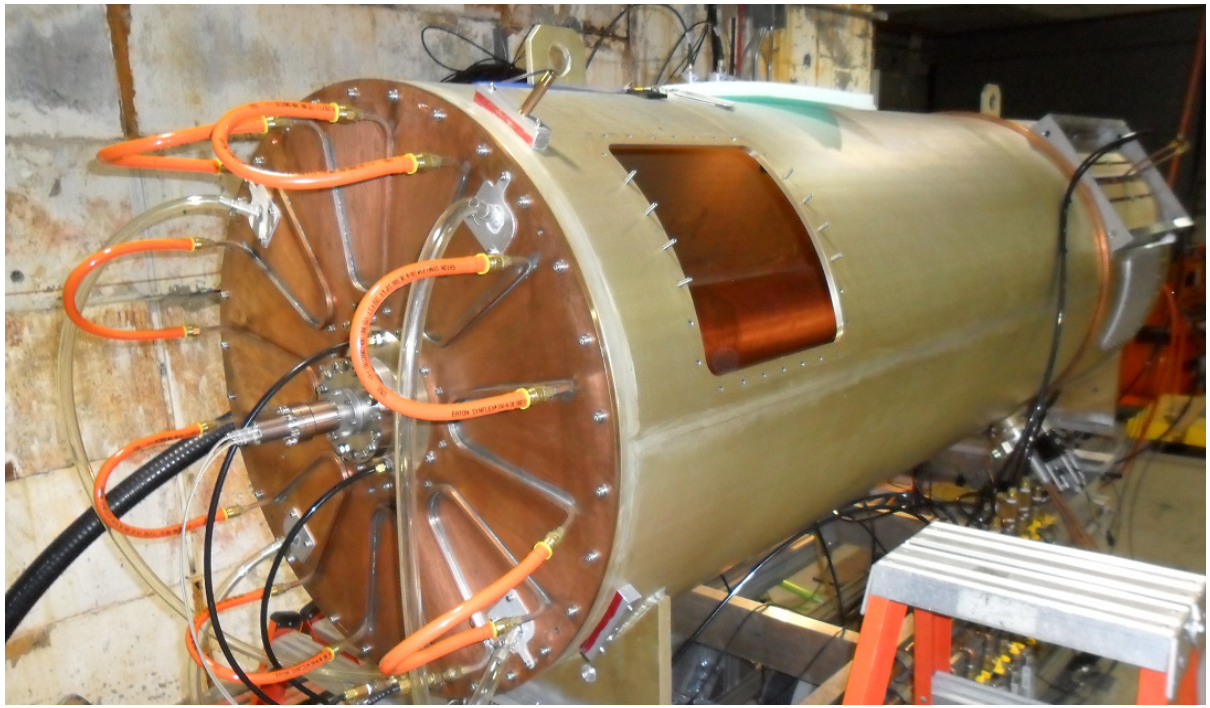
- Cavity Length ≈ 3m
- Cavity Radius = .45m

The resulting gap capacitor assembly is the product of an ongoing collaboration between BNL and Comet Technologies.

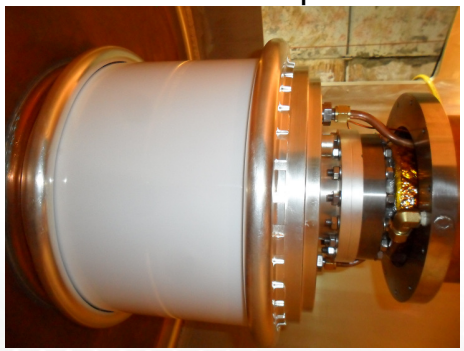




9MHz Cavity Design Overview



Internal Beam Pipe View



Bell Housing Installed

9MHz Cavity Performance Review
(Polarized Proton Operation Mode)

- Cavity Voltage

  - 32kV Peak
  - *60kV Max Design Voltage (53.4kV LEReC Design Requirement)*
- Frequency
  - 9.376MHz – 9.384MHz
  - *8.7MHz – 9.8MHz (LEReC Design Requirement)*
- Drive Power
  - **≈ 8.2kW Peak for ≈ 32kV (Acceleration ø =33°, $\beta_{fpc} \approx 2$)**
  - ≈ 5.4kW Peak for ≈ 32kV (Acceleration ø =16.5°, $\beta_{fpc} \approx 2$)
  - *≈ 7kW for 60kV (LEReC Design Requirement $\beta_{fpc} \approx 1$)*

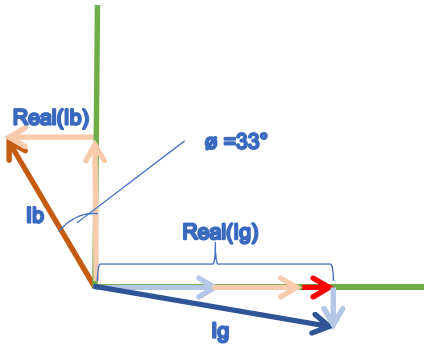
9MHz Cavity Performance Review

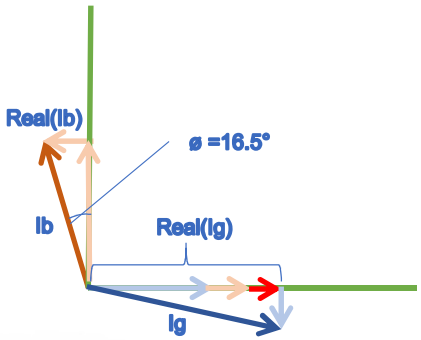
- Making voltage is not the challenge in the PP operation mode
- The challenge is to provide enough power to the beam during acceleration (max($\dot{B}$)) while maintaining sufficient power margin to fight transients.

- Fast Ramp ($\phi_{acc\ @\ max(\dot{B})}$ **= 33°)**
  - Fill Number = 20595
  - Bunch Intensity ≈ 2e11 protons
  - Ramp Time ≈ 4.5 minutes
  - Gap Voltage = 32kV
  - Drive Power ≈ 8.2kW

- Slow Ramp ($\phi_{acc\ @\ max(\dot{B})}$ **= 16.5°)**
  - Fill Number = 20865
  - Bunch Intensity ≈ 2.07e11 protons
  - Ramp Time ≈ 9 minutes
  - Gap Voltage = 32kV
  - Drive Power ≈ 5.4kW

Simplified post transition phasor plots

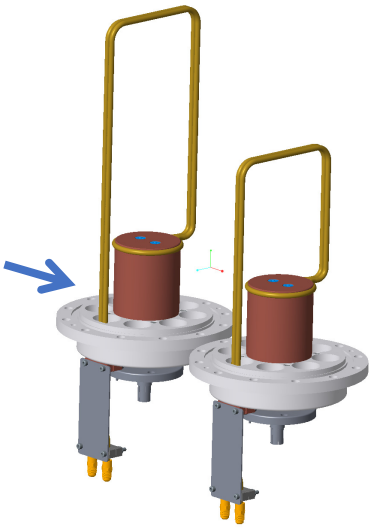




9MHz Cavity Performance Review

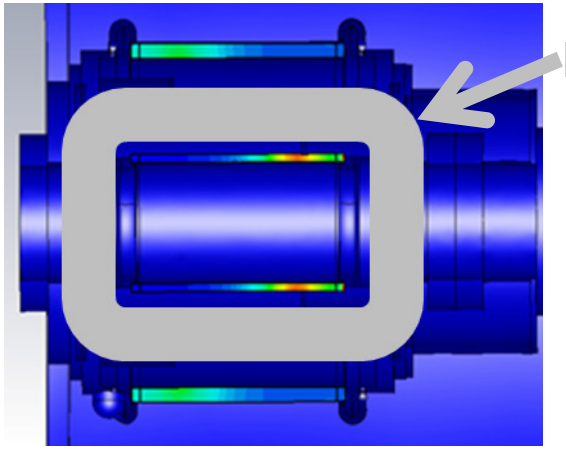
- Assuming we were able to push the beam intensity to peak FY15 levels (≈ 2.6e11 protons/bunch)
  - Estimated Drive Power > 10kW
  - Estimated Reflected Power > 1.2kW

- We may have wanted a bigger stick
  - Leverage the configurability of the cavity design to further optimize β_{fpc} thus minimizing $P_{reflected\ @\ max(\dot{B})}$
  - Peak Forward Power Reduction ≈ 10%

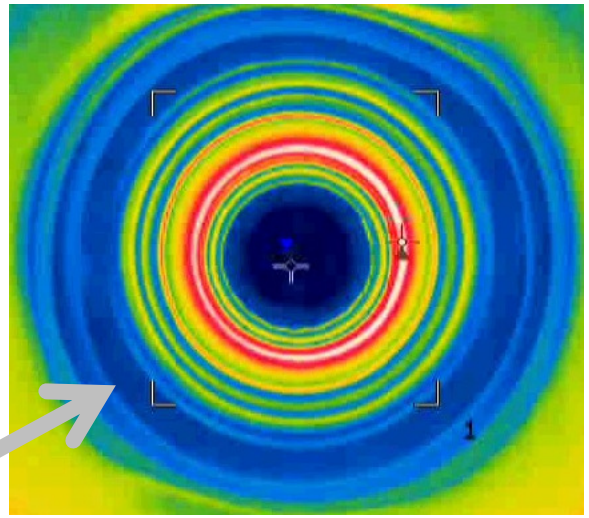


New 9MHz System Current Efforts

- Before ordering the balance of the gap cap devices we are working to improve the cavities high voltage margin by replacing the inner ceramic RF window with a higher performance alumina.



Dielectric loss profile inside alumina window

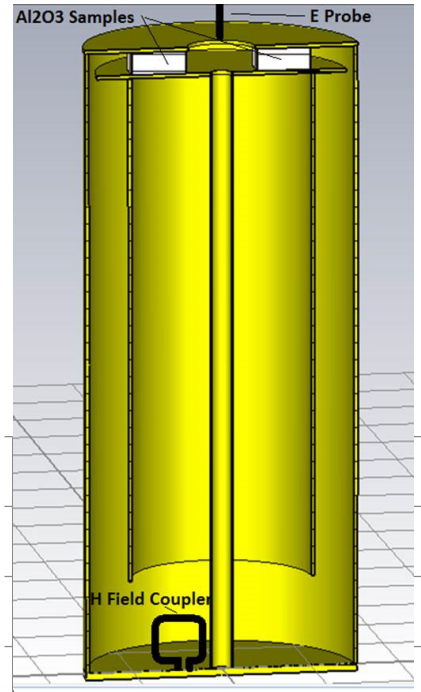


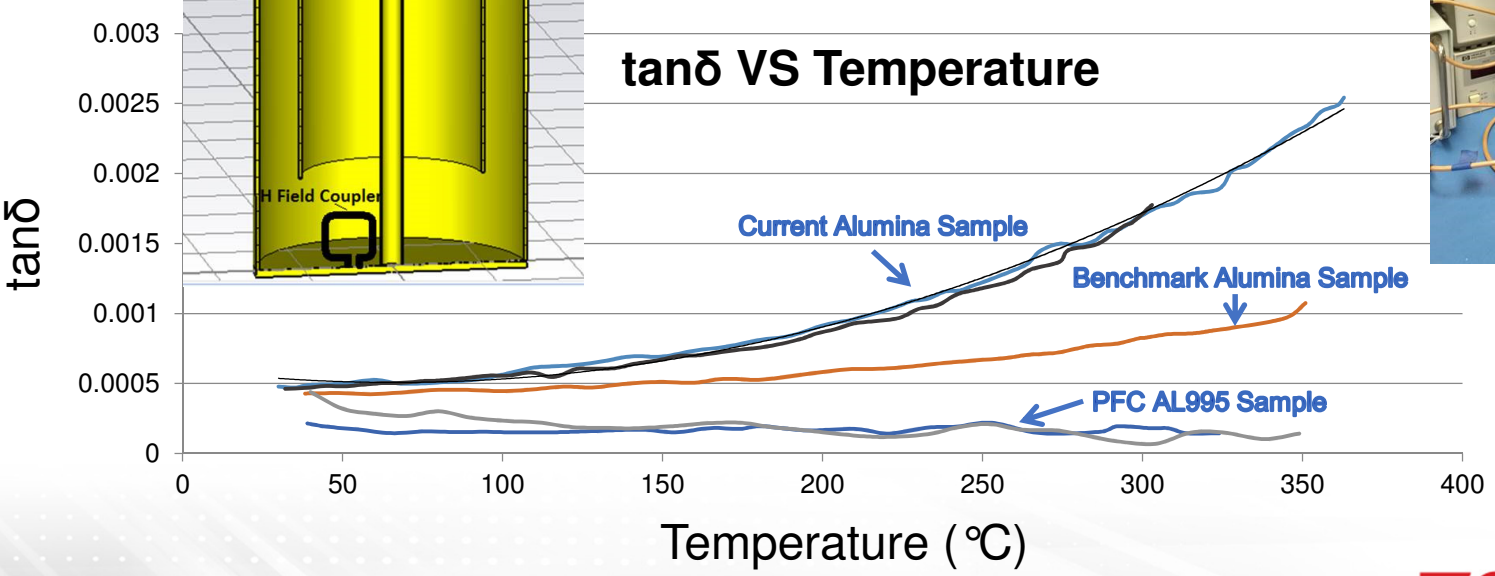
Thermal image taken through CaF_2 window
Max calibrated internal temp ≈ 70C @ 55kV

End result of window heating is cavity Q degradation and thermal runaway above 72kV

New 9MHz System Current Efforts

Dielectric Material Test Cavity (50MHz)

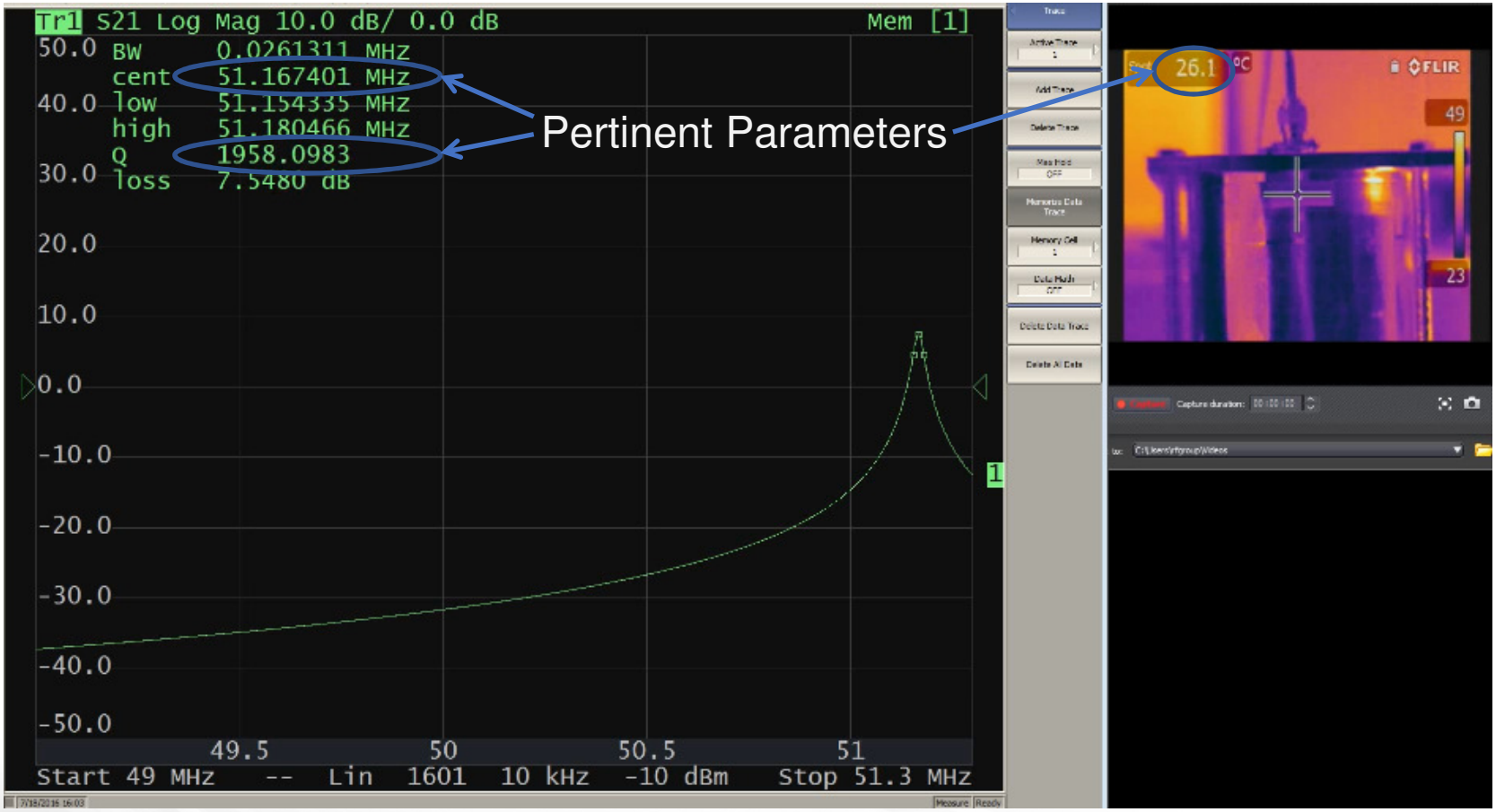




New 9MHz System Current Efforts

Dielectric Material Test Cavity (50MHz)

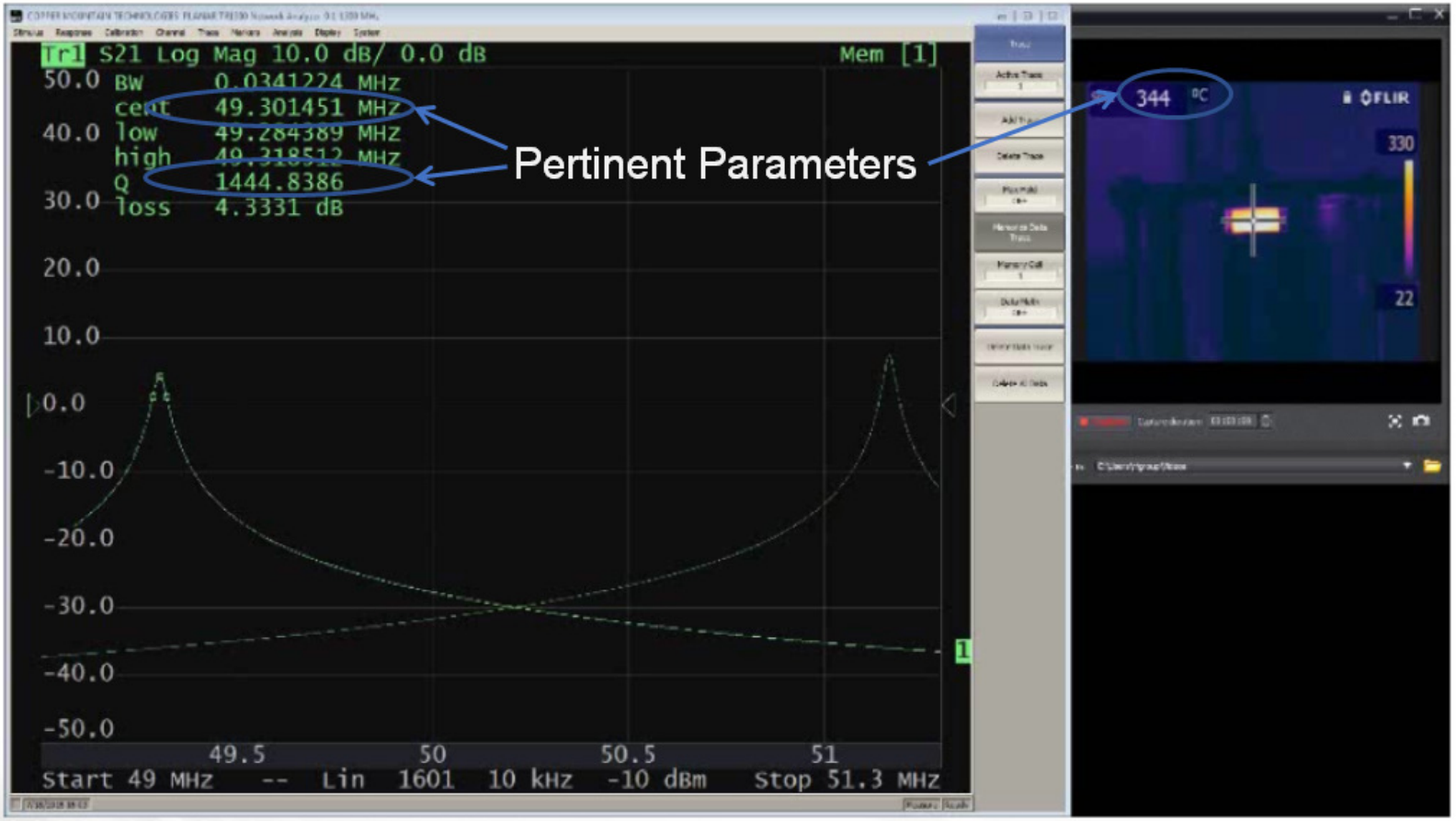
Bare Cavity (Picture)



New 9MHz System Current Efforts

Dielectric Material Test Cavity (50MHz)

Testing RF1080 Sample 2 (Video)



New 9MHz System Conclusions

- Summary
  - Overall the new 9MHz systems performed reliably during the FY17 PP run
  - High intensity fast ramping fills provided a good test of system design margins
  - Current efforts are focused on the enhancement of peak voltage margin
    - LEReC CW Voltage Requirement = 53.4kV (160kV per ring)
    - Current CW Voltage Limit ≈ 72kV CW (Goal = 80kV)

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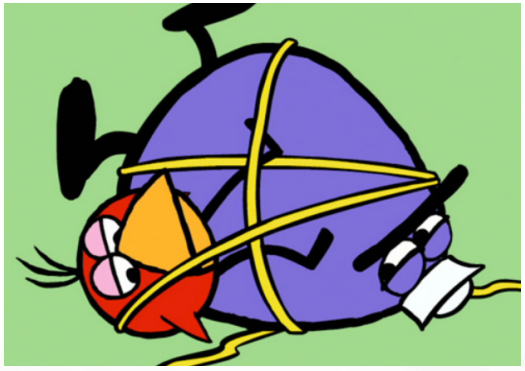
This is for ~~if~~ when we find ourselves in a bind.



Thank you