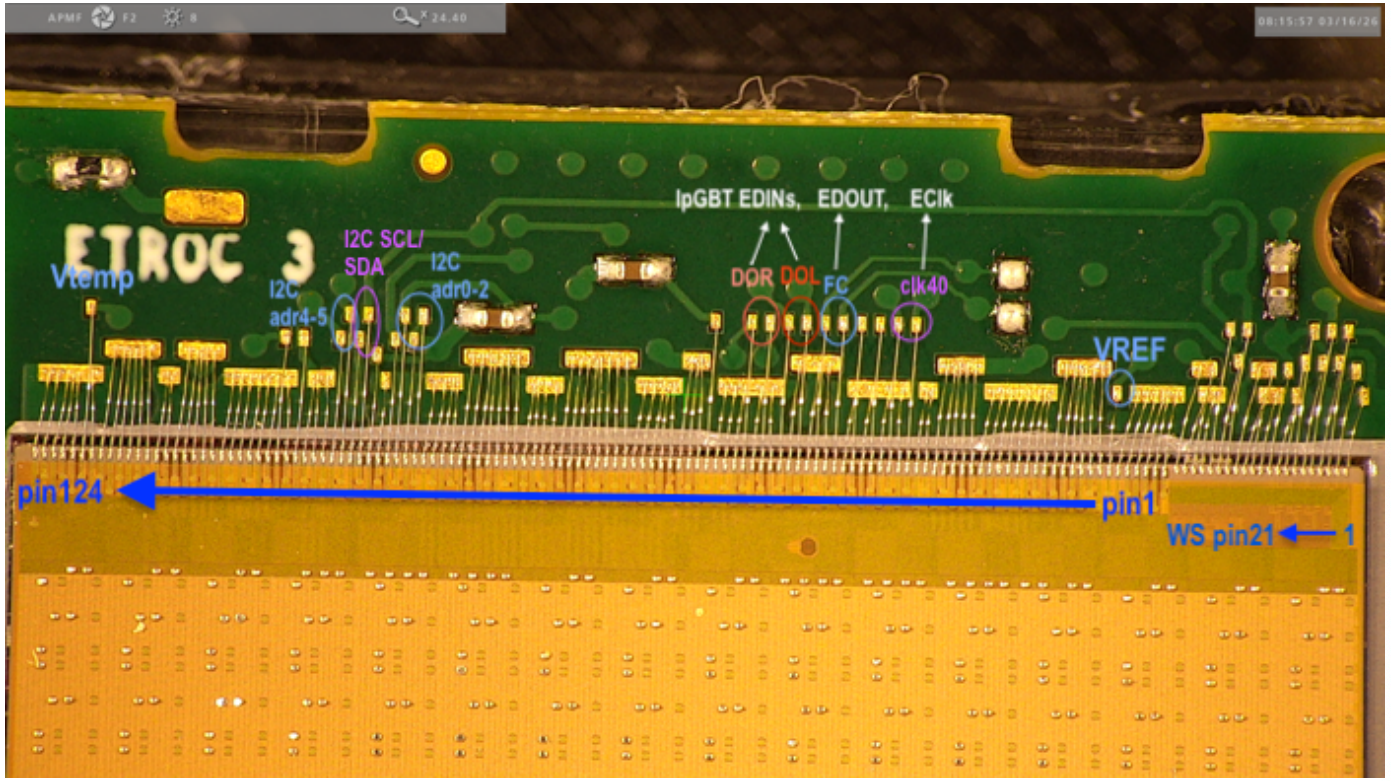
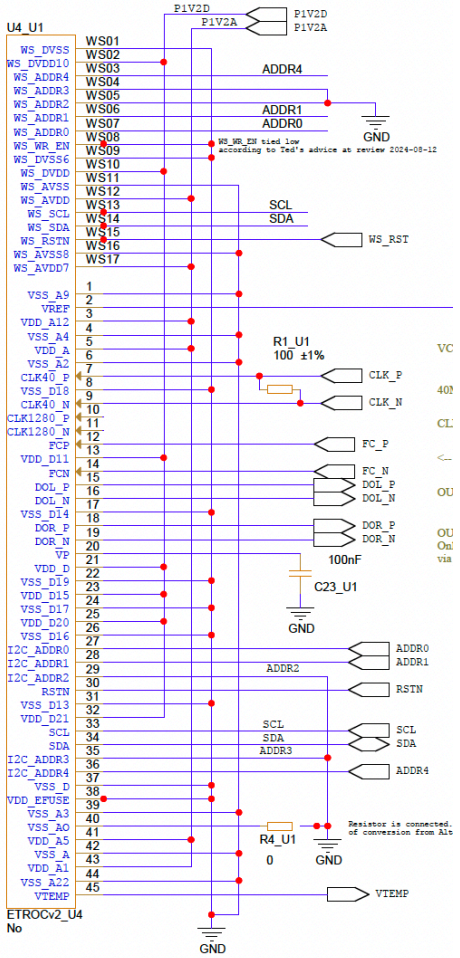
FTOF RDO Testing at Rice

April 17, 2026

ETL ETROC Wire-Bond





- ETROC:
  - Dimensions: 21x23 mm^2 with 16x16 pixels in 20.8x20.8 mm^2; thickness of die: ~280 μm
  - Main signals: 124 rectangular pads with pad pitch of 143 μm and opening of 70x200 μm^2
  - Waveform sampler: 21 rectangular pads with pitch of 130 μm and opening of 70x116 μm^2
- Module board: 45 signals for main part and 17 for Waveform Sampler (WS)
  - Some signals from ETROC are grouped into one pad: typical for digital 1.2V and corresponding GND, analog 1.2V and its GND
  - On module board, all digital 1.2V from same digital 1.2V and all analog 1.2V from same analog 1.2V, the GND is shared, w/wo termination

ETROC Pins and Module Board Pads

Begin of Table 22

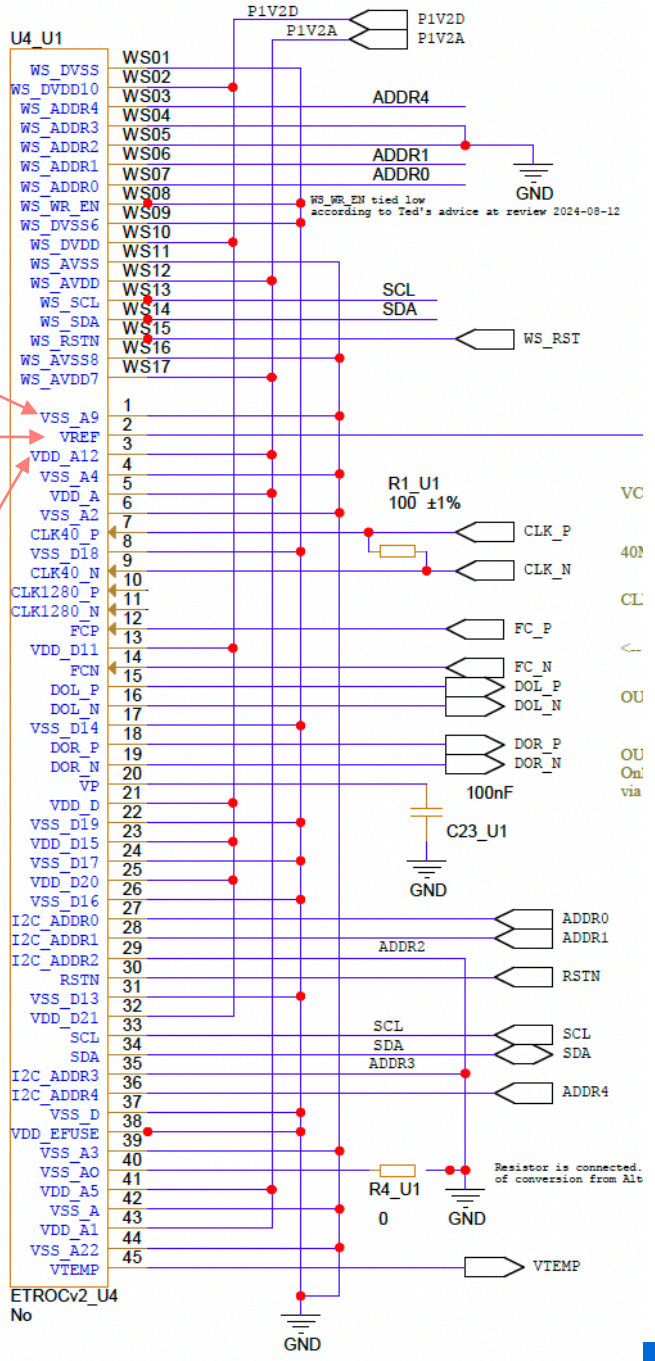
Num.	Internal Name	External Name	Category	Description	rectangular pad center coordinates (μm)	octagon pad center coordinates (μm)
1	VSS_PA	VSS_A	Power	Preamplifier ground, 0V	(3100, 155)	(3100, 505)
2	VSS_PA	VSS_A	Power	Preamplifier ground, 0V	(3243, 155)	(3243, 723)
3	VSS_PA	VSS_A	Power	Preamplifier ground, 0V	(3386, 155)	(3386, 505)
4	VSS_PA	VSS_A	Power	Preamplifier ground, 0V	(3529, 155)	(3529, 723)
5	VSS_PA	VSS_A	Power	Preamplifier ground, 0V	(3672, 155)	(3672, 505)
6	VSS_IO1	VSS_A	Power	analog ESD ground, 0 V	(3815, 155)	(3672, 723)
7	VREF	VREF	Analog Input/output	voltage reference, 1V. Monitoring the on-chip reference or receiving from external reference, or providing 1 V off-chip reference	(3958, 155)	(3958, 505)
8	VDD_PA	VDD_A	Power	Preamplifier supply, nominally 1.2 V	(4101, 155)	(4101, 723)
9	VDD_PA	VDD_A	Power	Preamplifier supply, nominally 1.2 V	(4244, 155)	(4244, 505)
10	VDD_PA	VDD_A	Power	Preamplifier supply, nominally 1.2 V	(4387, 155)	(4387, 723)
11	VDD_PA	VDD_A	Power	Preamplifier supply, nominally 1.2 V	(4530, 155)	(4530, 505)
12	VDD_PA	VDD_A	Power	Preamplifier supply, nominally 1.2 V	(4673, 155)	(4673, 723)

72

ETROC2 Reference Manual 4 PINOUT

Continuation of Table 22

Num.	Internal Name	External Name	Category	Description	rectangular pad center coordinates (μm)	octagon pad center coordinates (μm)
13	VDD_Qinj	VDD_A	Power	Charge injector supply, nominally 1.2 V	(4816, 155)	(4816, 505)
14	VSS_IO1	VSS_A	Power	analog ESD ground, 0 V	(4959, 155)	(4959, 723)
15	VSS_Qinj	VSS_A	Power	Charge injector ground, 0 V	(5102, 155)	(5102, 505)
16	VSS_Dis	VSS_A	Power	Discriminator ground, 0 V	(5245, 155)	(5245, 723)
17	VSS_Dis	VSS_A	Power	Discriminator ground, 0 V	(5388, 155)	(5388, 505)
18	VSS_Dis	VSS_A	Power	Discriminator ground, 0 V	(5531, 155)	(5531, 723)
19	VSS_Dis	VSS_A	Power	Discriminator ground, 0 V	(5674, 155)	(5674, 505)
20	VSS_Dis	VSS_A	Power	Discriminator ground, 0 V	(5817, 155)	(5817, 723)
21	VSS_IO1	VSS_A	Power	Analog ESD ground, 0 V	(5960, 155)	(5960, 505)
22	VDD_Dis	VDD_A	Power	Discriminator supply, nominally 1.2 V	(6103, 155)	(6103, 723)
23	VDD_Dis	VDD_A	Power	Discriminator supply, nominally 1.2 V	(6206, 155)	(6206, 505)
24	VDD_Dis	VDD_A	Power	Discriminator supply, nominally 1.2 V	(6389, 155)	(6389, 723)
25	VDD_Dis	VDD_A	Power	Discriminator supply, nominally 1.2 V	(6532, 155)	(6532, 505)
26	VDD_Dis	VDD_A	Power	Discriminator supply, nominally 1.2 V	(6675, 155)	(6675, 723)
27	VSS_S	VSS_A	Power	Ground for substrate, 0 V	(6818, 155)	(6818, 723)
28	VSS_S	VSS_A	Power	Ground for substrate, 0 V	(6916, 155)	(6916, 505)



Wire-bond between ETROC Pins and Module Board Pads

ETROC Main Pins	Module board	Description
VSS_PA, 1-6	VSS_A9	Preamplifier ground
VREF, 7	VREF	1V Ref for threshold
VDD_PA, 8-13	VDD_A12	Preamplifier PS, 1.2V
VSS_DIS, 14-21	VSS_A4	Discriminator ground
VDD_Dis, 22-26	VDD_A	Discriminator PS, 1.2V
VSS_S, 27-28	VSS_A2	Substrate GND
CLK40p/n, 29/31	CLK40_P/N	CLK40
VSS_SL, 30, 32, 34, 36	VSS_D18	Serial link GND
CLK1280p/n, 33/35	CLK1280p_P/N	CLK1280, Unused
FCp/n, 37/39	FCP/N	Fast control
VDD_SL, 38, 40, 42, 44	VDD_D11	Serial link PS, 1.2V
DOLp/n, 41/43	DOL_P/N	Left side data output
DORp/n, 45/ 47	DOR_P/N	Right side data output
VSS_IO/CLK, 44, 46, 48-50	VSS_D14	IO, CLK GDN
VP, 51	VP	VCP supply stabilization
VDD_CLK, 53-54	VDD_D	Clock gen PS, 1.2V

ETROC Main Pins	Module Board	Description
VSS_D, 56-59	VSS_D19	Digital core GND
VDD_D, 60-67	VDD_D15	Digital core PS, 1.2V
VSS_D, 68-71	VSS_D17	Digital core GND
VDD_D, 72-78	VDD_D20	Digital core PS, 1.2V
VSS_D, 79-82	VSS_D16	Digital core GND
I2CAddr0/1/2, 83/84/85	I2C_ADDR0/1/2	I2C address 0-2
RSTn, 86	RSTN	I2C reset, active low
VSS_IO2, 87	VSS_D13	Digital GND
VDD_IO2, 88	VDD_D21	Digital PS, 1.2V
SCL/SDA, 89/90	SCL/SDA	I2C data
I2CAddr3/4, 91/92	I2C_ADDR3/4	I2C address 3-4
VSS_D, 93-95	VSS_D	Digital core GND
VDD_EFUSE, 96	VDD_EFUSE	EFuse PS, 2.5V
VSS_S, 98	VSS_A3	Aluminum shielding GND
VSS_Dis, 97, 99-104	VSS_A0	Discriminator GND
VDD_Dis, 105-109	VDD_A5	Discriminator PS, 1.2V
VSS_IO, 110-111	VSS_A	Analog ESD GND
VDD_PA, 112-117	VDD_A1	Preamplifier PS, 1.2V
VSS_IO, 118, 120-124	VSS_A22	ESD/Preamplifier GND
VTEMP, 119	VTEMP	VTEMP

ETROC, Waveform Sampler Pins	Module Board	Description
DVSS, 1	WS_DVSS	Digital GND
DVDD, 2	WS_DVDD10	Digital PS, 1.2V
I2C_addr[4:0], 3-7	WS_ADDR4-0	I2C address
WR_EN_EXT, 8	WS_WR_EN	External write enable
DVSS, 9	WS_DVSS6	Digital GND
DVDD, 10	WS_DVDD	Digital power, 1.2V
AVSS, 11, 13	WS_AVSS	Analog GNd
AVDD, 12, 14	WS_AVDD	Analog power, 1.2V
SCL/SDA, 15/16	WS_SCL/SDA	I2C data
RST, 17	WS_RSTN	I2C reset
AVSS, 18, 20	WS_AVSS8	Analog GND
AVDD, 19, 21	WS_AVDD7	Analog power, 1.2V

- Each ETROC has one waveform sampler (WS) to sample the pxiel's pre-amplifier output waveform at 2.56 GS/s and convert it into digital
  - ➡ 1024 points at 2.56 GS/s => 400 ns time window
- Purpose: periodically monitor LGAD signal during operation

RDOv1 ADCs

RDO ADC+MUX64 readouts with power board:

Reading DAQ lpGBT ADC values:

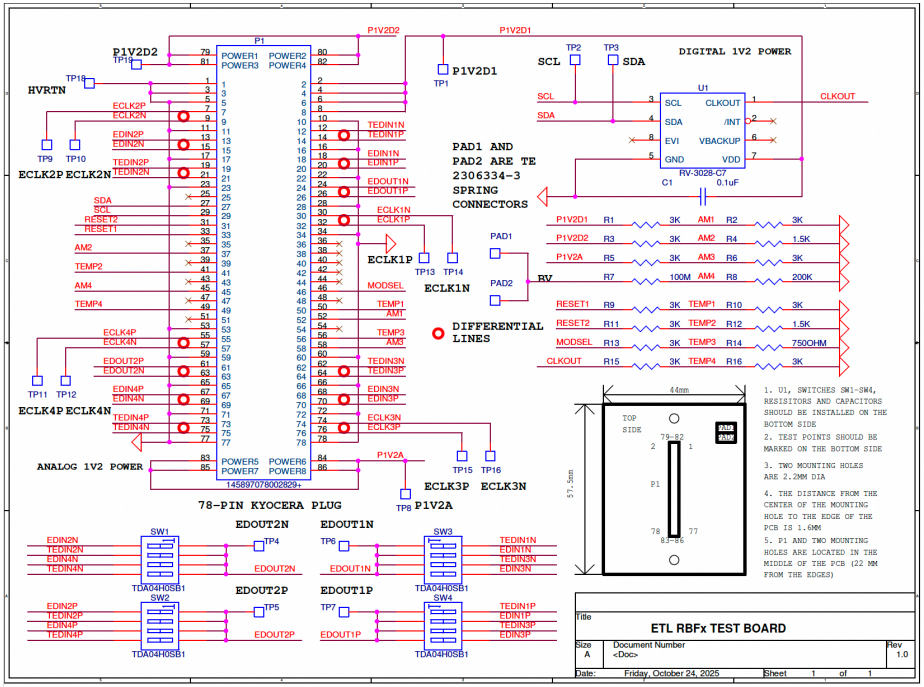
Register	Pin	Reading (raw)	Reading (calib)	Voltage (direct)	Voltage (conv)	Status	Comment
TH1	0	112	82.693	0.081	0.081	OK	VTRX TH1
MUX64OUT	1	35	0.567	0.001	0.001	OK	MUX64OUT / 2, ADC2 raw
LVRB	2	661	668.295	0.653	13.457	OK	LVRB / 20.6
2V5TX_ADC	3	820	837.897	0.819	2.457	OK	2V5TX / 3
RSSI_ADC	4	586	588.300	0.575	1.150	OK	RSSI current = 0.242 mA
1V2RA	5	570	571.229	0.558	0.558	OK	1V2RA(ADC5), RT1
2V5RX_ADC	6	818	835.763	0.817	2.451	OK	2V5RX / 3
RT2_ADC	7	434	426.163	0.417	0.417	OK	RT2
VDAC	8	993	1022.428	0.999	0.999	OK	VDAC output (internal)
VSSA	9	35	0.567	0.001	0.001	OK	VSSA, Analog ground (internal)
VDDTX	10	526	524.296	0.513	1.220	OK	VDDTX * 0.42, TX supply (internal)
VDDRX	11	527	525.367	0.514	1.222	OK	VDDRX * 0.42, RX supply (internal)
VDD	12	527	525.362	0.514	1.222	OK	VDD * 0.42, Digital supply (internal)
VDDA	13	528	526.424	0.515	1.225	OK	VDDA * 0.42, Analog supply (internal)
TEMP	14	546	545.634	0.533	0.533	OK	Temp = 35.3 C (internal signal)
VREF	15	514	511.501	0.500	1.000	OK	ADC VREF/2 (internal)

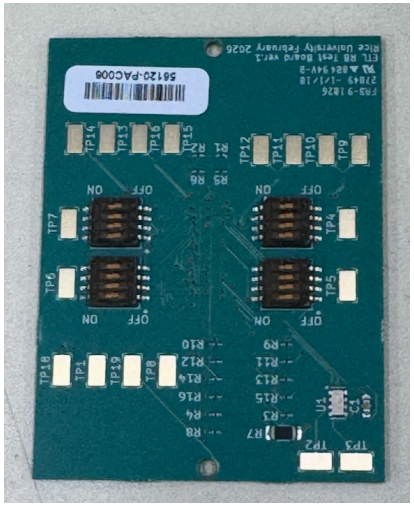
Reading MUX64 values:

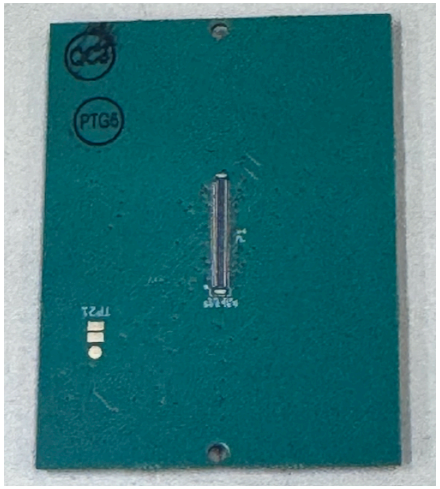
Channel	Pin	Reading (raw)	Reading (calib)	Voltage (direct)	Voltage (conv)	Comment
HVMON	31	36	1.633	0.002	1.616	HVMON
ADC2	0	335	320.570	0.313	13.229	LVRB
ADC5	1	251	230.959	0.226	0.452	Thermistor
PTAT2	32	90	59.233	0.058	0.706	PTAT2
PTAT1	33	83	51.766	0.051	0.617	PTAT1
GROUND	63	36	1.633	0.002	0.003	Background

Temperature on RB RT1 is: 33.1 C
Temperature on RB RT2 is: 28.4 C
Temperature on RB VTRX is: 30.5 C
Temprature on DAQ lpGBT is 34.9 C
This RB status: All good! Downlink Ready, Uplinks Ready, No FEC errors.

RBF Test Board



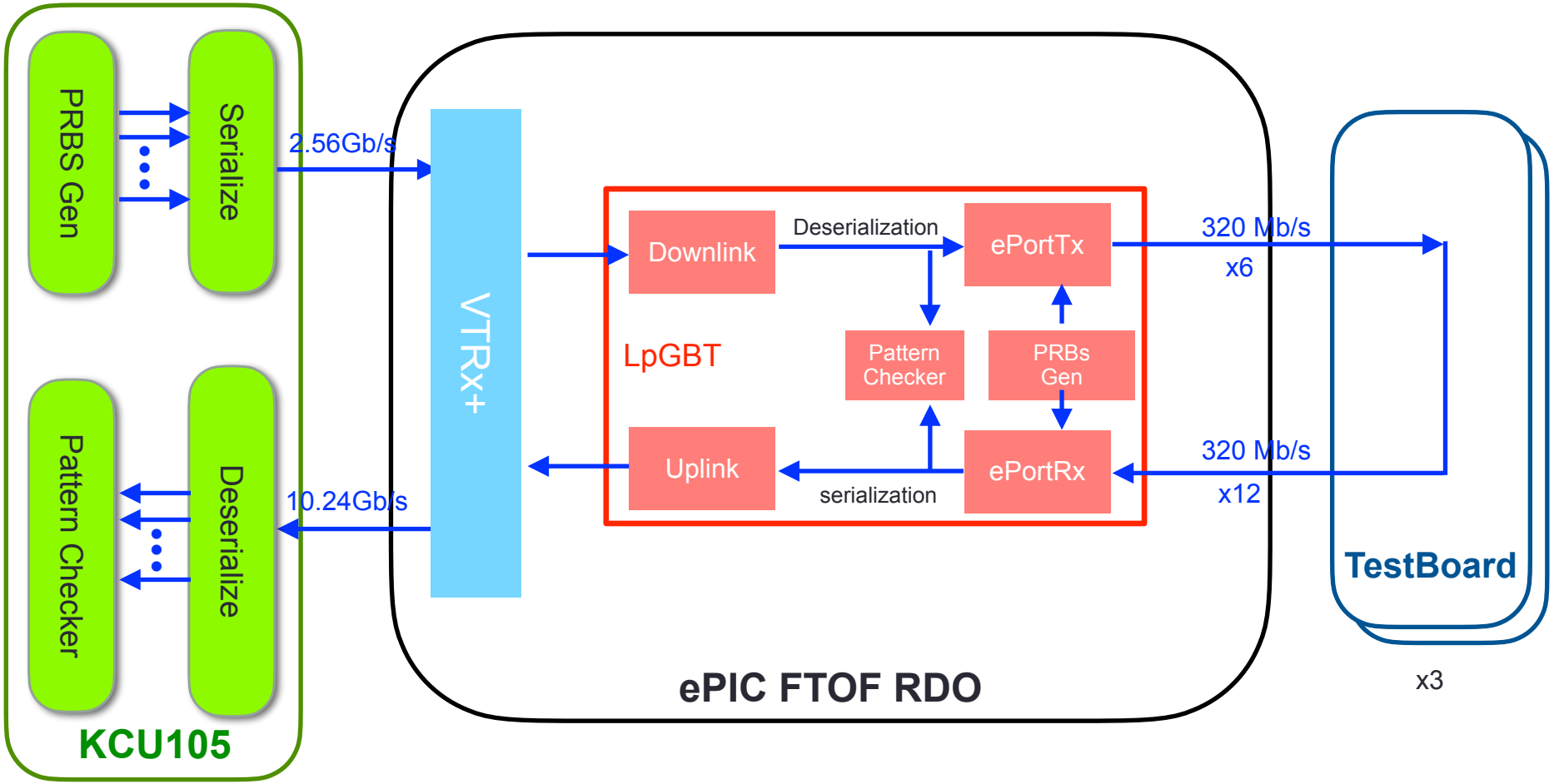




- Goal: running “loopback” test to verify the signal connections between RB and module board without using real module board
  - ➡ Analog signals like P1V2D1/P1V2D2/P1V2A etc. are read out via MUX64 by repurposing VREFs/TEMPs, and are compared to expected values during test
  - ➡ I2C communication verified via a Real-Time chip (RTC)
  - ➡ Loopback ePortTx to ePortRx for PRBs test
  - ➡ CLk40 probed by oscilloscope

PRBS Test: KCU+RDO+Testboard

Both KCU and LPGBT can generate PRBs and check PRBs



Full path loopback test: KCU PRBS generator → lpGBT downlink → lpGBT ePortTx → test board → lpGBT ePortRx → lpGBT uplinks → KCU pattern checker

The plan is to run PRBs test with test board installed in the middle location of RB3