- 1x EICROC1 Testboard with a wirebound EICROC1 is shipped to BNL
- after some thinking and emails from Mike we decided on a cautious and “least effort” approach:

1. assemble the system in the lab where the RBv1 is
   a. note: Wayne promised he’ll update the PC kernel today
2. start with ZCU106 because that’s the least effort thing to do – replicate the French setup
   a. Alex/Prithwish: do you know how to do this electronically/mechanically?
3. connect the ZCU to the daqst3 PC with JTAG and USB
   a. I will install Xilinx Vivado as soon as the PC is up to date
4. can we test the board really quickly with the French firmware??
   a. just to make sure the board is correctly powered, that the EICROC1 is working – I2C scan only
   b. Christophe tells me that the board has been checked out but NOT the lpGBT interface – that is on us
   c. I would like to assist and understand the steps but who will do this at BNL?
   d. does BNL have the French Vivado project and/or the VHDL source?
5. once these steps are done (or in parallel) I would like to take over the ZCU and put small snippets of VHDL to start checking out the lpGBT part of the EICROC1 interface
6. once I am comfortable with EICROC1 and the interfaces work and are understood we attach it to RBv1 (in the same lab) and take it from there
   a. Note: we’ll need tech help since we need to modify the Testboard to match RBv1
      i. remove some resistors to make it compatible with 1.2V, also power
      ii. Mike can explain it in details
      iii. but note that this makes the Testboard not compatible with ZCU!

Thoughts? Comments?

- EICROC1 ASIC Modules
  - Mike sent out schematics of the FTOF Module Board (4 ASICs to 1 Kyocera)
    - NOTE: we won't proceed until we seriously test EICROC1 with the French Testboard
  - lots of pins/wires will cause problems [Mike]
    - TL: some are only for testing, some won't exist in EICROC2; but not that many
    - but especially power and ground
      - Christophe: "the ASIC needs a lot of power thus a lot of power pins"...
  - size of the required area for wire-bonding is also problematic [Mike]
    - Mike eyeballed 16x5 mm^2 at the Testboard but we only have 14x4 mm^2 available for FTOF
  - some questions to ASIC designers [Mike]
    - can we float unused pins e.g. CLK160P/N?
      - I think yes but I'll check
    - status of SELFCMD?
      - I'll check…
    - EICROC2: can they add CHIPID4 to I2C?
      - I kinda recollect that they said that this is "not simple" due to the way they implemented some silicon core they took from somewhere?
      - we should start compiling a list of suggestions and/or features (as "users") for EICROC2 [TL: I'll do this so let me know]
  - TL: we also need some sort of temperature sensor on the Module Board
    - read-out by lpGBT (via MUX64?)
  - Roman Pots Module Board
    - Jack, can you provide us with your current thinking, is there a sketch?
      - 3 ASICs, right?
      - size of the board, connector?
      - cable to RBv1? Expected length?
    - timescale?

Power Tree request from the Project

- Fernando is requesting details for the so-called Power Tree of all detectors
  - usual: voltages, currents, interconnect topology, cable count, cable type, blah
  - as much as possible; some things exist from Tim
  - see yesterday's meeting
    - https://indico.bnl.gov/event/32412/
- he lumped us under "AC-LGAD" and put 6 detectors
  - BTOF, FTOF, RP, OMD, B0, Lumi PS tracker
- he put me as the "responsible person" (oddly enough) but let me know if this is OK
- it sounds like a hassle and many things already exist but I will take this opportunity to document the count of things (RBs, FEBs, ASICs) for all 6 detectors above so that we have it in 1 document
- expect emails from me because I will need the details of this stuff
  - this is especially true for FF due to my lack of knowledge (and/or bad memory :-))
- also, expect a meeting on the various power boards we have in EPIC in ~1 month
  - there's some effort in trying to standardize as much as we can (many detectors plan to use bPOL48's)
  - would be good if Mike & Jack can join – I will send out a reminder