

ESB Updates & Path Forward

Progress Report

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BIC General Meeting

April 24, 2026

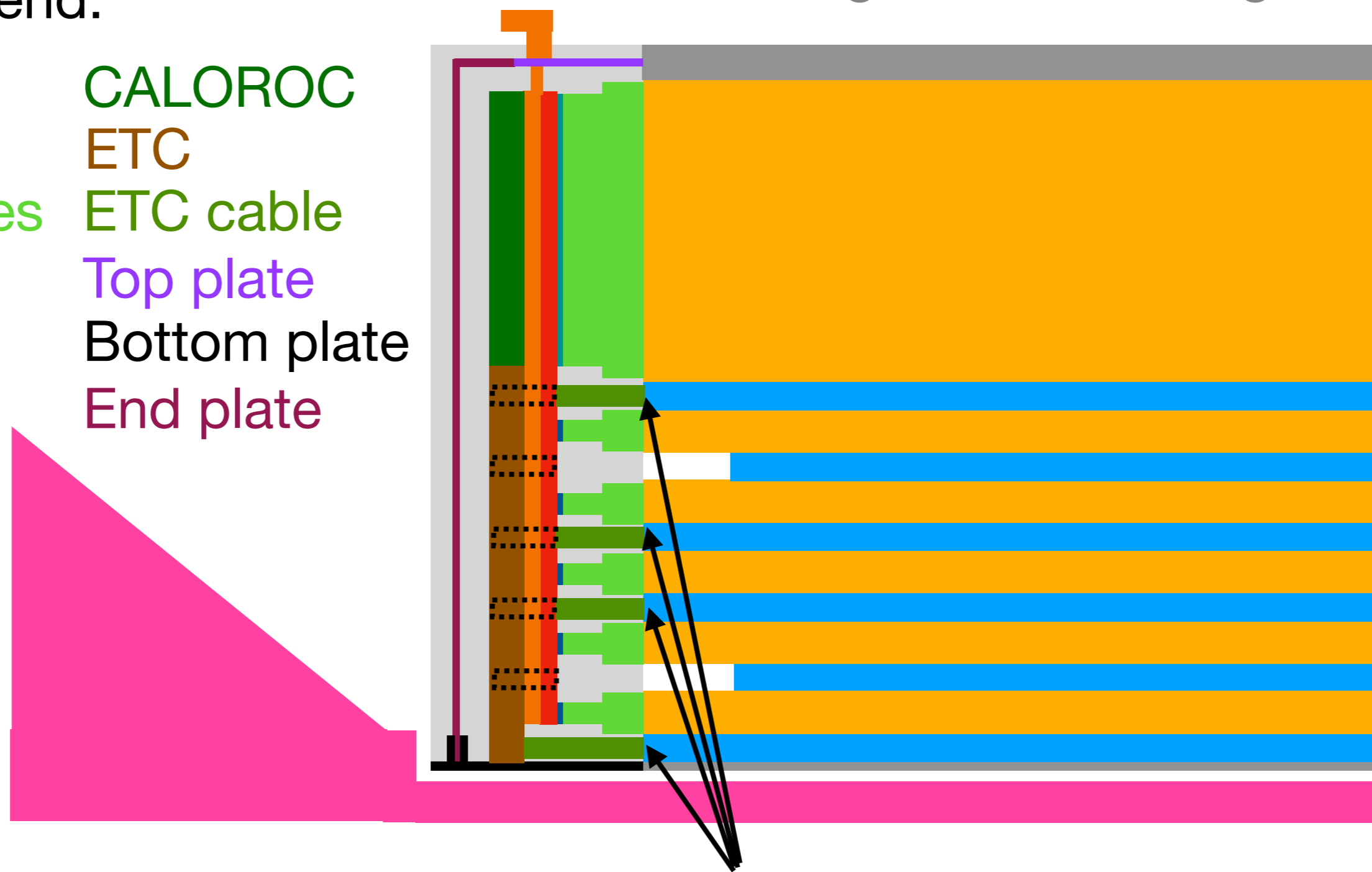
ESB Napkin Sketch - Electron End

Legend:

- PbScFi
- Astropix
- Light Guides
- Cookies
- SiPMs
- Cooling
- CALOROC
- ETC
- ETC cable
- Top plate
- Bottom plate
- End plate

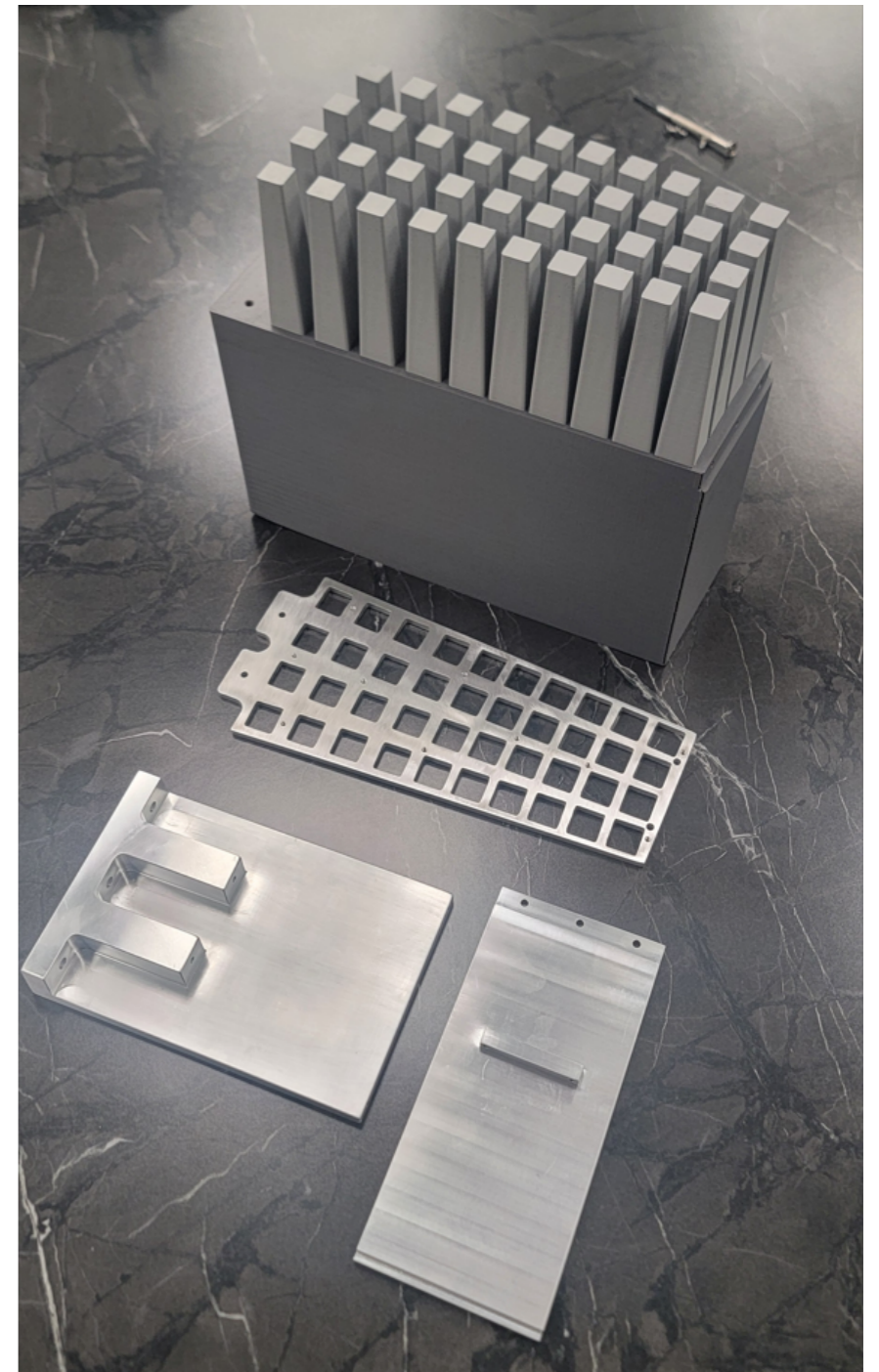
(Nasty)
DIRC

Challenge in servicing



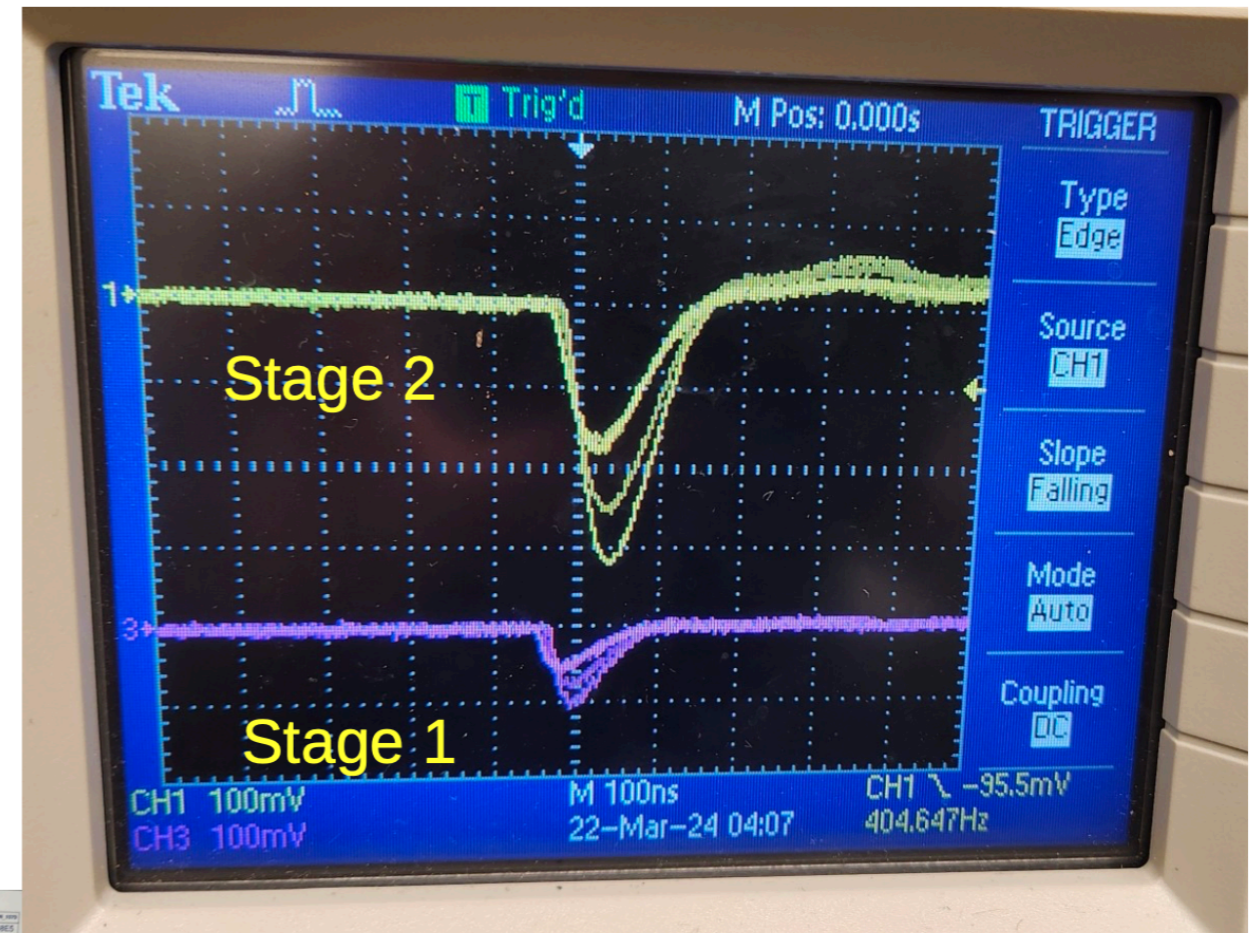
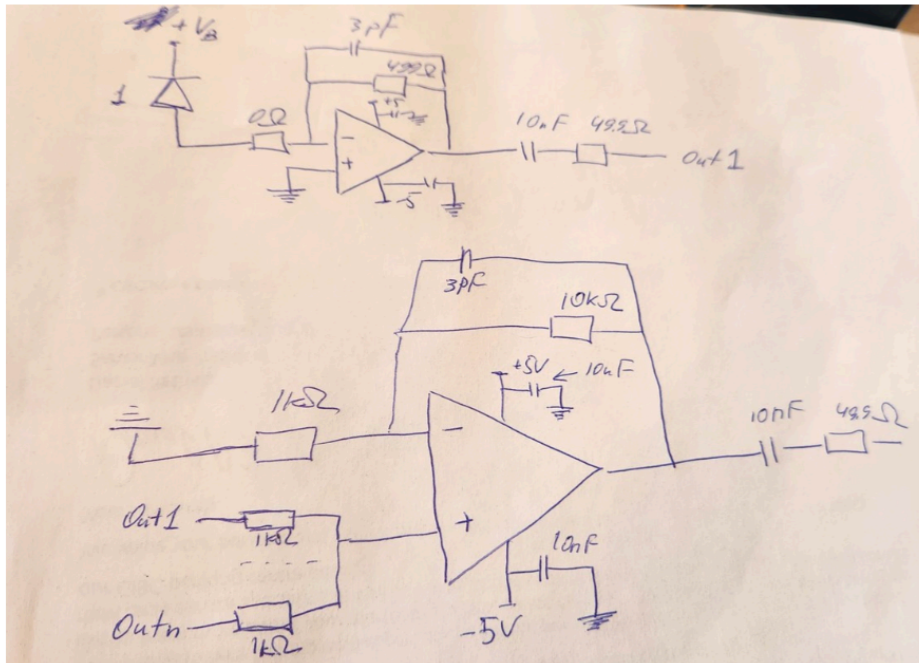
ETC to Astropix connector
ETC window thru SiPM/Cooling layers

Baby BCAL Box - Design & 3D-print mockup

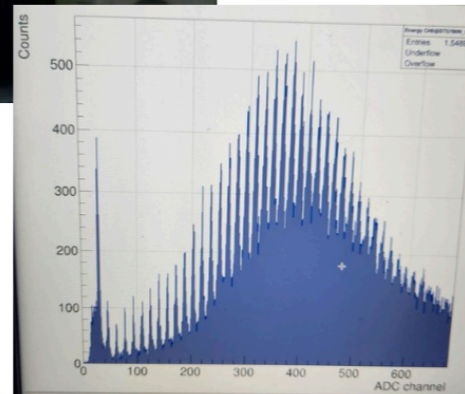


Inner plate "cancelled"?

SiPM readout basic design



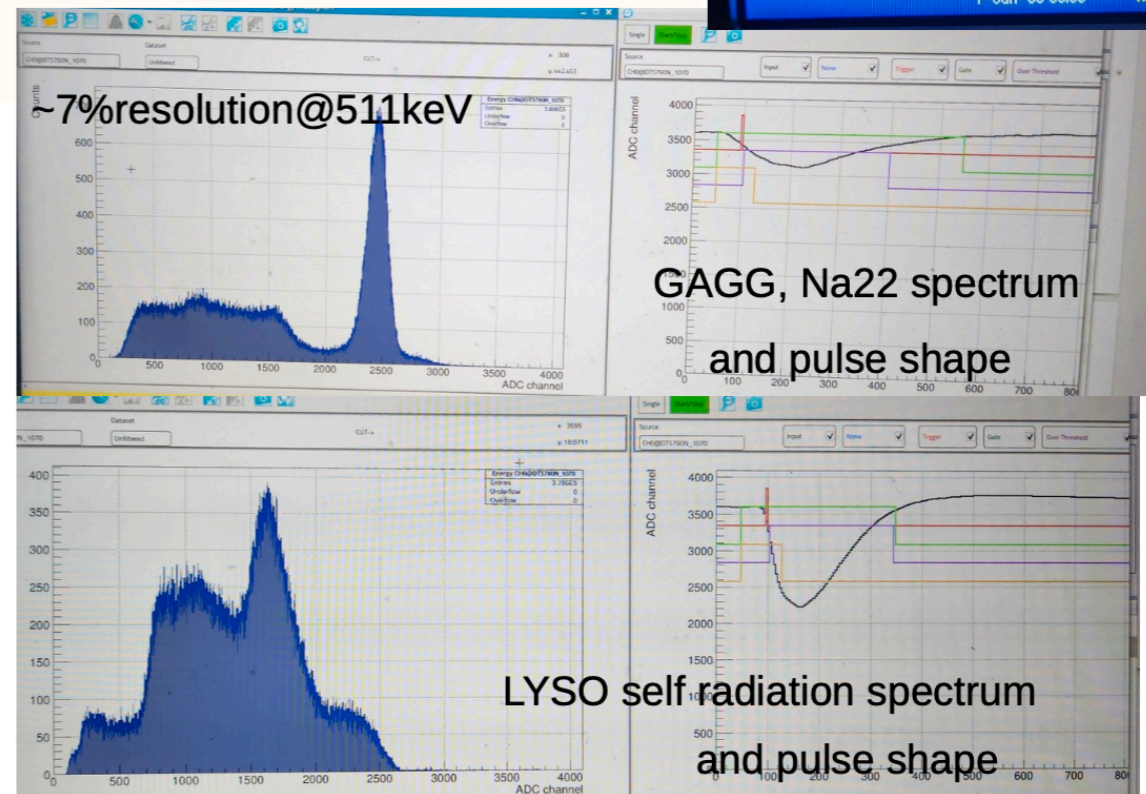
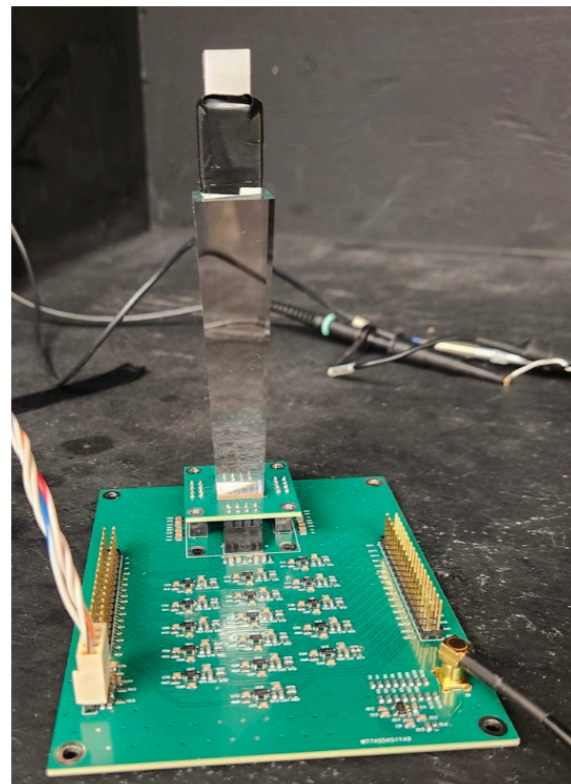
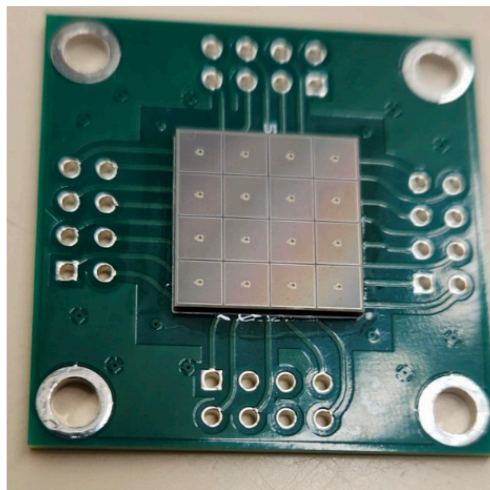
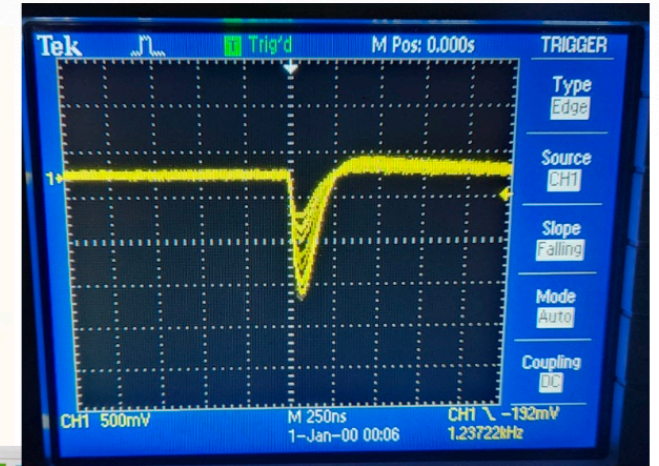
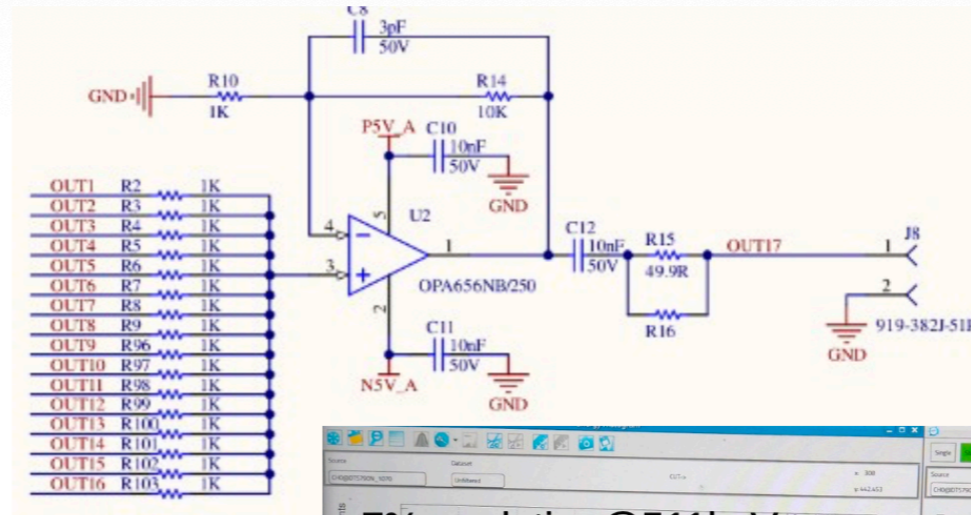
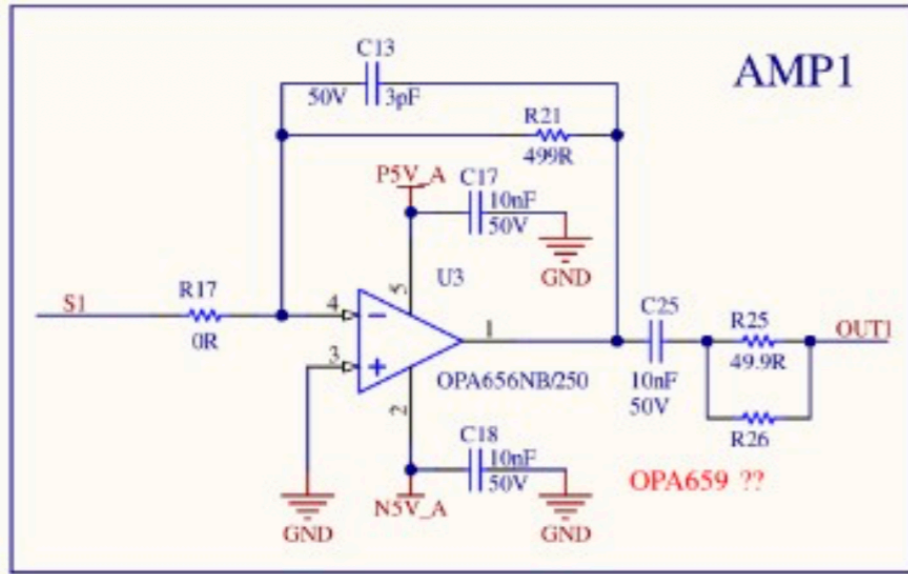
Signals clean enough to see up to 30+ single photons! Readout with CAEN DT5790



Tested with single 3x3 mm² SensL C-series sipm .. mid 2023?

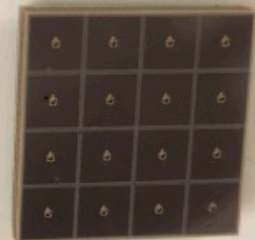
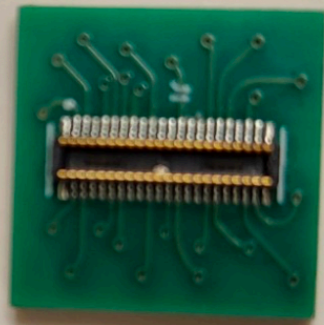
Disipated power ~0.3W per sipm

SipM 16 channel readout

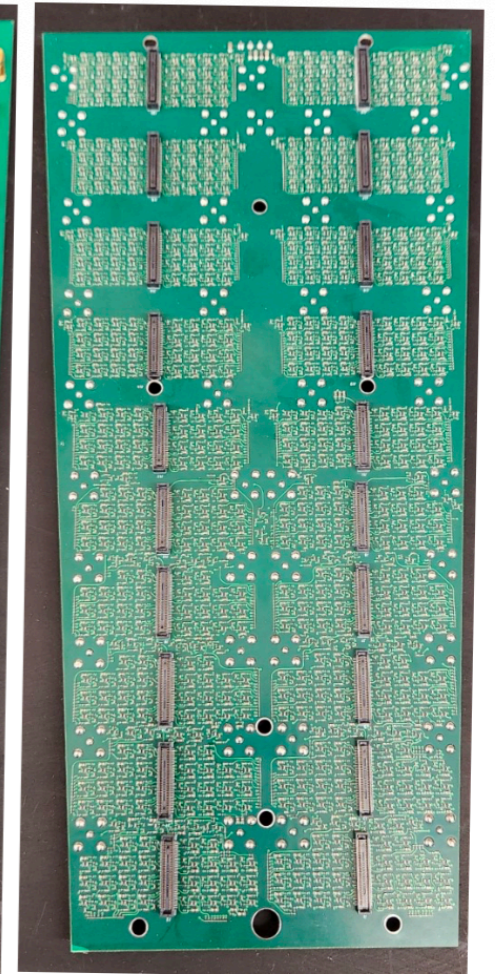
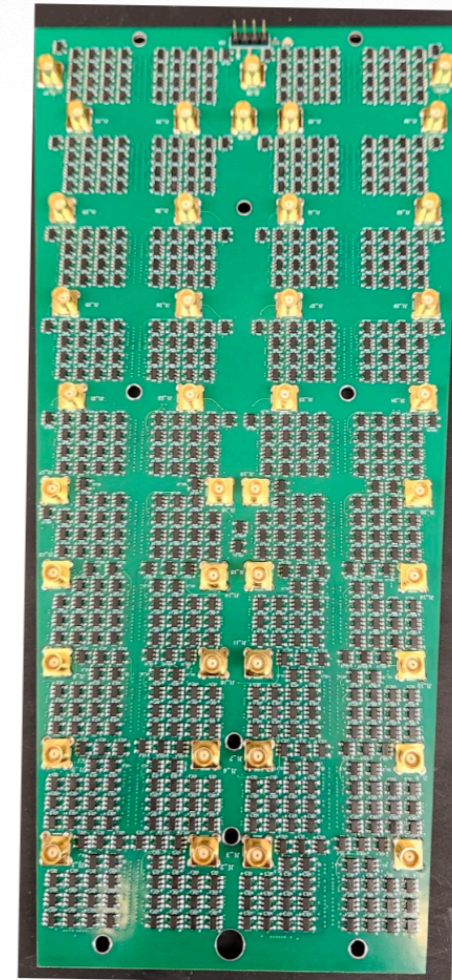
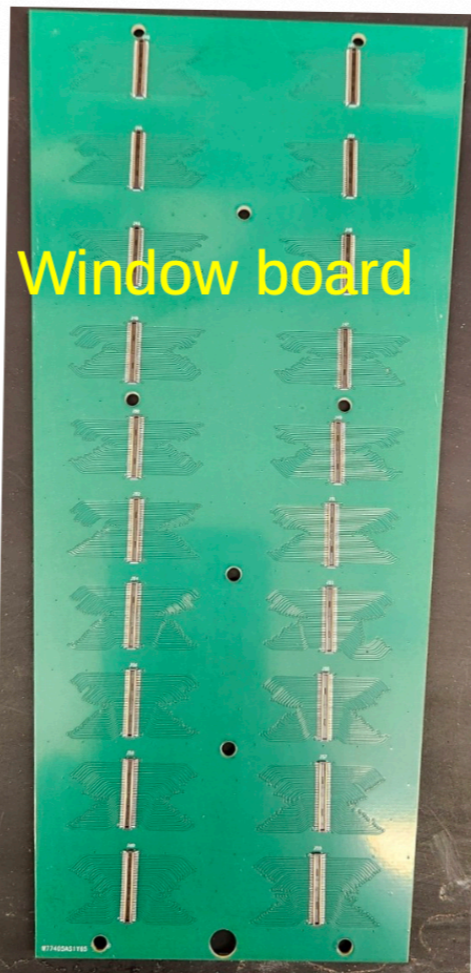


Good resolution but a **power hog ~2.5W per 4x4 sipm array!!**

Baby BCAL readout based on 16 channel readout

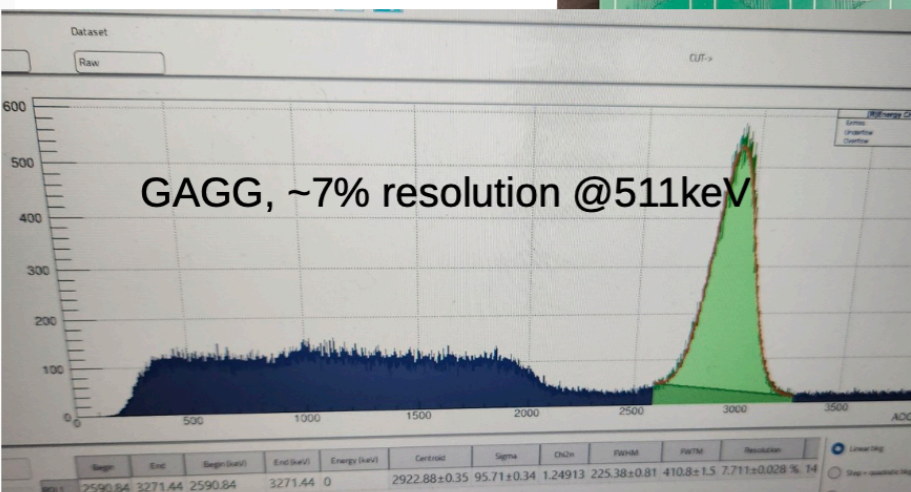


Mini-board



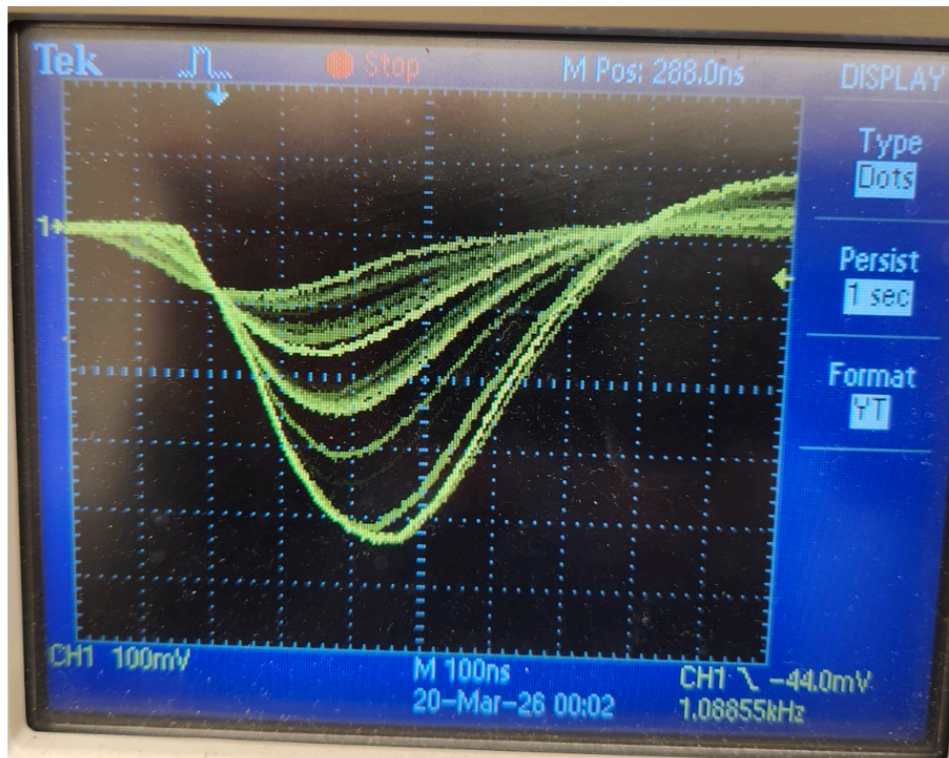
Amplifier board for 40 sipm arrays
16 channels each.
Only ~8W! For entire board

GAGG, ~7% resolution @511keV



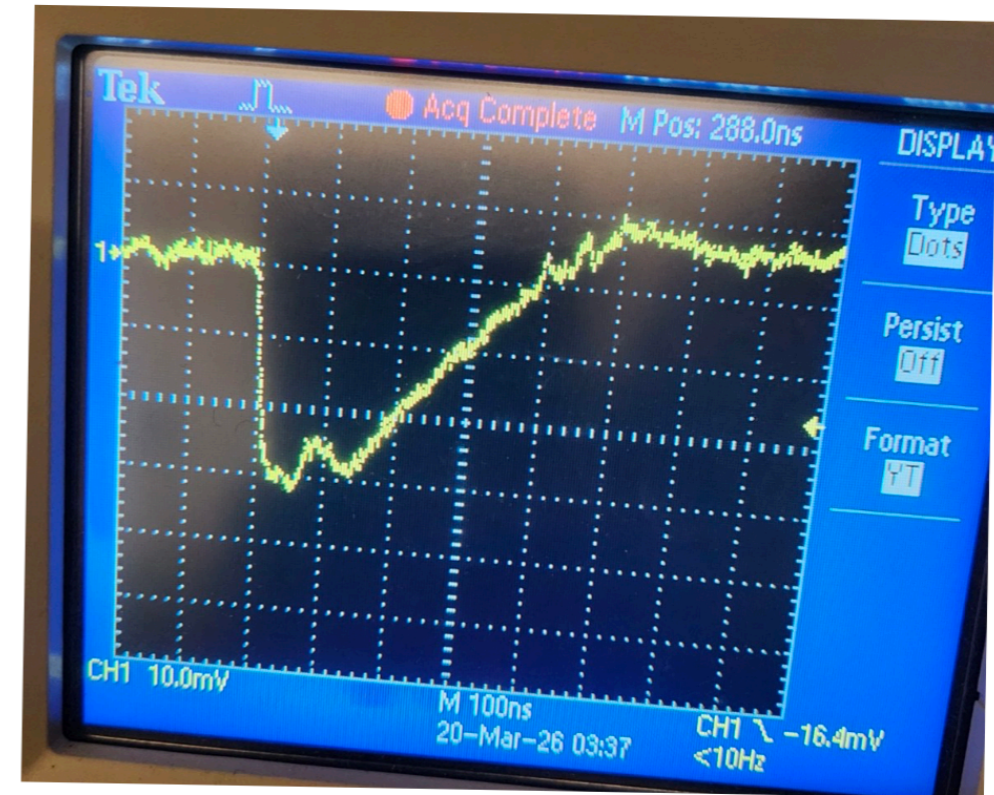
Boards to be tested at JLab

Baby BCAL readout based on 16 channel readout



GAGG, pulse shape of 16 sipm SUM with ^{22}Na source

- Pulses are ~500-600ns at the base
- Rise time ~130ns (88ns is the scintillator)



Pulse shape of a scintillating fiber matrix in LEAD (small piece of a GlueX detector prototype)-- poor optical contact

- Very fast rise time!
- Pulses are <400ns at the base

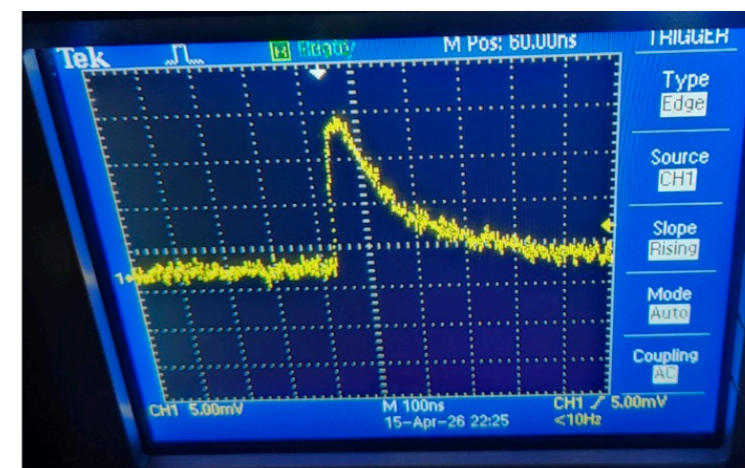
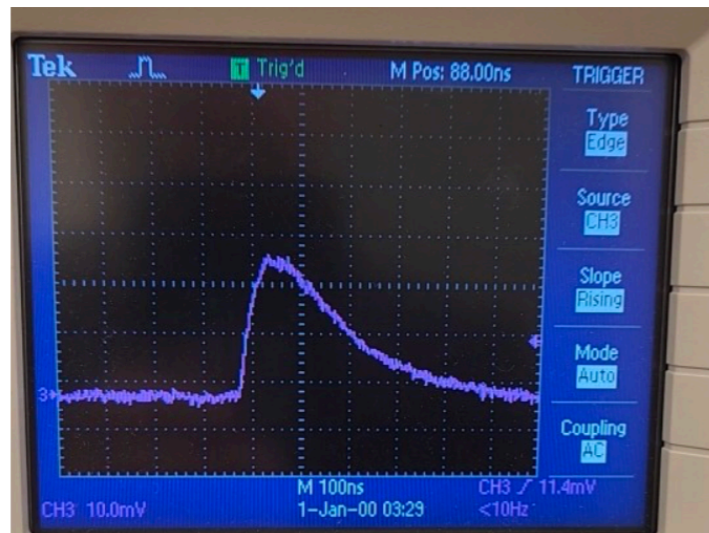
Currently aim is to further reduce the power consumption

1- Resistive /passive first stage per SiPM pixel followed by a summing/amplification stage

- Low power consumption
- Decent timing properties
- Potentially prone to crosstalk between pixels

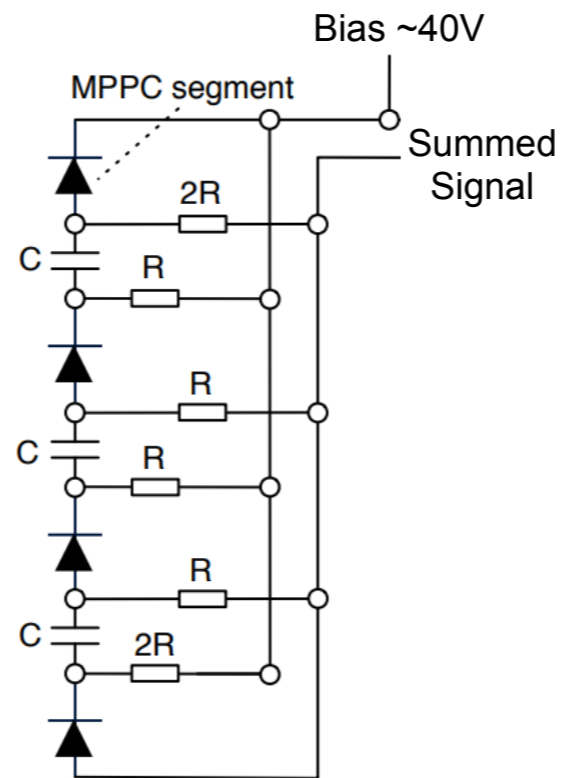
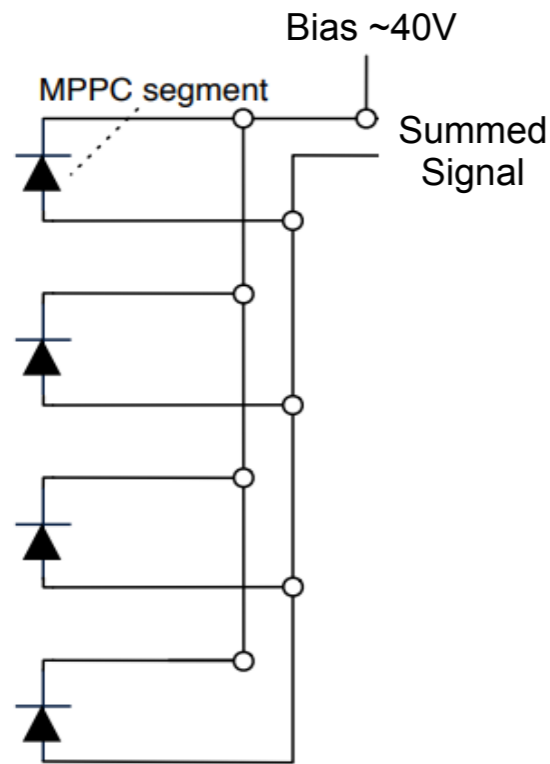
2 - Diode coupled first stage per SiPM pixel followed by a summing/amplification stage

- Low power consumption
- Decent timing properties
- Almost completely eliminates crosstalk between pixels

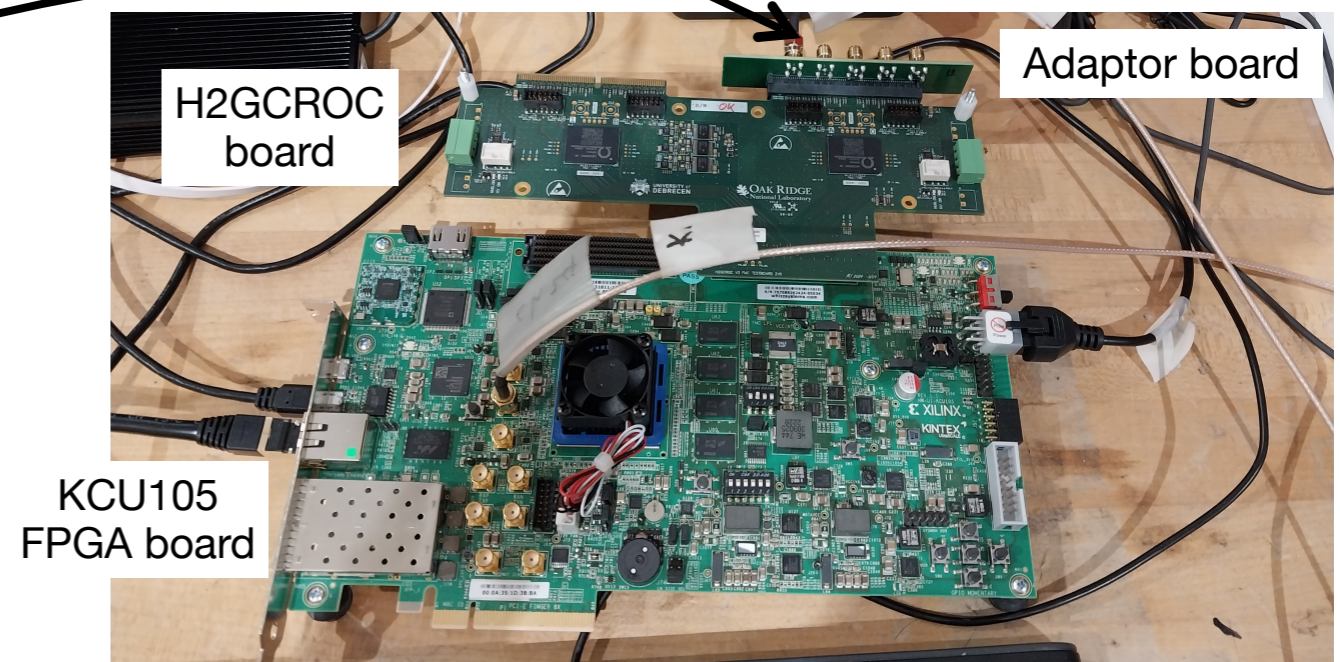
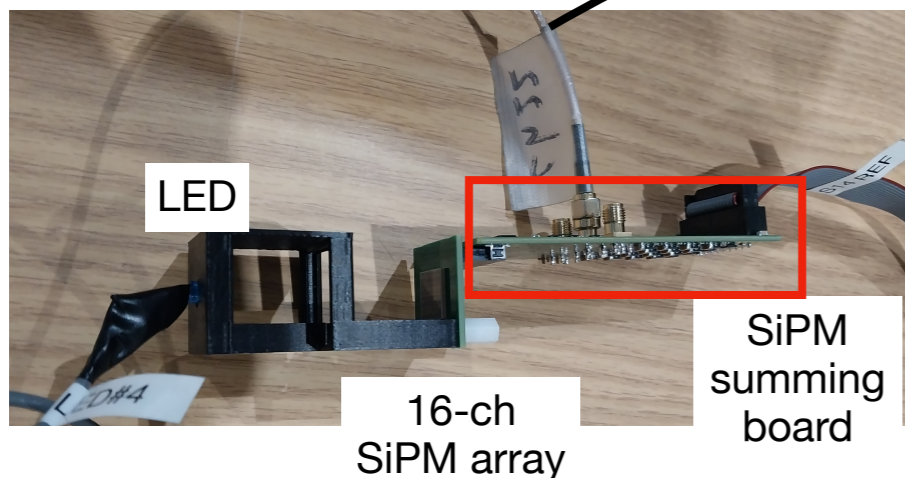


H2GCROC SiPM summing board

- 16-ch parallel sum
- 16-ch hybrid sum
- 1-ch Individual

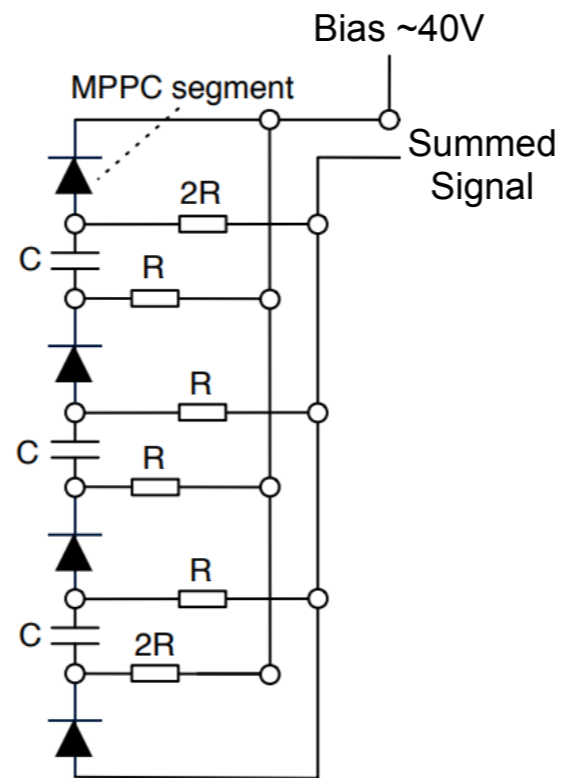
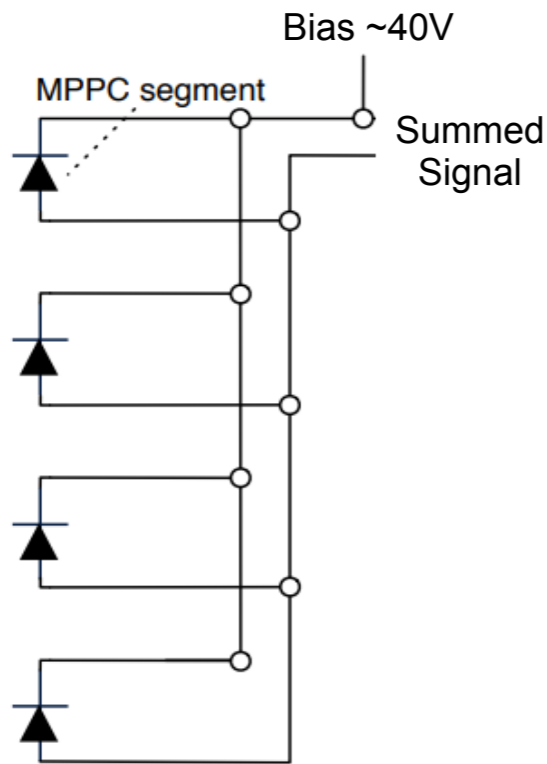


- Test setup

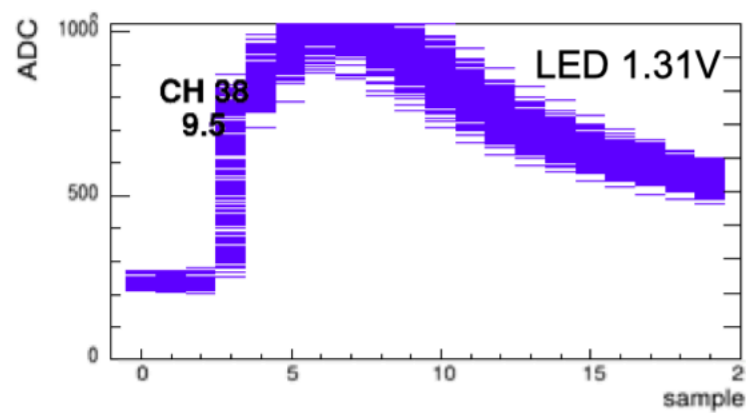


H2GCROC SiPM summing board

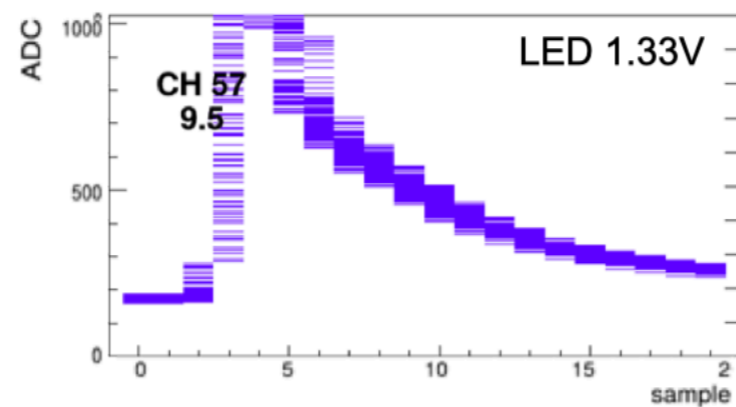
- 16-ch parallel sum
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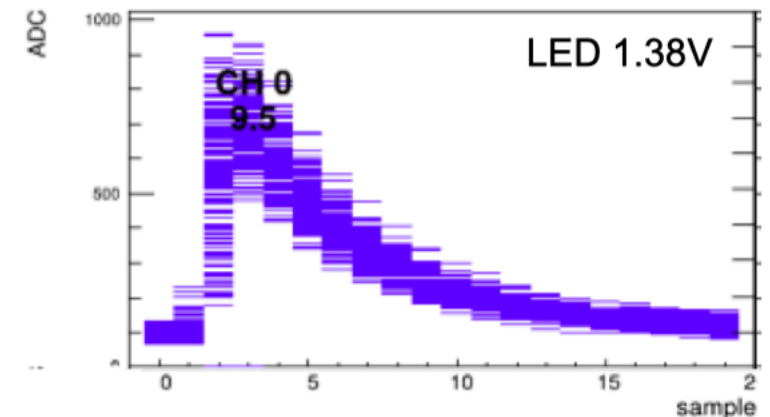
Results



- rising time: 75 ns
- falling time: ~1 μ s

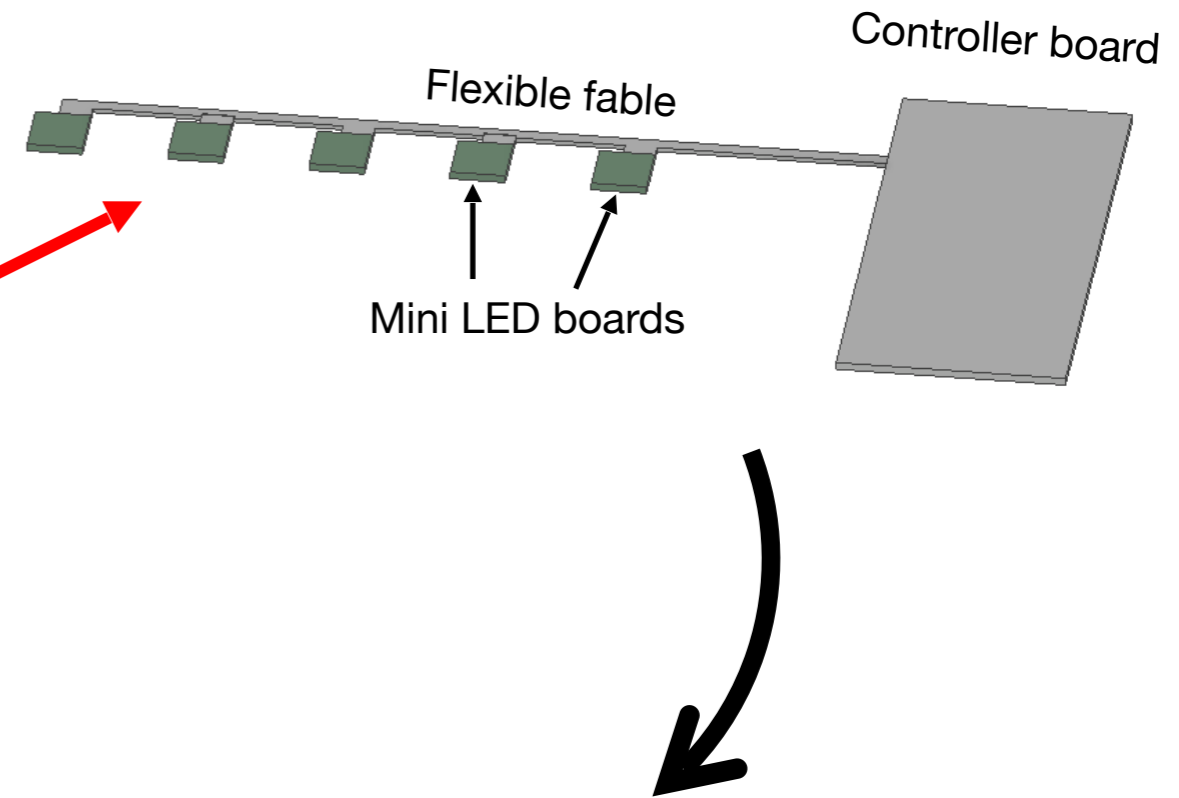
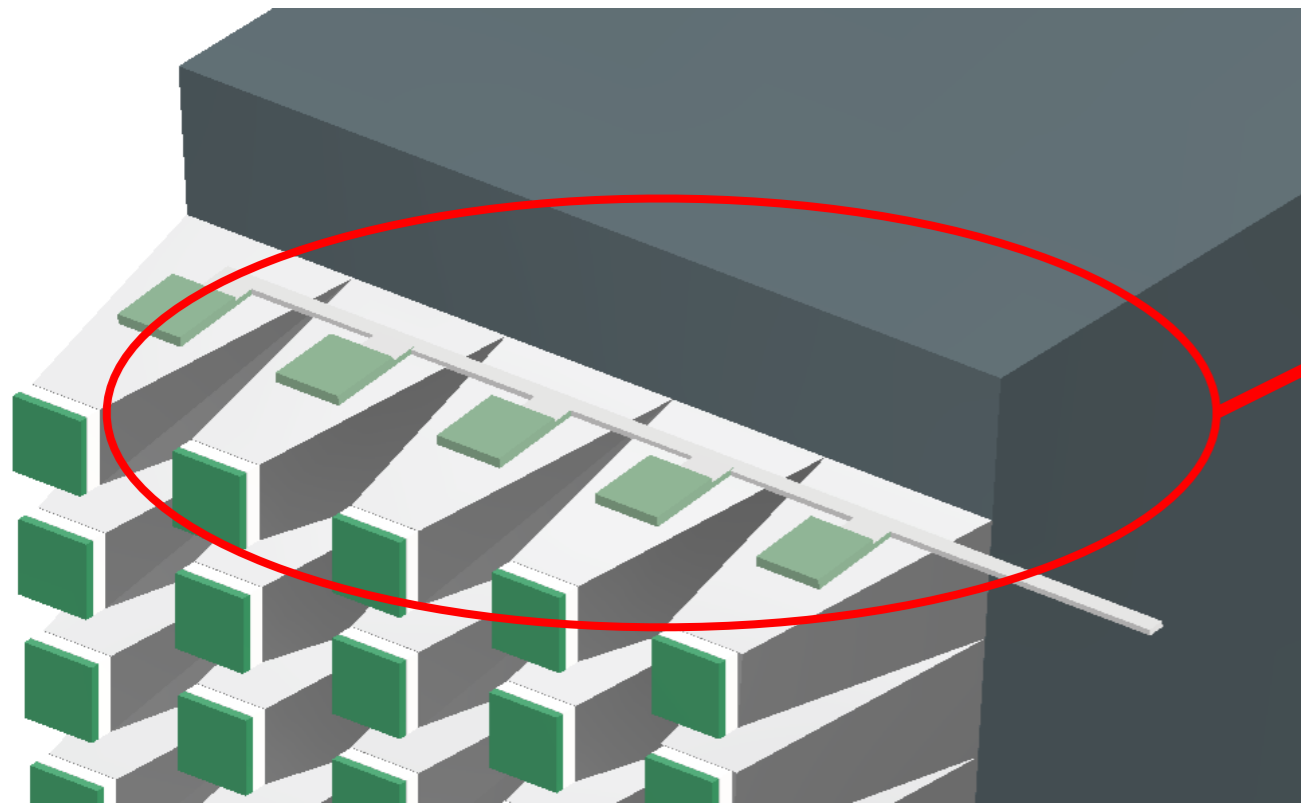


- rising time: 25 ns
- falling time: ~300 ns



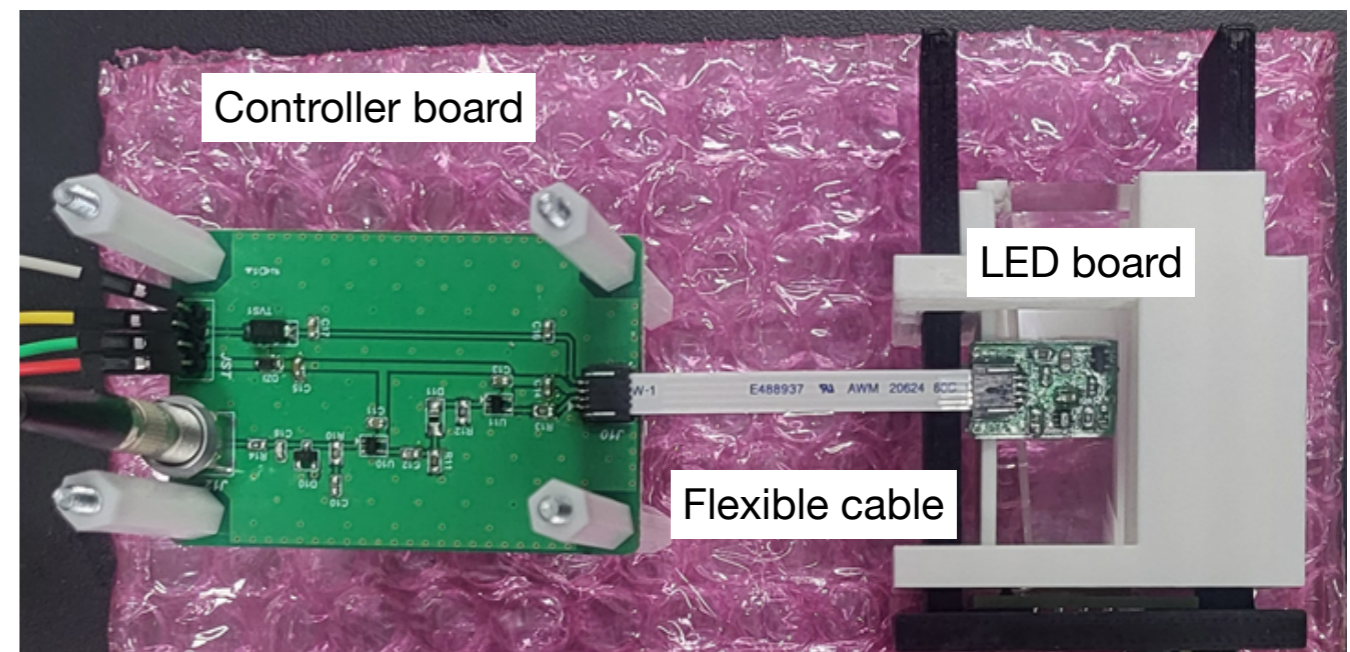
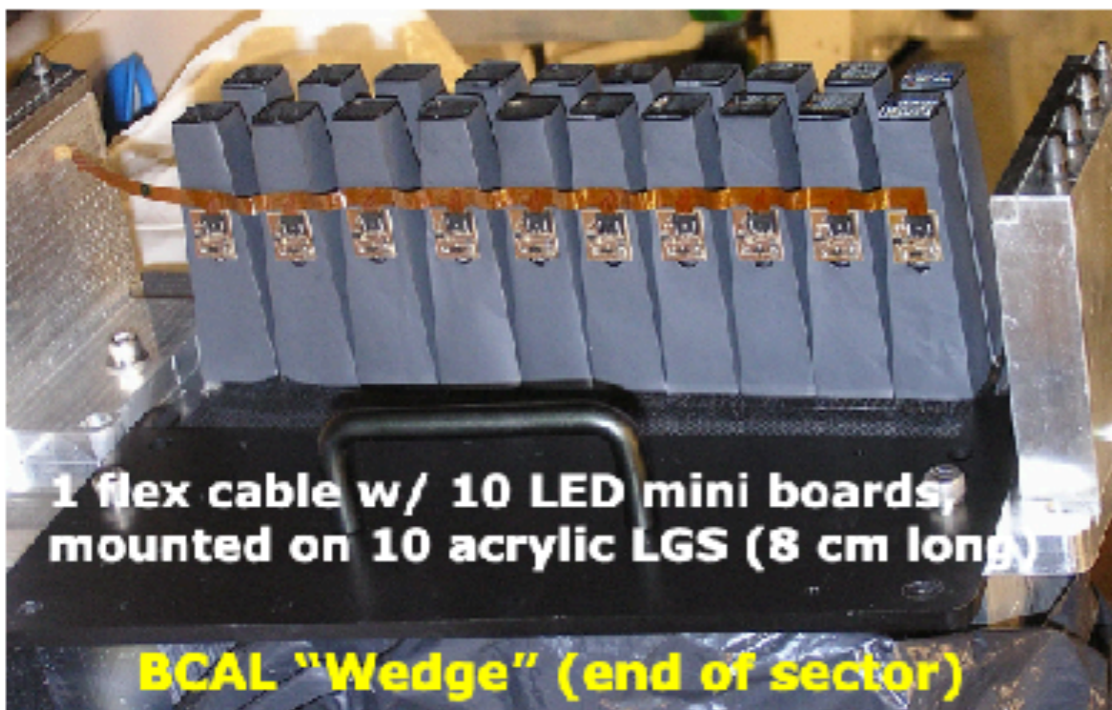
- rising time: 25 ns
- falling time: ~250 ns

LMS system



- glueX LMS system

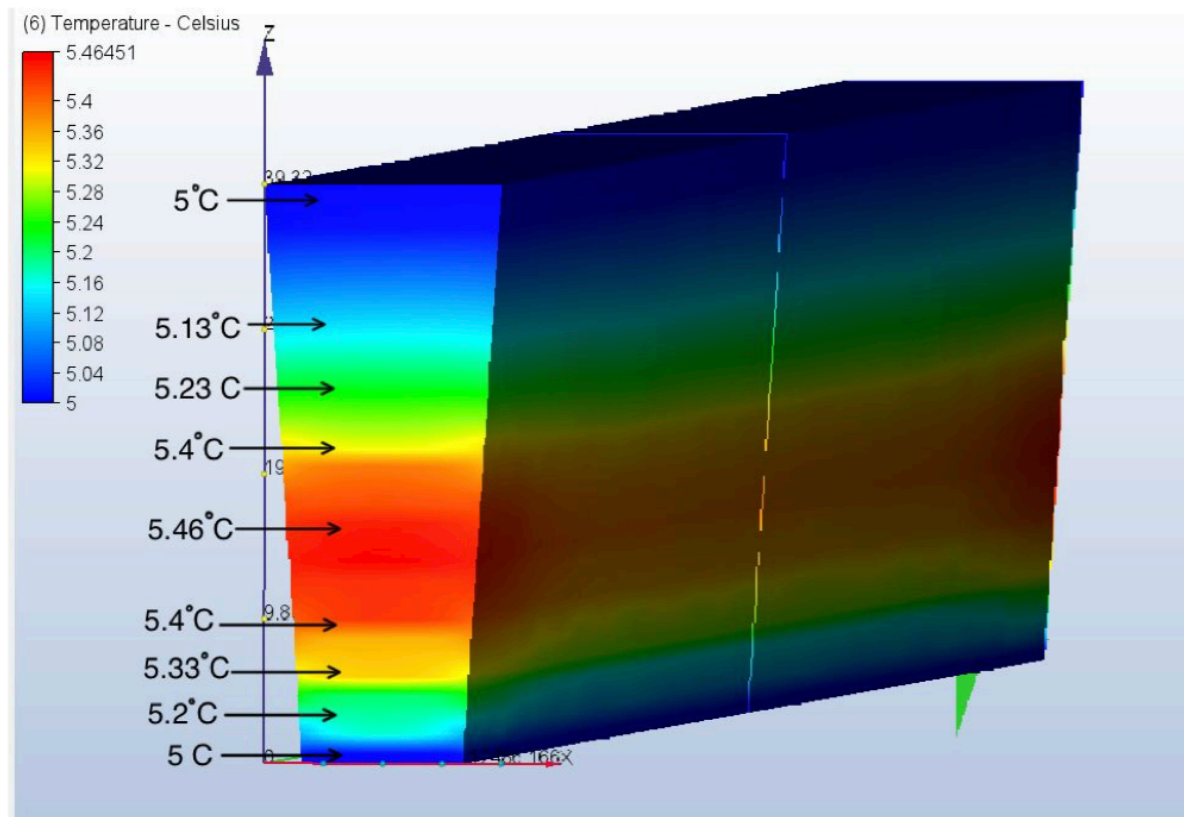
- 1-ch prototype board at KNU



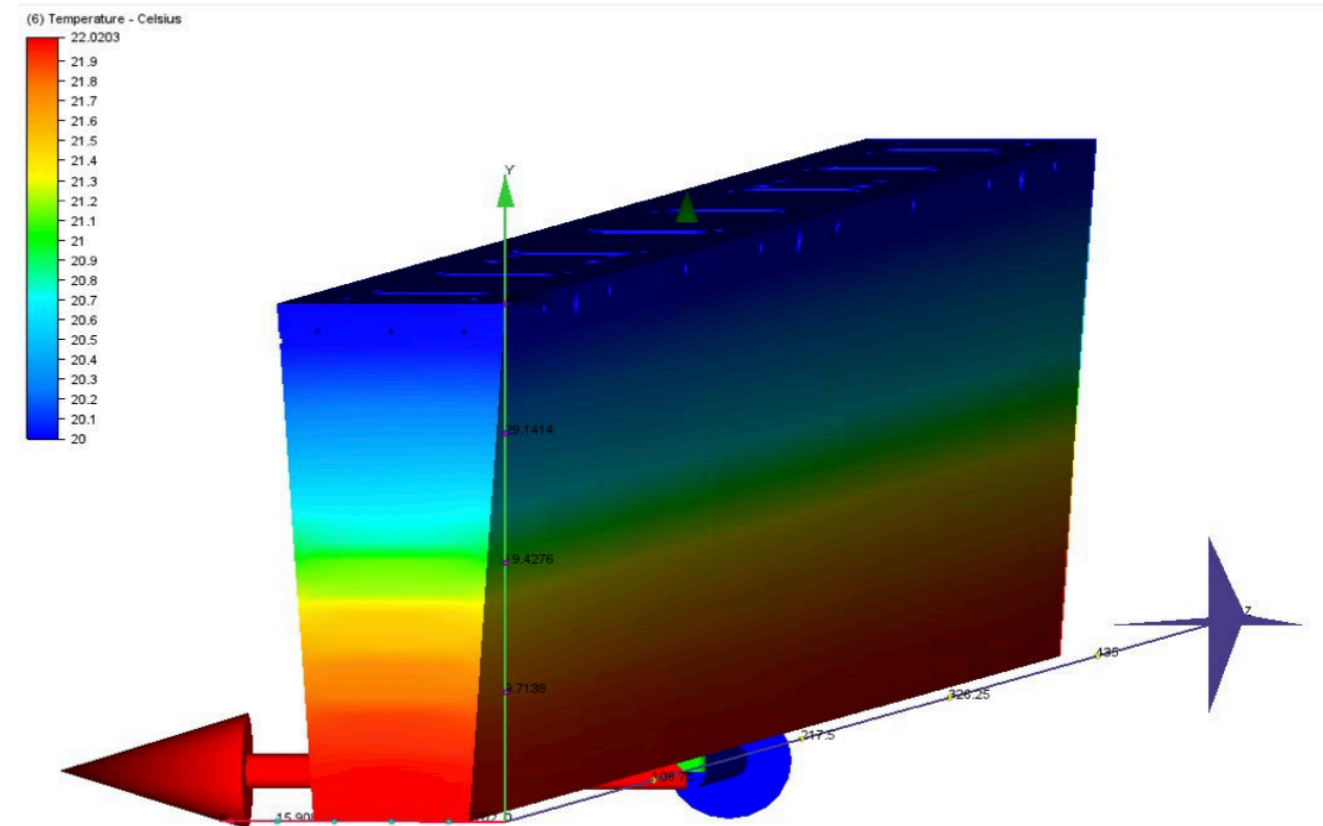
- Test on-going

BIC - Cooling Simulations (Manitoba)

Simulation Results (1 Sector)



Old simulation results

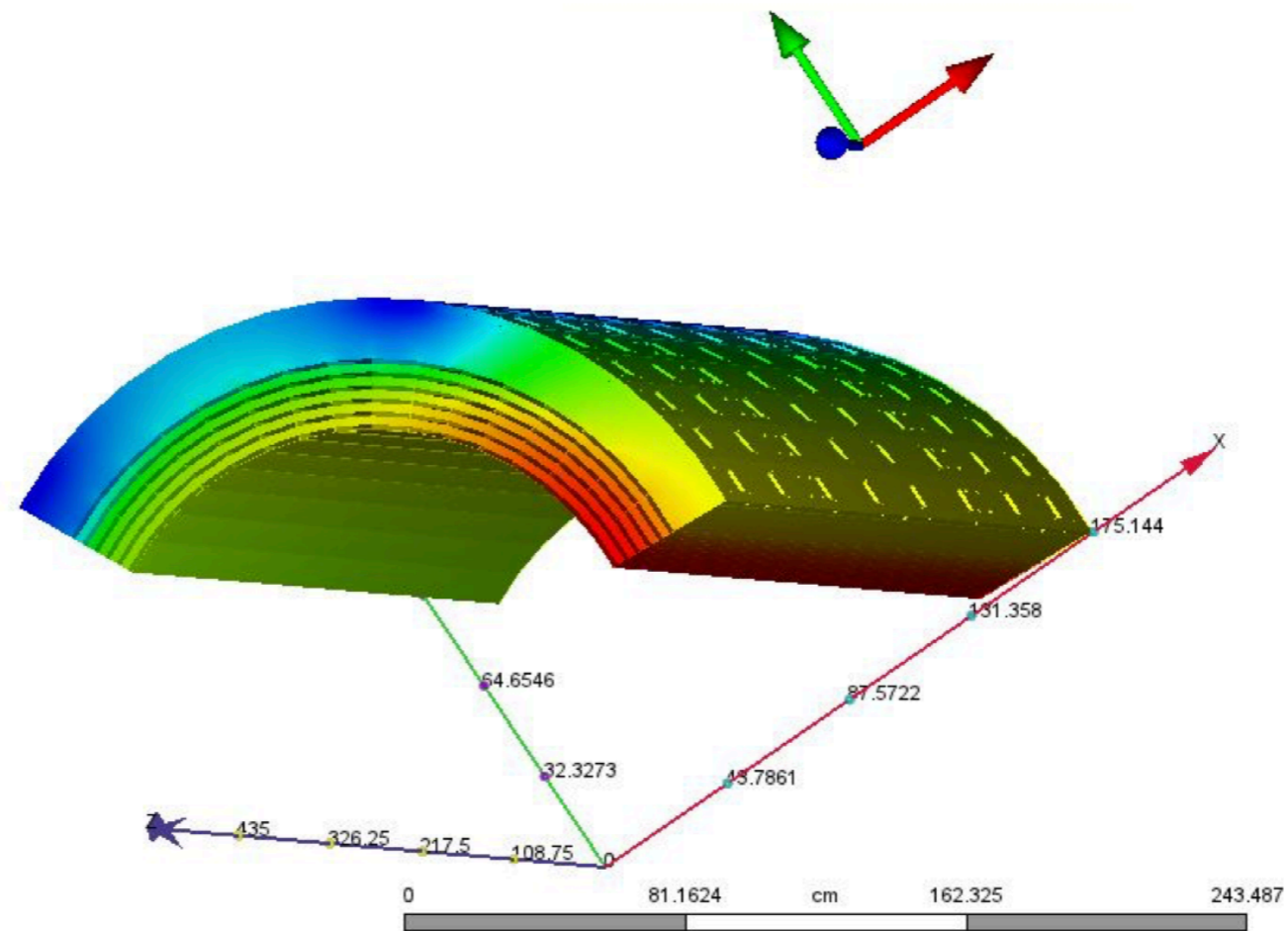
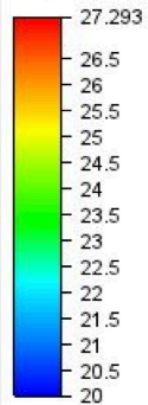


New simulation results

BIC - Cooling Simulations (Manitoba)

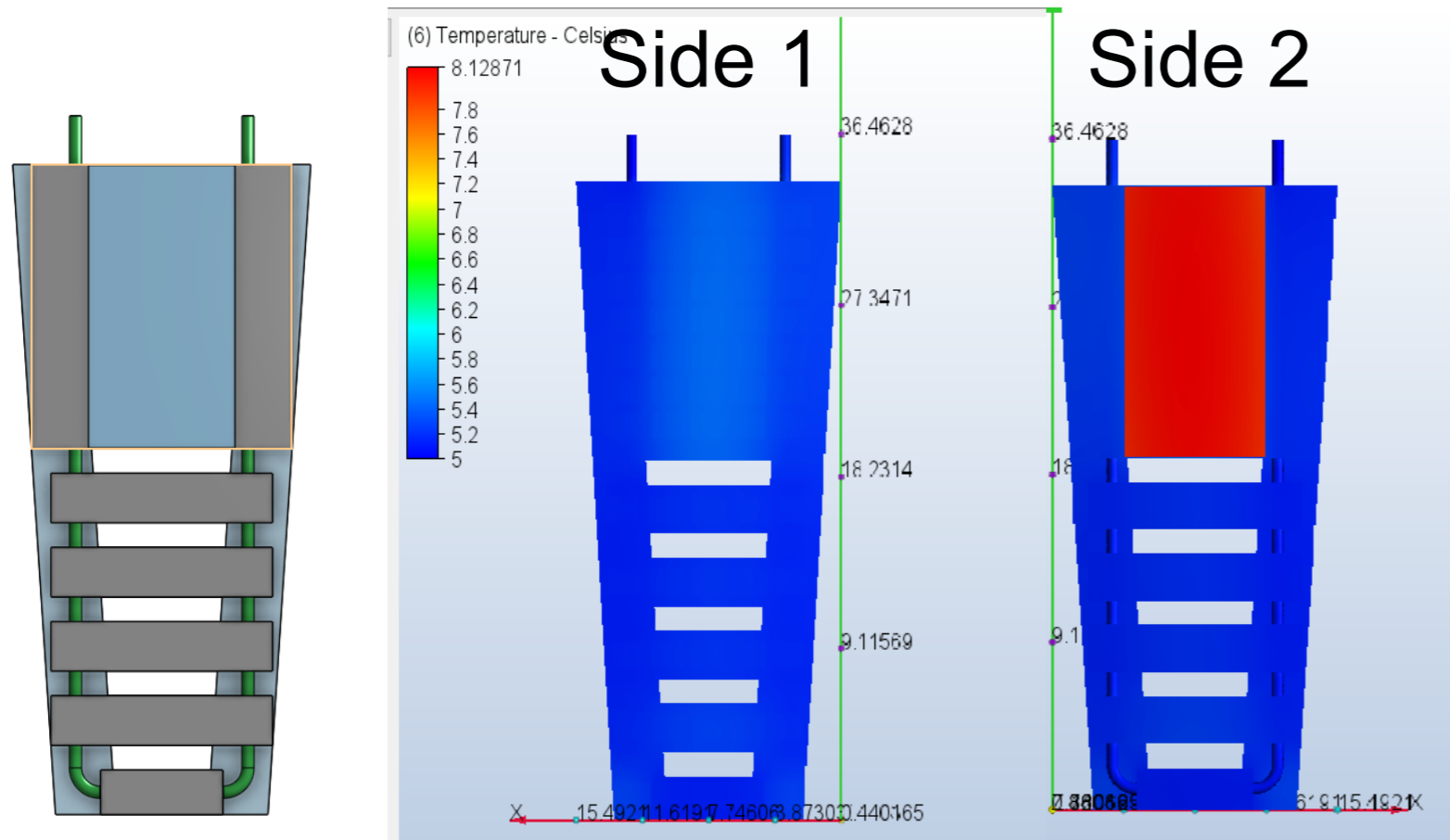
Simulation Results (16 Sector)

(6) Temperature - Celsius

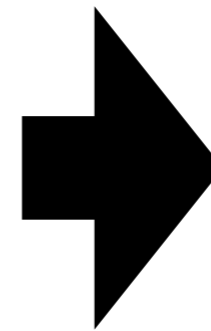


Cooling R&D

- Thermal simulation at Manitoba Univ.



- Prototype at KNU



Aluminum cold plate, PCBs on both sides:

- Side 1: ESB PCB with SiPMs
- Side 2: CALOROC and AstroPix ETC

Design dimensions:

- Cu cooling lines $\frac{1}{4}$ " OD
- Aluminum cold plate thickness $\frac{1}{2}$ "

Cooling R&D

Goal: Temp/Gain Stabilize SiPMs;
Use passive circuit (copy BCAL)

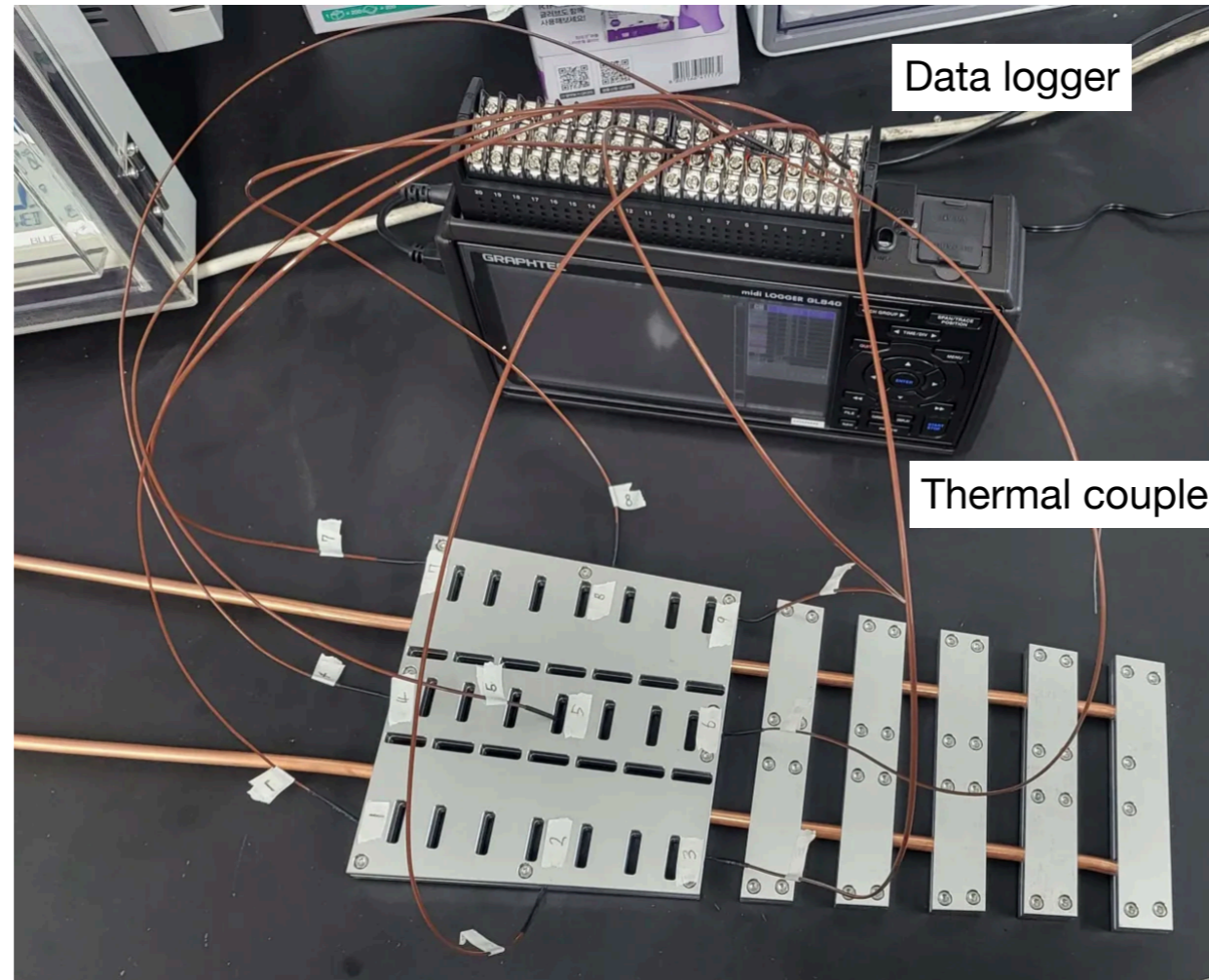
- Prototype at KNU

- Water cooling

- Temperature monitoring

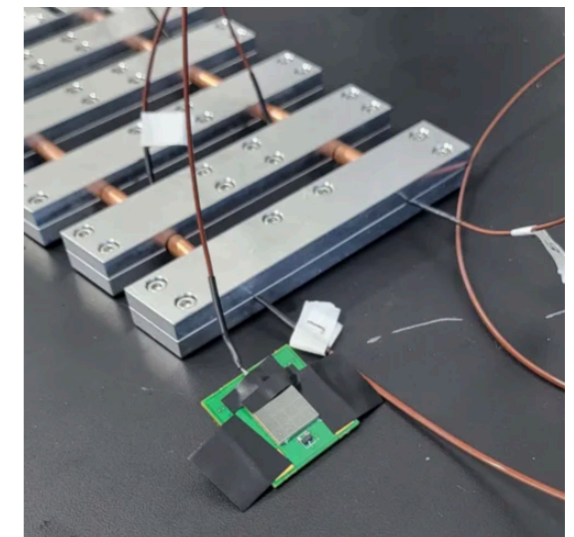


Chiller (7 °C , 1.1 L/min)



Data logger

Thermal couples



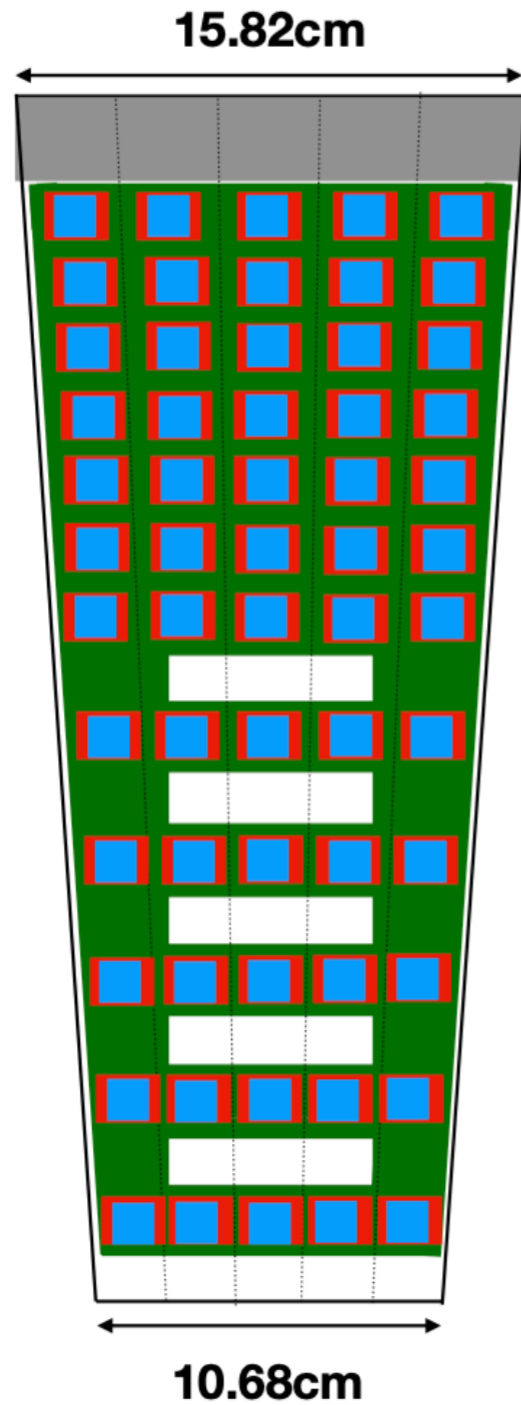
- Water temperature: -25 ~ 150 °C
- flow rate: 0.006 ~ 3400 mL/min

- Ongoing: development and construction of PCB (thermal) test articles for validation of CFD calculations
 - resistive element array distributed at locations of SiPMs

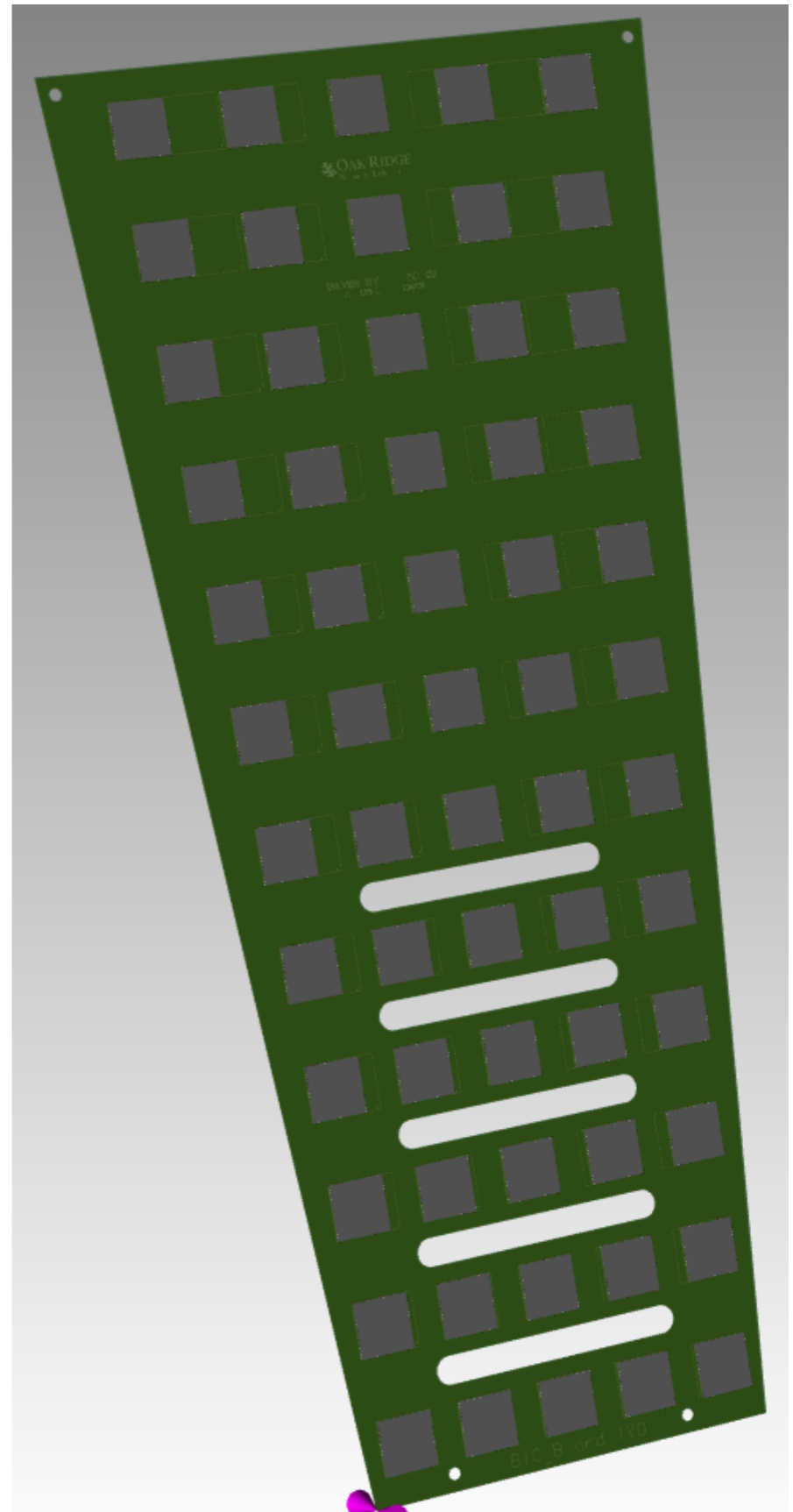
Summary & Looking Ahead

- Mechanical:
 - Baby BCAL - design advanced; **August 2026 (include cooling)**
 - BIC - design over the summer
 - LGs settled; need to make more
- Electronics:
 - HGCROC / readout: JLab beam test
 - Streams at Regina, ORNL, KNU: merge by June BIC workshop at ANL
 - Cooling design advanced

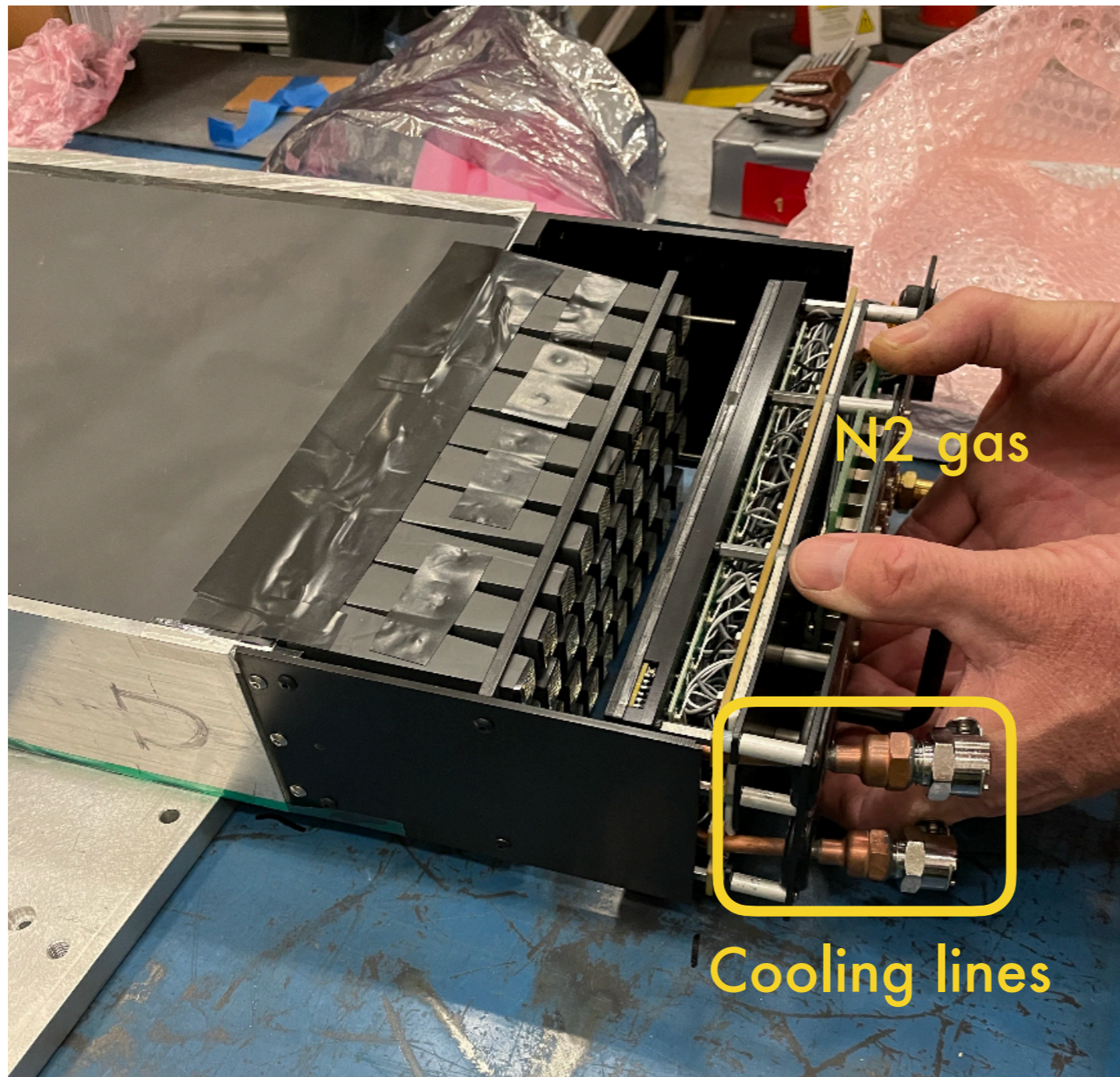
Backup slides



Testing at ORNL



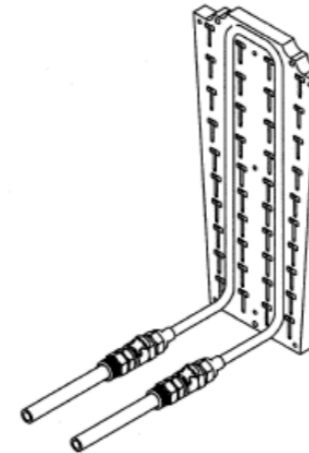
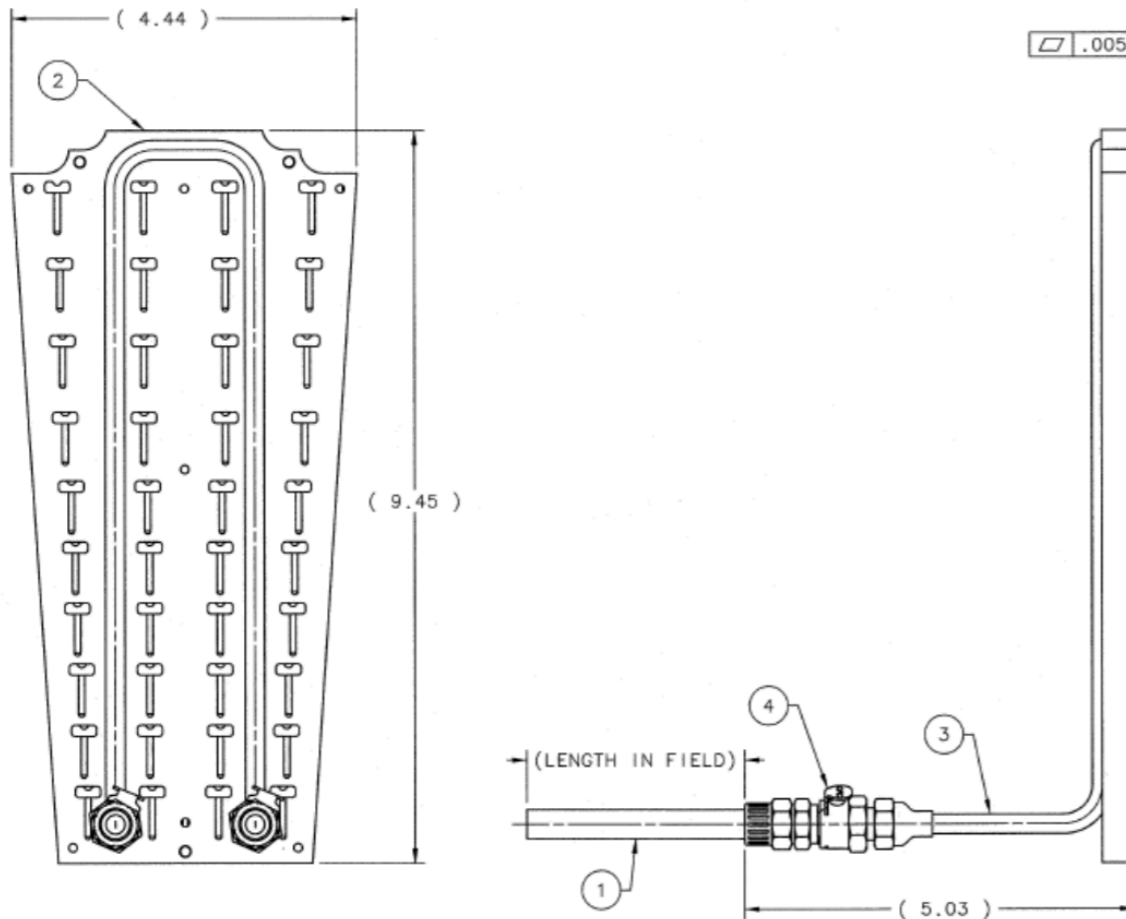
BCAL "Wedges"



- Contiguous LG stacking
- LG-SiPM air gap
- BIC: Si cookie
- Spring loading
- Integrated ESB for installation ease

Cooling Assembly

REVISION HISTORY				
ZONE	REV	DESCRIPTION	DATE	APPROVED



NOTES:

1. SUGGESTED SOURCES OR JLAB APPROVED ALTERNATE:
COLDER PRODUCTS COMPANY
1-800-444-2474
www.colder.com
2. SOLDER ITEM 2 TO ITEM 3 IN SUCH A WAY TO ENSURE GOOD THERMAL AND MECHANICAL CONTACT.
4. SOLDERING ITEMS 2 & 3 TOGETHER USING 50/50 TIN-LEAD SOLDER WITH GENERAL PURPOSE FLUX USING ANY STANDARD SOLDERING PROCESS.
5. PROCESS SHOULD ENSURE COMPONENT TEMPERATURES ARE MAINTAINED BELOW 800°F.
6. THOROUGHLY CLEAN ALL FLUXES WITH APPROPRIATE METHODS TO ENSURE REMAINING FLUX IS COMPLETELY REMOVED OR RENDERED NON-CORROSIVE
7. LENGTH OF ITEM 1 TO BE DECIDED IN FIELD TO ALLOW FOR APPROPRIATE LENGTH AND THEN INSTALLED AS SHOWN.

QTY	ITEM NO.	PART OR IDENTIFYING NO.	DESCRIPTION	MATERIAL SPECIFICATION	NOTES
2	4	COLDER PRODUCTS MCD1002	1/8 NPT VALVED COUPLING BODY	BRASS	1
1	3	D00000-01-07-2041	COOLING TUBE W/FITTINGS		
1	2	D00000-01-07-2040	COOLING PLATE		
2	1	D00000-01-07-1022	HOSE ASSY		

DOCUMENT CONTROL STAMP DCG	UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMAL ANGLES # N/A .X ± .1 .XXX ± .005	TRACKING NO. N/A		United States Department of Energy Jefferson Lab Thomas Jefferson National Accelerator Facility Newport News Virginia
		APPROVALS	DATE	
MATERIAL SEE PARTS LIST	THIRD ANGLE PROJECTION	DRAWN C. L. HUTTON	DATE 01/20/11	HALL D - GLUEX DETECTOR BARREL CALORIMETER COOLING PLATE ASSY
FINISH MACHINED SURFACES UNLESS OTHERWISE NOTED DEBURR & BREAK ALL SHARP EDGES	DO NOT SCALE DRAWING	CHECKED <i>[Signature]</i>	DATE 2/20/11	SIZE DWG. NO. D D00000-01-07-1021
SCALE 1:1			SHEET 1 OF 1	