L0 design and prototype testing plan

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Homework for L0 design

1. How can we improve the rotation angle of a ladder with the lower sensor edge at r=6cm, not the censor center?

2. Occupancy calculation for new L0 designs with central Au+Au events

Summary of simulated sensors

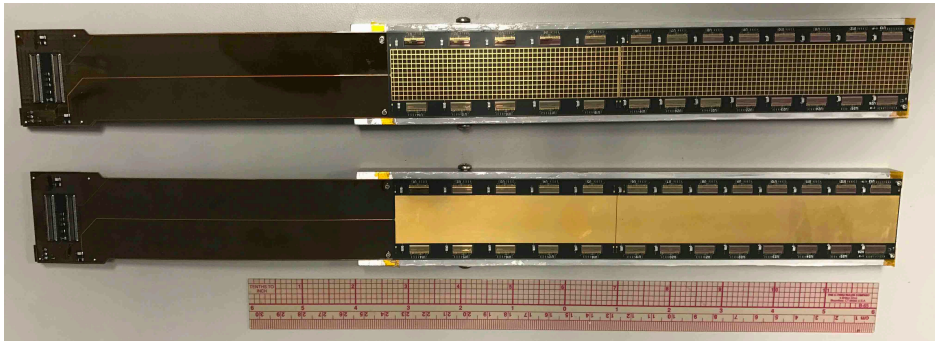
sensor length	@r=6cm	rotation angle (deg)	overlap	acceptance	occupancy	ladders	gap btwn ladders
10mmx2	center	14	5%	0.965	5.2%	20	0.5mm
10mm	center	19.5	22%	0.967	5.8%	48	1mm
	lower edge	16					
9mm	center	19	13%	0.966	5.4%		
	lower edge	15.5					
8.5mm	center	18.5	8%	0.965	5.1%		
	lower edge	15					
8mm	center	18	2.5%	0.947	-		
	lower edge	14.5					

Definition: Occupancy = # of fired L0 channels / total L0 channels

- Total L0 channels = 128channels x 20chips x ladders
- Input event: Hijing 0-4fm(=0-10% centrality) Au+Au collision
  - ✓ Total 20k events, |zvtx|<5cm
  - ✓ Hits by secondary particles are taken into account.
  - ✓ INTT threshold = 25% of MIP energy deposit with 200μm-Si

Prototype production & tests

1. Assembly of HDI on Al stave
   - ✓ 1st test: confirmation of no leak current by connection of HDI and stave
2. Assembly & wire-bonding of FPHX chips on HDI
   - ✓ 2nd test: check of FPHX chip status with calibration pulse
3. Assembly of Si sensor on HDI (not yet wire-bonding to chips)
   - ✓ 3rd test: same with 2nd test
   - ← **We are here**
4. Wire-bonding of Si sensor to FPHX chips
   - ✓ 4th test: check noise level with biased sensor
   - ✓ 5th test: cosmic ray measurement
     - Monitoring temperature of chips during the test



Module2: Mesh ground

Module1: Solid ground

Prototype production status

Module ID	GND type	Current status	Bad chips	Note
1	solid	passed 3rd test	Chip17: noisy Chip20: bad wires Chip21: bad wires	latter sensor was broken after mounted on HDI, then replaced with new sensor. Will redo wire-bonding of bad chips.
2	mesh	passed 3rd test	Chip13: bad wires	Good so far. Will redo Chip13 wire-bonding.
3	solid	assembly of sensor & chips on HDI	No check yet	Spare module.

Module 2 FPHX chip status at 3rd test