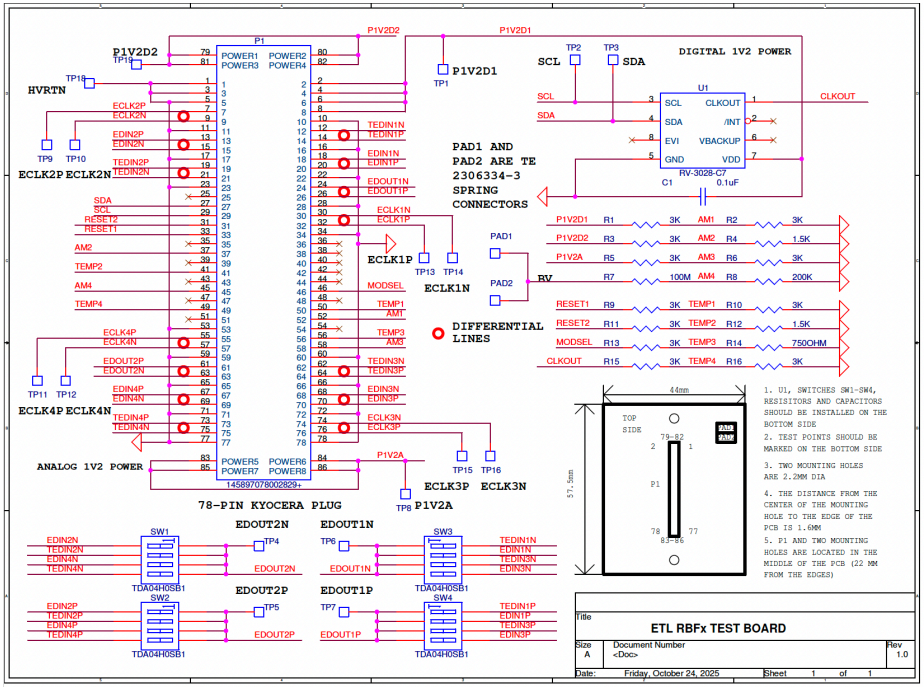
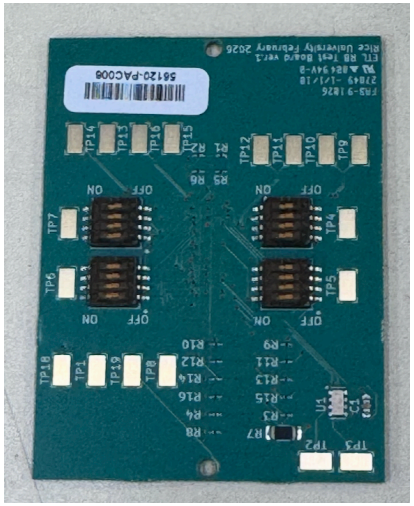
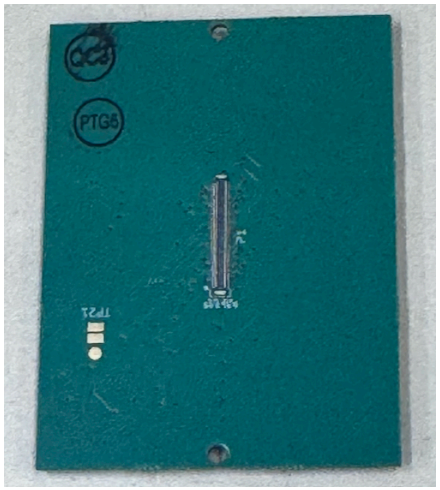
FTOF RDO Testing at Rice

June 3, 2026

Rice Test Board







- Goal: running “loopback” test to verify the signal connections between RDO and module board without using real module board
  - ➡ Analog signals like P1V2D1/P1V2D2/P1V2A etc. are read out via MUX64 by repurposing VREFs/VTEMPs, and are compared to expected values during test
  - ➡ I2C communication verified via a Real-Time chip (RTC)
  - ➡ Loopback ePortTx to ePortRx for PRBs test
  - ➡ CLk40 probed by oscilloscope

Analog Signal Loopback

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Testing Rice Test Board in slot 2
ADC value for ETROC2_VREF1 from MUX64 is inconsistent with that from NOADC
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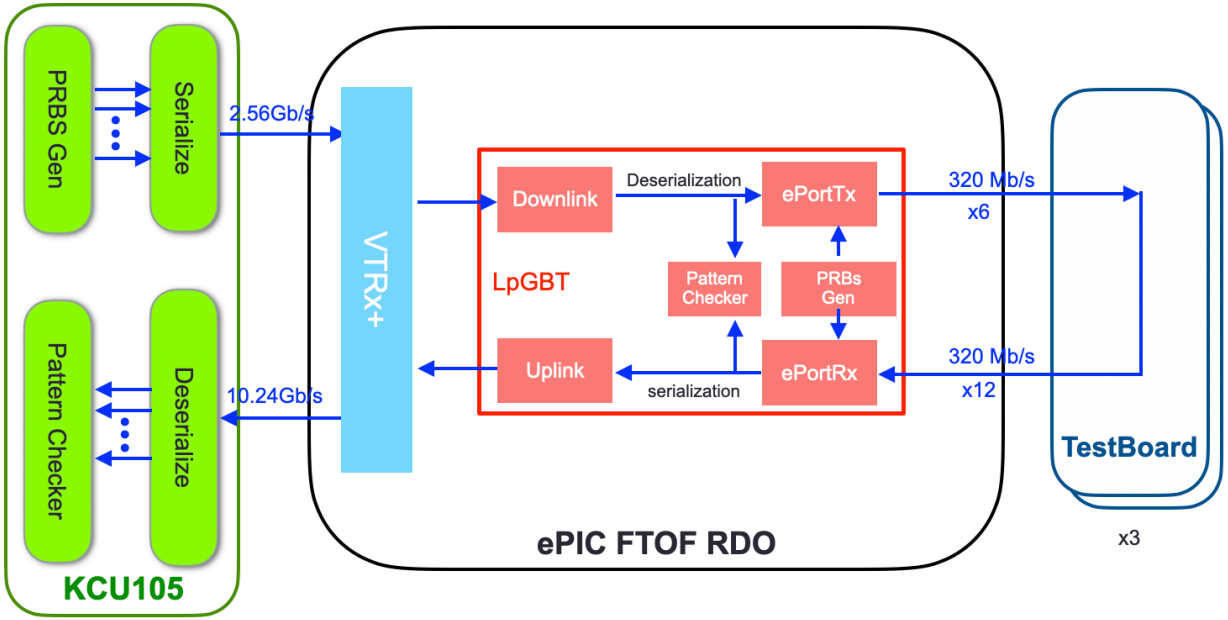
TestBoard2	ModuleBoardName	Expected Value	Testboard Direct	Testboard Value	Pass	comment
P1V2A	ETROC2_VREF1	1.25	0.00112568	0.000345405	False	N/A,bPOL2
BV	ETROC2_VREF2	0.0921763	8.32302e-05	6.75631	True	HVMON
P1V2D1	ETROC2_VREF3	1.25	0.190851	1.17373	True	N/A,bPOL3
P1V2D2	ETROC2_VREF4	1.25	0.278417	1.15547	True	N/A,bPOL3
MODSEL	ETROC2_VTEMP1	1.22086	0.115795	1.17532	True	MODULE_SELECT1
RESET1	ETROC2_VTEMP3	1.22086	0.274247	1.13808	True	RESET1
RESET2	ETROC2_VTEMP4	1.22086	0.188776	1.16732	True	RESET2

```
Some ADC values are inconsistent between MUX64 and TESTBOARD LOOPBACK!
RTC read/write via I2C test passed!
LPGBT RX eLink locked on slot 2: DAQ_eRX6:1, DAQ_eRX16:1, DAQ_eRX4:1, DAQ_eRX18:1,
```

- Analog signals like P1V2D1/P1V2D2/P1V2A/MODSEL etc. are read out via MUX64 by repurposing VREFs/VTEMPs designed for front-end EICROC
  - ➡ Expected values for P1V2D1/P1V2D2/P1V2A: ~1.2V
  - ➡ Expected values for signals originating from lpGBT GPIOs, MODSEL and RESET1/2, are also ~1.2V, close to the lpGBT power supply
- Successfully verified most analog signals to module board

PRBS Test: KCU+RB+TestBoards



- Full path PRBS test: KCU PRBS generator → DAQ lpGBT downlink → DAQ lpGBT ePortTx → test boards → DAQ+TRIG lpGBT ePortRx → DAQ+TRIG lpGBT uplinks → KCU pattern checker for each elink
  - Verified VTRx+, downlink, DAQ lpGBT eTX and eRX, TRIG lpGBT eRX, uplinks
- Alternative PRBS tests with lpGBT built-in test features: useful for debugging
  - Downlink test: KCU PRBS generator → DAQ lpGBT downlink → DAQ lpGBT ePortTx → DAQ lpGBT pattern checker
  - E-link test: DAQ lpGBT PRBS generator → DAQ lpGBT ePortTx → test board → DAQ+TRIG lpGBT ePortRx → DAQ+TRIG lpGBT pattern checker
  - Uplink test: DAQ+TRIG lpGBT PRBS generator → DAQ+TRIG lpGBT ePortRx → DAQ+TRIG lpGBT uplinks → KCU pattern checker
  - Basically any combination of PRBS Generation and Pattern checker is possible
- All above PRBS test methods have been verified
- Routine test with RBF prototype: >=3 hours run with full path PRBS test and short runs with other three PRBS tests

Right now test board is only installed in the middle slot of RDO

PRBS Test using lpGBT Built-in Feature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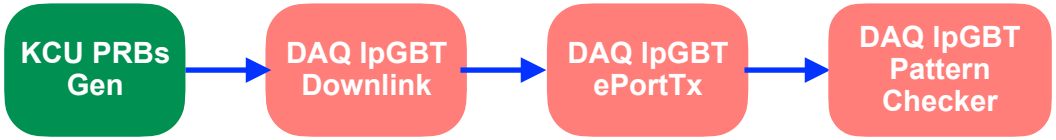
Running PRBS test with lpGBT built-in checker for 10 seconds, with DAQ rx links [6, 16, 4, 18] and Trigger rx links []...
LPGBT RX eLink locked on slot 2: DAQ_eRX6:1, DAQ_eRX16:1, DAQ_eRX4:1, DAQ_eRX18:1,
DAQ  eRX 6 ( <= EDOUT22/eTX10 ): BERT pass (errors=0, PRBS flag=0), eRX lock=1
DAQ  eRX16 ( <= EDOUT22/eTX10 ): BERT pass (errors=0, PRBS flag=0), eRX lock=1
DAQ  eRX 4 ( <= EDOUT02/eTX 2 ): BERT pass (errors=0, PRBS flag=0), eRX lock=1
DAQ  eRX18 ( <= EDOUT02/eTX 2 ): BERT pass (errors=0, PRBS flag=0), eRX lock=1

PRBS test results after 13.00 seconds :
```

Module	DAQ eRX	PRBS Errors	BER	Link Status
2	eTX10->eRX 6	0	0	GOOD
2	eTX10->eRX16	0	0	GOOD
2	eTX 2->eRX 4	0	0	GOOD
2	eTX 2->eRX18	0	0	GOOD

- lpGBT has built-in PRBS Generator and Checker
- PRBS test using lpGBT built-in features to verify the elinks

Downlink PRBS Test



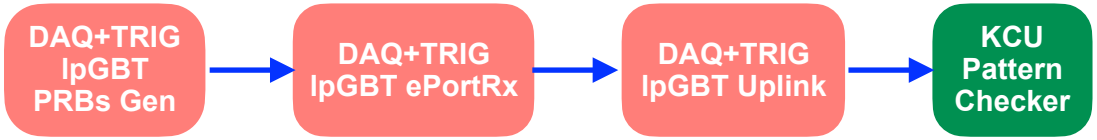
Downlink PRBS test results after 13.00 seconds:

DAQ eTX	PRBS Errors	BER	BERT Flag	Status
eTX 0	0	0	0	GOOD
eTX 4	0	0	0	GOOD
eTX 8	0	0	0	GOOD
eTX12	0	0	0	GOOD

Summary during 13.00 seconds test time: 4 PASS, 0 FAIL

- PRBS is generated in KCU and received+checked in lpGBT via downlink
  - No test board is needed in this downlink PRBS test
  - All 4 TX groups can be tested
    - Usually the mirror function is enabled during nominal operation: channels in each egroup is sending the same data as the first channel
- This PRBS test verified the downlink path from KCU to lpGBT ePortTx

Uplink PRBS Test

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Running PRBS test on uplinks with KCU pattern checker for 0.017 hours with all  DAQ rx links
Checking uplink 0 status
Uplink ready: 1
FEC count: 0

PRBS test results after 60.24 seconds :
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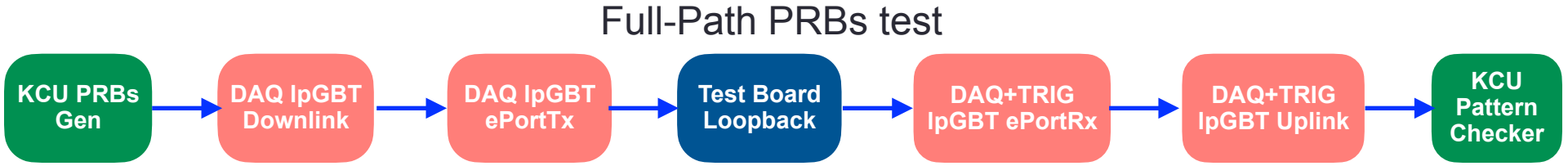
EPGroup	DAQ eRX	PRBS Errors	BER	Link Status
0	0	0	0	GOOD
0	1	0	0	GOOD
0	2	0	0	GOOD
0	3	0	0	GOOD
1	4	0	0	GOOD
1	5	0	0	GOOD
1	6	0	0	GOOD
1	7	0	0	GOOD
2	8	0	0	GOOD
2	9	0	0	GOOD
2	10	0	0	GOOD
2	11	0	0	GOOD
3	12	0	0	GOOD
3	13	0	0	GOOD
3	14	0	0	GOOD
3	15	0	0	GOOD
4	16	0	0	GOOD
4	17	0	0	GOOD
4	18	0	0	GOOD
4	19	0	0	GOOD
5	20	0	0	GOOD
5	21	0	0	GOOD
5	22	0	0	GOOD
5	23	0	0	GOOD
6	24	0	0	GOOD
6	25	0	0	GOOD
6	26	0	0	GOOD
6	27	0	0	GOOD

- PRBS is generated in lpGBT and received+checked in KCU
- This PRBS test verified the uplink path from lpGBT ePortRx to KCU
  - ➡ All 28 Rx from 7 egroups
- NO test board is needed in this

Full-Path PRBS Test



PRBS test results after 601.30 seconds :

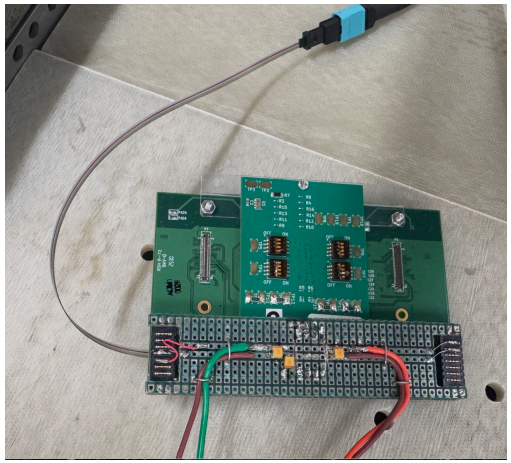
Module	DAQ eRX	PRBS Errors	BER	Link Status
2	eTX10->eRX 6	0	0	GOOD
2	eTX10->eRX16	0	0	GOOD
2	eTX 2->eRX 4	0	0	GOOD
2	eTX 2->eRX18	0	0	GOOD

Summary during 601.30 seconds test time: 4 GOOD, 0 WARNING, 0 ERROR

- The full-path PRBS test verified the reliability of all high speed links in RDO: downlink from KCU to lpGBT, elinks between lpGBT and EICROC, uplink from lpGBT to KCU

RBF6v1 + TestBoards: Summary

Module board signals	#	Testing with TestBoard	Tested	Description
I2C	1	Read/Write Real-Time Chip	✅	I2C communication with ETROCs
P1V2D1	1	Read via MUX64	✅	1.2 V digital power 1
P1V2D2	1	Read via MUX64	✅	1.2 V digital power 2
P1V2A	1	Read via MUX64	—	1.2 V analog power
BV	1	Read via MUX64	—	BV
RESET1	1	Read via MUX64	✅	RESET1 for ETROC, controlled by lpGBT GPIO
RESET2	1	Read via MUX64	✅	RESET2 for ETROC, controlled by lpGBT GPIO
Module_Select	1	Read via MUX64	✅	ETROC I2C address bit, controlled by lpGBT GPIO
EDOUT	2	Loopback with PRBS	✅	E-links (eTX) from LPGBT for fast control, 320 Mb/s
EDIN	4	Loopback with PRBS	✅	E-links (eRX) from LPGBT, 320 Mb/s
ECLK	4	Oscilloscope	—	CLOCKs (ECLK) from LPGBT, 40 MHz



Connections between RDO and module board have been tested via test boards

Summary

- We used the custom test board to verify the interface between RDO and EICROC
  - Readout the analog signals via MUX64+lpGBT ADC by repurposing the VREFs/VTEMPs
  - PRBS test with elink loopback: lpGBT eTx to test board to lpGBT eRx
    - PRBS generated/Checked by KCU or lpGBT built-in function
  - Right now we can only install test board in the middle slot due to physical size limit

Backup

RDOv1 ADCs

RDO ADC+MUX64 readouts with power board:

Reading DAQ lpGBT ADC values:

Register	Pin	Reading (raw)	Reading (calib)	Voltage (direct)	Voltage (conv)	Status	Comment
TH1	0	112	82.693	0.081	0.081	OK	VTRX TH1
MUX64OUT	1	35	0.567	0.001	0.001	OK	MUX64OUT / 2, ADC2 raw
LVRB	2	661	668.295	0.653	13.457	OK	LVRB / 20.6
2V5TX_ADC	3	820	837.897	0.819	2.457	OK	2V5TX / 3
RSSI_ADC	4	586	588.300	0.575	1.150	OK	RSSI current = 0.242 mA
1V2RA	5	570	571.229	0.558	0.558	OK	1V2RA(ADC5), RT1
2V5RX_ADC	6	818	835.763	0.817	2.451	OK	2V5RX / 3
RT2_ADC	7	434	426.163	0.417	0.417	OK	RT2
VDAC	8	993	1022.428	0.999	0.999	OK	VDAC output (internal)
VSSA	9	35	0.567	0.001	0.001	OK	VSSA, Analog ground (internal)
VDDTX	10	526	524.296	0.513	1.220	OK	VDDTX * 0.42, TX supply (internal)
VDDRX	11	527	525.367	0.514	1.222	OK	VDDRX * 0.42, RX supply (internal)
VDD	12	527	525.362	0.514	1.222	OK	VDD * 0.42, Digital supply (internal)
VDDA	13	528	526.424	0.515	1.225	OK	VDDA * 0.42, Analog supply (internal)
TEMP	14	546	545.634	0.533	0.533	OK	Temp = 35.3 C (internal signal)
VREF	15	514	511.501	0.500	1.000	OK	ADC VREF/2 (internal)

Reading MUX64 values:

Channel	Pin	Reading (raw)	Reading (calib)	Voltage (direct)	Voltage (conv)	Comment
HVMON	31	36	1.633	0.002	1.616	HVMON
ADC2	0	335	320.570	0.313	13.229	LVRB
ADC5	1	251	230.959	0.226	0.452	Thermistor
PTAT2	32	90	59.233	0.058	0.706	PTAT2
PTAT1	33	83	51.766	0.051	0.617	PTAT1
GROUND	63	36	1.633	0.002	0.003	Background

Temperature on RB RT1 is: 33.1 C
Temperature on RB RT2 is: 28.4 C
Temperature on RB VTRX is: 30.5 C
Temprature on DAQ lpGBT is 34.9 C
This RB status: All good! Downlink Ready, Uplinks Ready, No FEC errors.