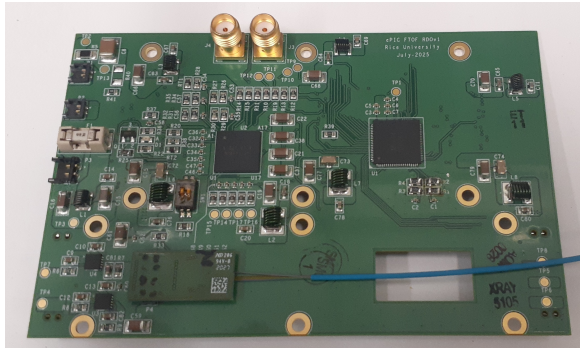
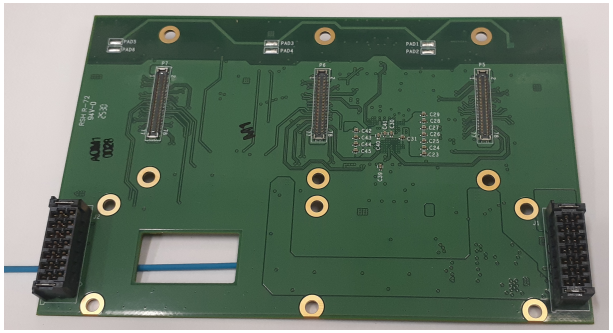
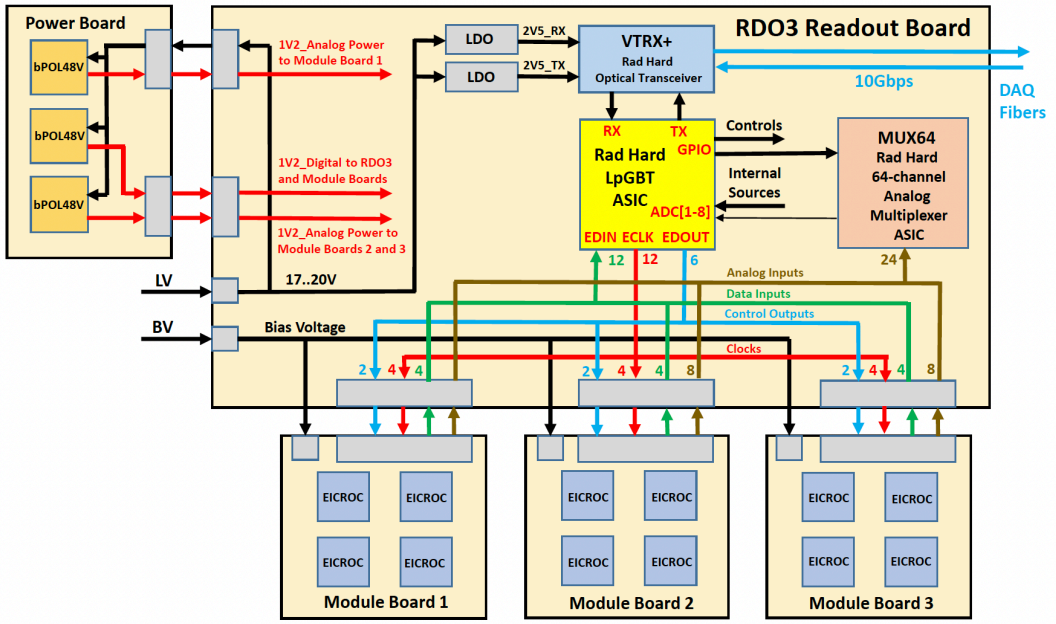
FTOF RDO Testing at Rice

June 12, 2026

RDOv1: FTOF Readout Board

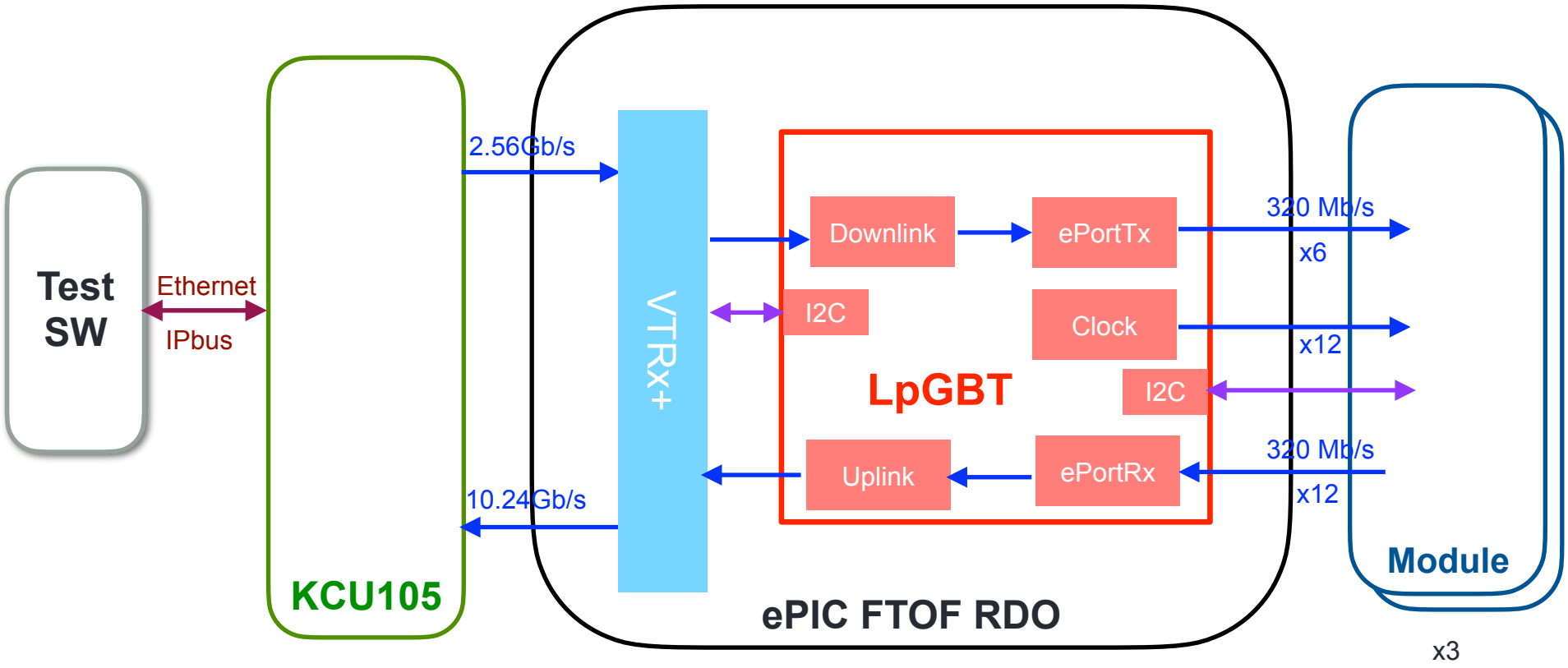






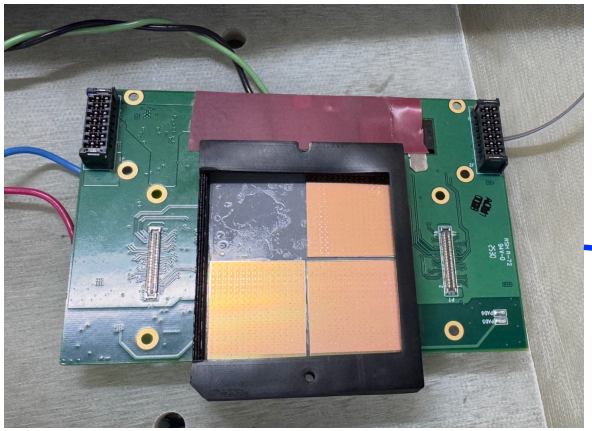
- RDOv1: Readout board v1 that supports three module boards, twiki page
  - VTRx+: optical transceiver, RX @ 2.56 Gb/s and TX @ 10.24 Gb/s
  - lpGBT v1: control and data transmission
    - Fast control: 320 Mb/s to modules, two elinks per module board
    - Data readout: 320 Mb/s from modules, four elinks per module board
    - Clocks: 40 MHz to modules, four per module boards
    - I2C communication to VTRX+ and modules
    - ADCs for analog monitoring and GPIOs for slow control
  - MUX64: extension of analog monitoring channels
- Power-supply: LV is 17-20 V, and three bPOL48 DC-DC converters on Power Board to provide 1.2V for lpGBT + modules
  - Without Power Board, 10-12V and 1.2V are directly provided

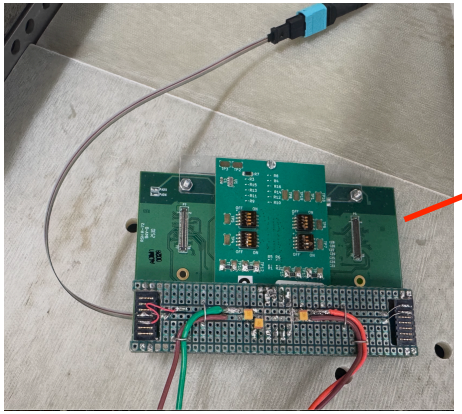
ePIC RDO Test with KCU

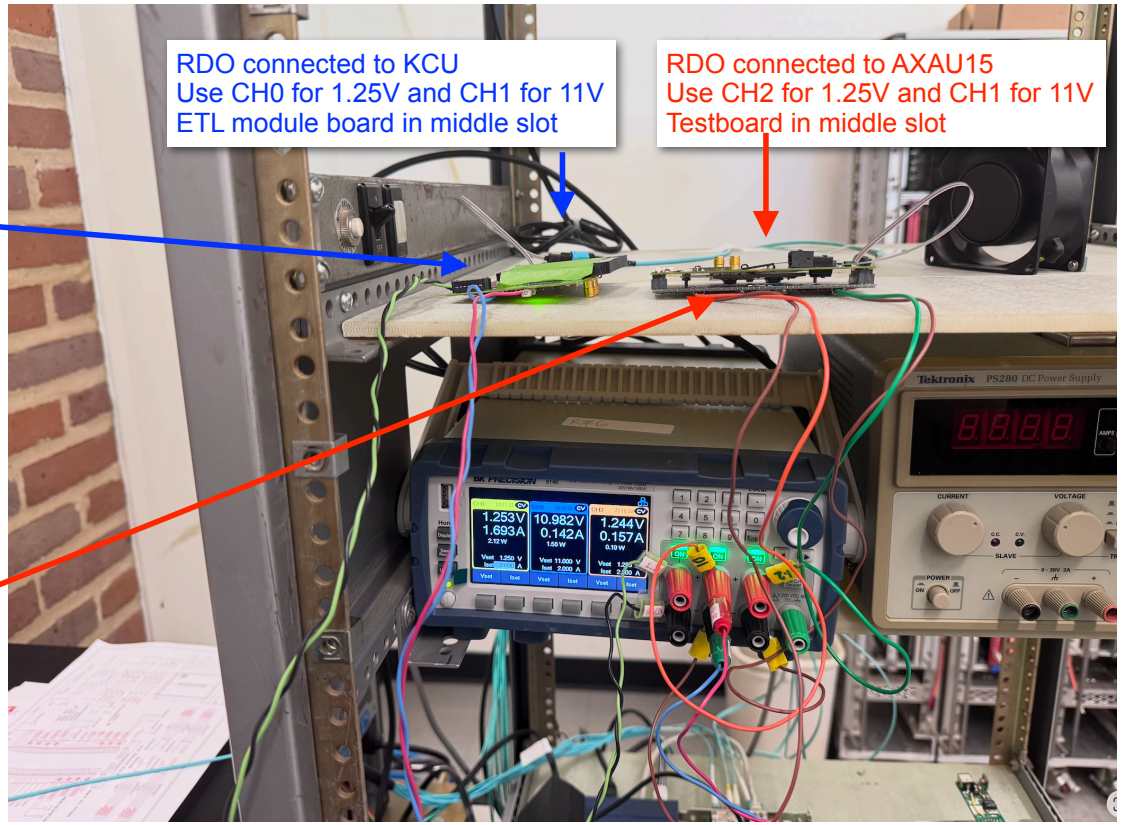


- The test stand uses the KCU105 to send+receive data from RDO
- Without using modules, we designed one custom test board for loopback test to verify the interface between RDO and module: both analog signals and elinks

RDO+CMS ETL ETROCs







- Installed CMS ETL module board with three bare ETROCs in the middle slot of RDO
  - ETROC is like EICROC in ePIC TFOF
- Two test stands at Rice:
  - KCU + RDO + ETL CMS module board
  - AXAU15 + RDO + test board: loopback test reported last time
  - At this moment, no Power Board is used in these two setups and 11V+1.2V are directly provided

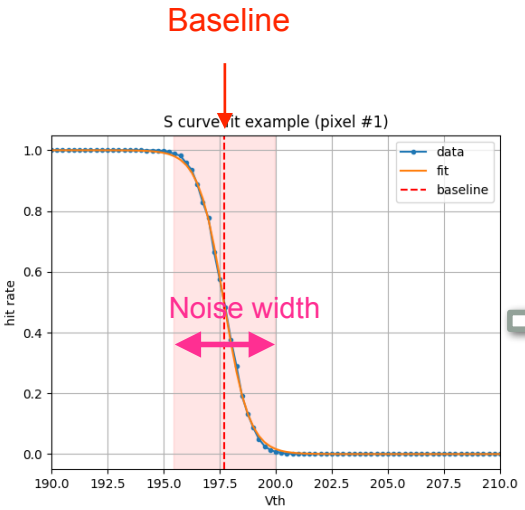
MUX64: ETROC in middle location

Reading MUX64 values:

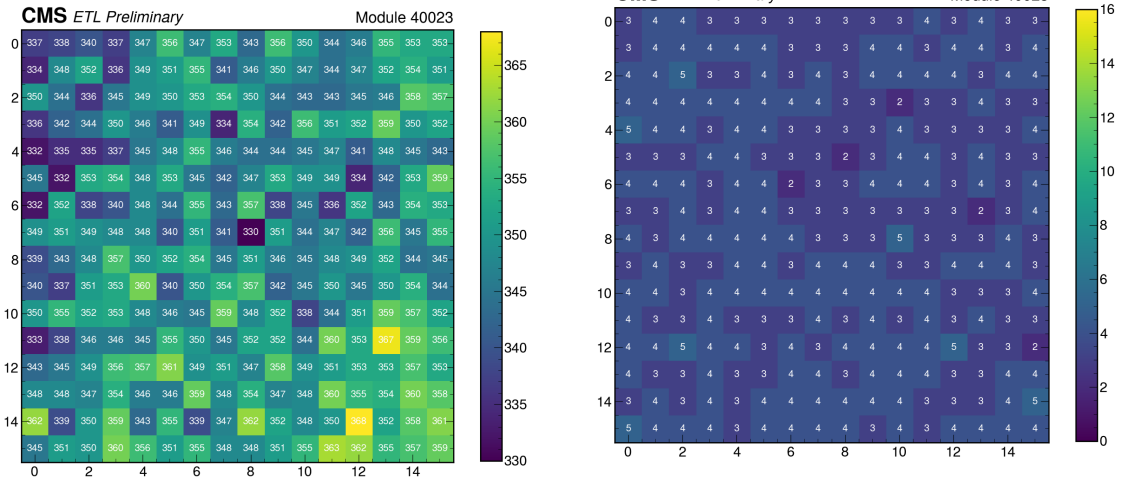
Channel	Pin	Reading (raw)	Reading (calib)	Voltage (direct)	Voltage (conv)	Comment
HVMON	31	33	3.000	0.003	2.953	HVMON
ADC2	0	273	258.426	0.253	10.538	LVRB
ADC5	1	216	197.762	0.193	0.387	Thermistor
PTAT2	32	33	3.000	0.003	0.024	PTAT2
PTAT1	33	32	1.937	0.002	0.015	PTAT1
GROUND	63	32	1.936	0.002	0.004	Background
ETROC1_VREF3	2	33	3.000	0.003	0.007	VREF3 on module 1
ETROC1_VREF2	3	32	1.936	0.002	0.004	VREF2 on module 1
ETROC1_VREF4	4	32	1.936	0.002	0.004	VREF4 on module 1
ETROC1_VREF1	5	33	2.999	0.003	0.007	VREF1 on module 1
ETROC2_VREF1	6	32	1.934	0.002	0.004	VREF3 on module 2
ETROC2_VREF2	7	424	419.126	0.410	0.934	VREF2 on module 2
ETROC2_VREF4	8	417	411.681	0.402	0.918	VREF4 on module 2
ETROC2_VREF3	9	418	412.745	0.403	0.920	VREF1 on module 2
ETROC3_VREF3	10	33	3.000	0.003	0.007	VREF3 on module 3
ETROC3_VREF2	11	33	3.000	0.003	0.007	VREF2 on module 3
ETROC3_VREF4	12	32	1.936	0.002	0.004	VREF4 on module 3
ETROC3_VREF1	13	32	1.936	0.002	0.004	VREF1 on module 3
ETROC1_VTEMP2	14	32	1.936	0.002	0.004	VTEMP2 in module 1
ETROC2_VTEMP2	15	310	297.804	0.291	0.582	VTEMP2 in module 2
ETROC3_VTEMP2	16	32	1.936	0.002	0.004	VTEMP2 in module 3
ETROC2_VTEMP4	60	318	306.314	0.299	0.599	VTEMP4 in module 2
ETROC2_VTEMP1	59	33	3.000	0.003	0.006	VTEMP1 in module 2
ETROC2_VTEMP3	58	294	280.775	0.274	0.549	VTEMP3 in module 2
ETROC1_VTEMP4	57	32	1.934	0.002	0.004	VTEMP4 in module 1
ETROC1_VTEMP1	56	32	1.933	0.002	0.004	VTEMP1 in module 1
ETROC1_VTEMP3	55	32	1.936	0.002	0.004	VTEMP3 in module 1
ETROC3_VTEMP3	36	32	1.934	0.002	0.004	VTEMP3 in module 3
ETROC3_VTEMP1	35	33	3.000	0.003	0.006	VTEMP1 in module 3
ETROC3_VTEMP4	34	32	1.936	0.002	0.004	VTEMP4 in module 3

- MUX64 monitors VREF and VTEMP for each ETROC
  - ➡ VREF is used to define threshold and is critical for performance, typically 1V
    - Can be provided externally or generated internally
  - ➡ VTEMP is proportional to chip temperature

CMS ETL ETROC: Threshold Scan and Noise Width



S-curve for each pixel



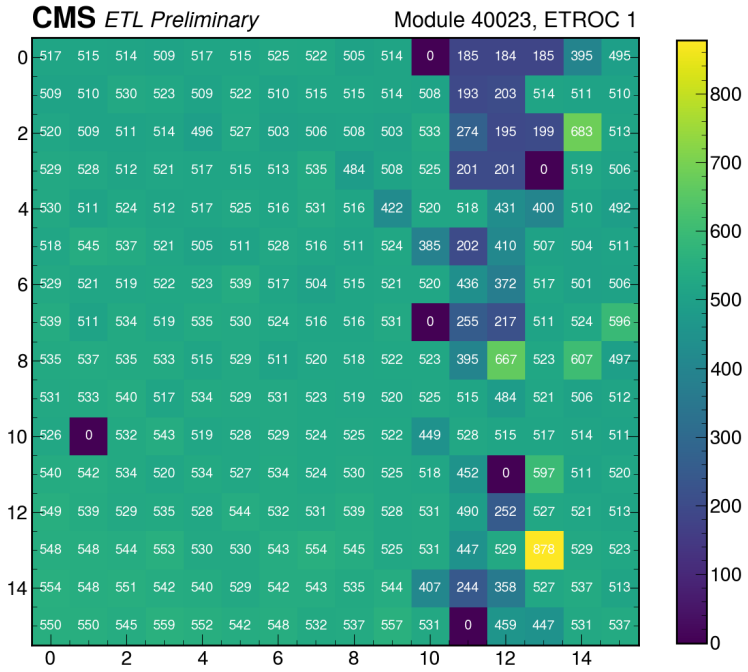
Baseline and Noise width distribution

- 10-bit DAC threshold generation for discriminator from 0.6-1V with VREF=1.0V
- Adjust the threshold to get the different hit rates => S-curve for each pixel
- Auto threshold scan function: controlled via I2C and results (baseline and noise width) saved in registers
  - ETROC2 manual: CMS ETL meeting indico page
  - ETROC paper on auto threshold scan calibration

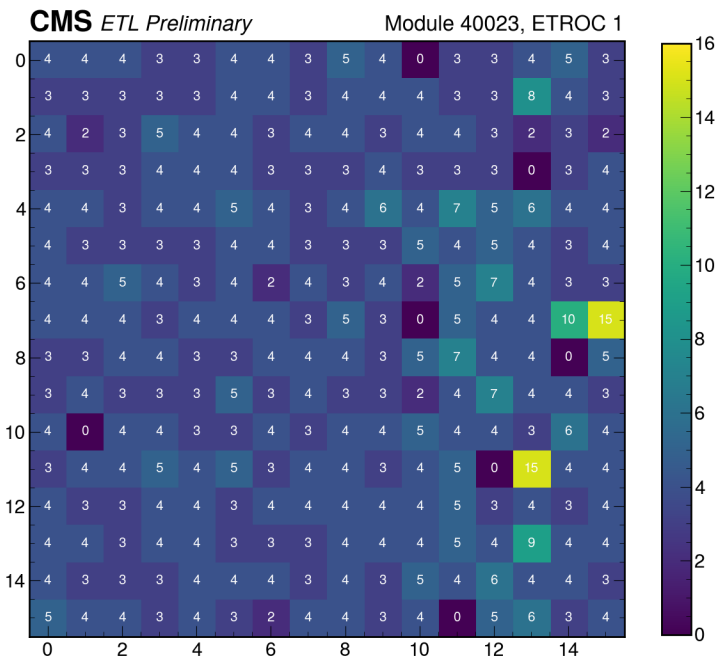
Auto Threshold Scan

Auto threshold scan with RDO+CMS ETL ETROCs: good elink status in the end
=> good elinks status = KCU can correctly decode data from ETROCs with expected data headers in order

ETROC 1 Results



Baseline



Noise Width

- Repeated the same results obtained using CMS ETL RB
  - Some bad pixels on these ETROCs
  - Reasonable noise width is ~3-4 DAC counts, while the baseline strongly reply on the VREF

Summary

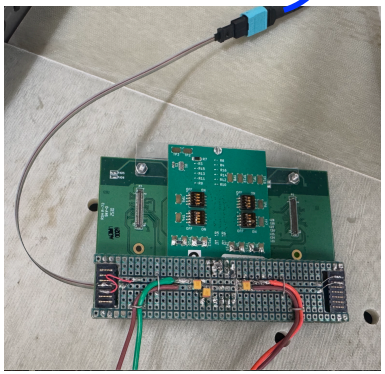
- Last time we reported the loopback test with RDOv1+customized test board to verify interface btw RDO and module:
  - ➡ Analog signals to module board are readout by MUX64+ lpGBT ADC
  - ➡ PRBS test for elink loopback:
    - KCU PRBS generator → lpGBT downlink → lpGBT ePortTx → test boards → lpGBT ePortRx → lpGBT uplinks → KCU pattern checker for each elink
- This time we tested the RDOv1 + CMS ETL module board with three bare ETROCs
  - ➡ VREFs and VTEMPs are monitored via MUX64 + lpGBT ADC
  - ➡ Good elink status: KCU can correctly decode ETROC data
  - ➡ Auto threshold scan: repeated the same results using CMS ETL RB+this module board

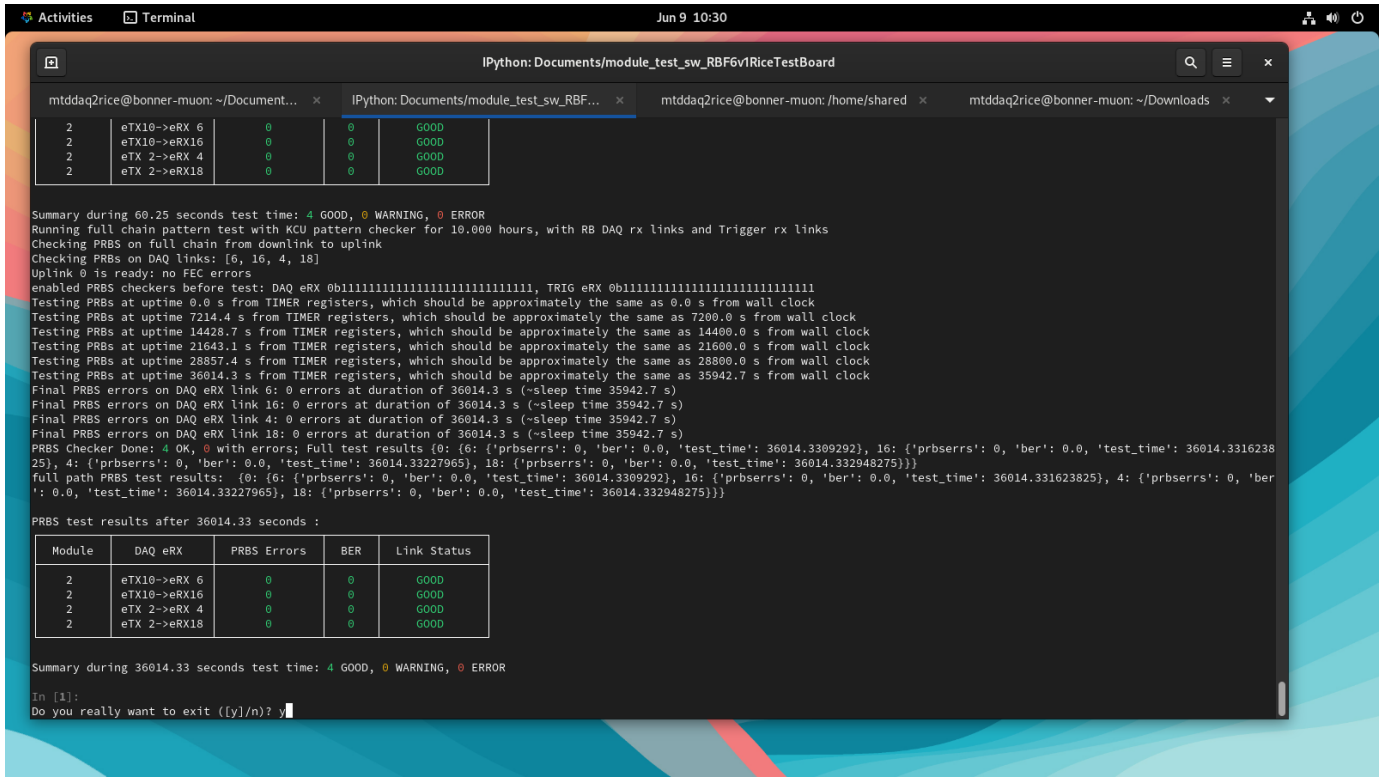
Backup

Long PRBS Test

Full-Path PRBs test

KCU





PRBS test over 10 hours: no error observed

RDOv1 ADCs

RDO ADC+MUX64 readouts with power board:

Reading DAQ lpGBT ADC values:

Register	Pin	Reading (raw)	Reading (calib)	Voltage (direct)	Voltage (conv)	Status	Comment
TH1	0	112	82.693	0.081	0.081	OK	VTRX TH1
MUX64OUT	1	35	0.567	0.001	0.001	OK	MUX64OUT / 2, ADC2 raw
LVRB	2	661	668.295	0.653	13.457	OK	LVRB / 20.6
2V5TX_ADC	3	820	837.897	0.819	2.457	OK	2V5TX / 3
RSSI_ADC	4	586	588.300	0.575	1.150	OK	RSSI current = 0.242 mA
1V2RA	5	570	571.229	0.558	0.558	OK	1V2RA(ADC5), RT1
2V5RX_ADC	6	818	835.763	0.817	2.451	OK	2V5RX / 3
RT2_ADC	7	434	426.163	0.417	0.417	OK	RT2
VDAC	8	993	1022.428	0.999	0.999	OK	VDAC output (internal)
VSSA	9	35	0.567	0.001	0.001	OK	VSSA, Analog ground (internal)
VDDTX	10	526	524.296	0.513	1.220	OK	VDDTX * 0.42, TX supply (internal)
VDDRX	11	527	525.367	0.514	1.222	OK	VDDRX * 0.42, RX supply (internal)
VDD	12	527	525.362	0.514	1.222	OK	VDD * 0.42, Digital supply (internal)
VDDA	13	528	526.424	0.515	1.225	OK	VDDA * 0.42, Analog supply (internal)
TEMP	14	546	545.634	0.533	0.533	OK	Temp = 35.3 C (internal signal)
VREF	15	514	511.501	0.500	1.000	OK	ADC VREF/2 (internal)

Reading MUX64 values:

Channel	Pin	Reading (raw)	Reading (calib)	Voltage (direct)	Voltage (conv)	Comment
HVMON	31	36	1.633	0.002	1.616	HVMON
ADC2	0	335	320.570	0.313	13.229	LVRB
ADC5	1	251	230.959	0.226	0.452	Thermistor
PTAT2	32	90	59.233	0.058	0.706	PTAT2
PTAT1	33	83	51.766	0.051	0.617	PTAT1
GROUND	63	36	1.633	0.002	0.003	Background

Temperature on RB RT1 is: 33.1 C
Temperature on RB RT2 is: 28.4 C
Temperature on RB VTRX is: 30.5 C
Temprature on DAQ lpGBT is 34.9 C
This RB status: All good! Downlink Ready, Uplinks Ready, No FEC errors.