ALCOR development status

Update on ALCOR-64

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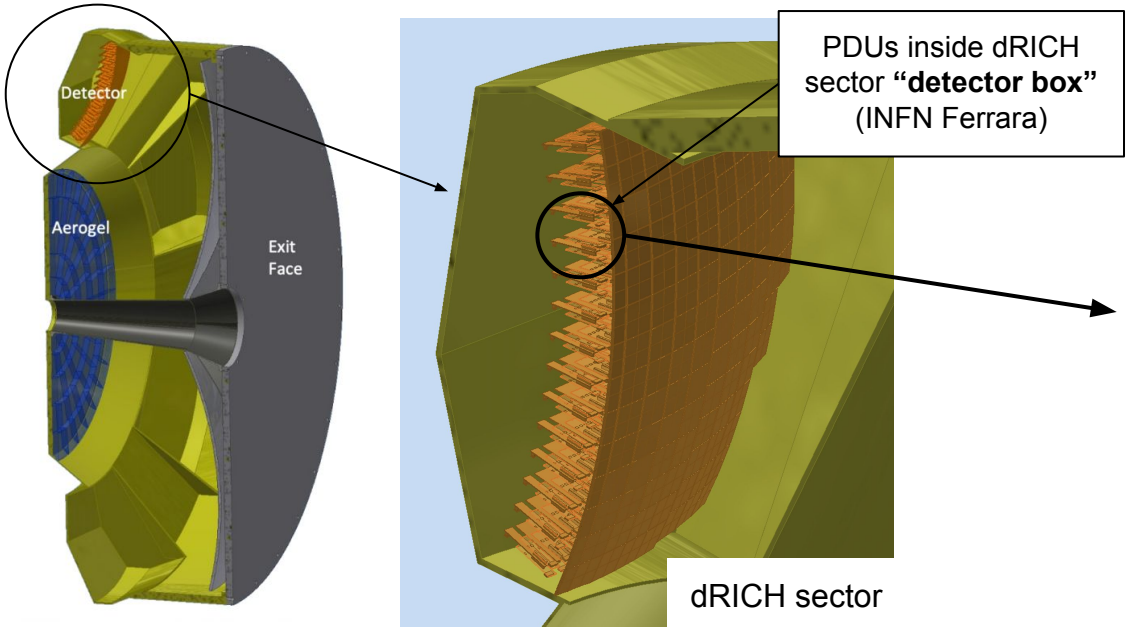
INFN Torino

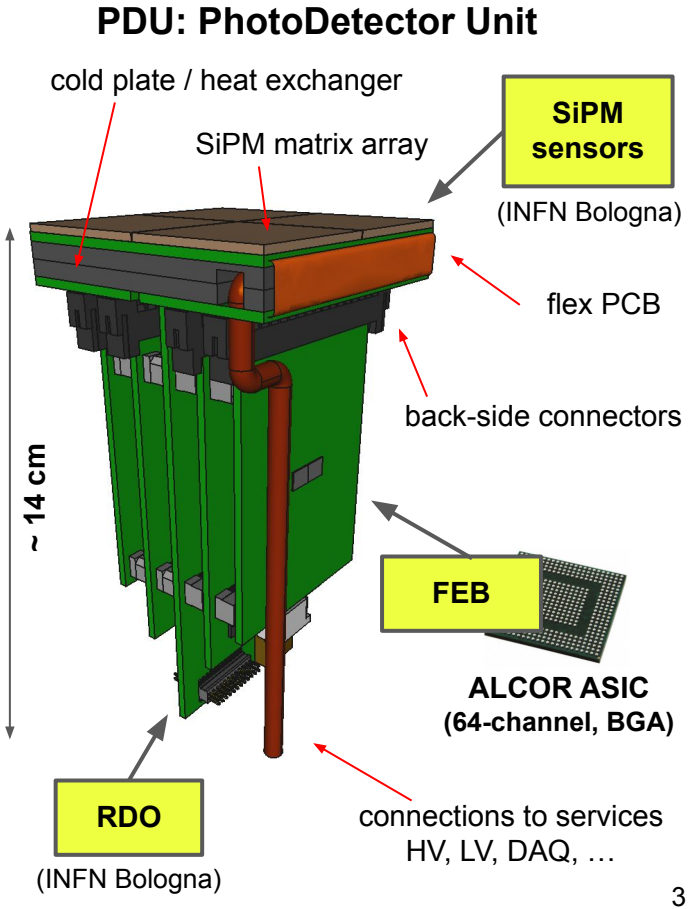
dRICH Meeting
13.05.2026

Outline

- Introduction
- Updates on ALCOR-64
  - BGA packaging issues
  - Ongoing corrective actions
- Updates on ALCOR FEB and other ALCOR boards
  - dRICH ALCOR FEB
  - FEB adapter board
  - ALCOR-32 FEB

dRICH electronics overview





- **1 PDU**: 4x64 SiPM array device (256 channels), **4 FEBs, 1 RDO**
- **1 ALCOR** (64 channels) per **FEB:** 8x8 SiPM matrix readout
- 6 sectors: 208 PDUs/sector → **1248 PDUs** for full dRICH readout
- **4992 FEBs → 4992 ALCOR v3** (64-channel)
- **319488** readout **channels**

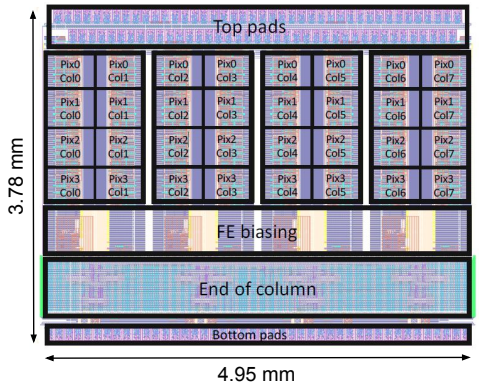
ALCOR: **A** **L**ow power **C**hip for **O**ptical sensor **R**eadout

Main requirements for the ePIC dRICH detector

- ➢ Provide **single-photon time tagging** of signals coming from SiPM sensors
- ➢ Cope with **SiPM DCR: 300 kHz/channel** (at max SiPM radiation damage)

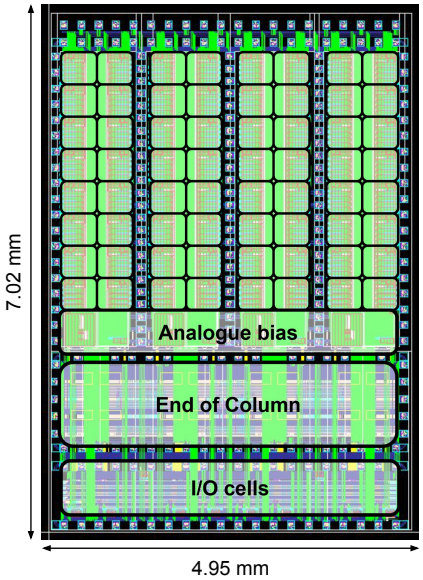
- **32** or **64-pixel matrix** mixed-signal ASIC with on-chip signal amplification, conditioning and digitization
- **ToA** + **ToT** or **Slew-Rate** measurements for **time walk compensation**
- **Triggerless readout**, fully digital output
- Power consumption **~12 mW/channel**
- **110 nm** CMOS technology

ALCOR-32



- ALCORv1: Developed for the DarkSide Experiment for SiPM readout at cryogenic temperature
- **32-channel**, **wire-bond**
- **320 MHz clock** frequency
- 4 LVDS 320 MHz DDR Tx links
- Extensively used within the ePIC-dRICH Collaboration **since 2021** and validated with multiple **successful beam tests** (ALCORv2)

ALCOR-64

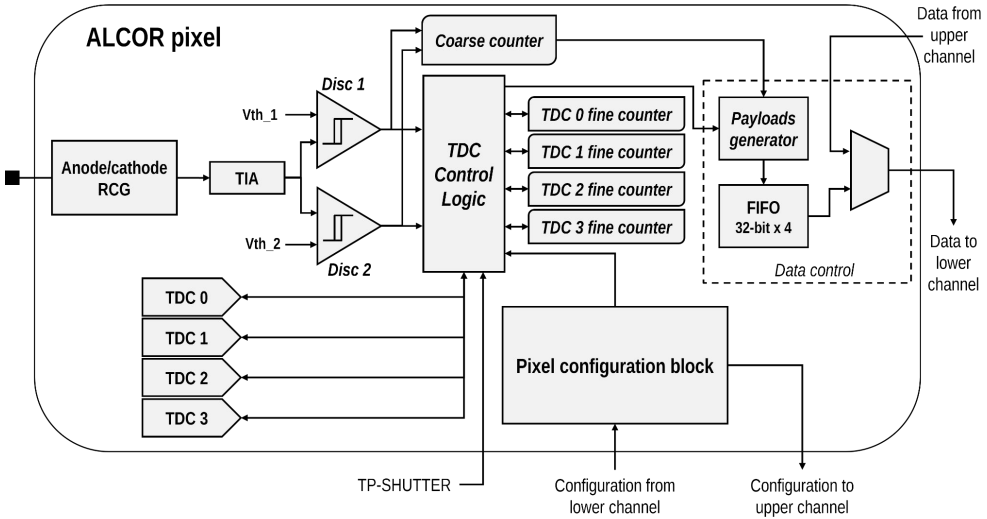


- New version (ALCORv3) with specific EIC-driven features
- **64-channel, FC-BGA** package
- Increased amplifier bandwidth to improve time resolution
- Hardware **shutter**
- **394 MHz clock** frequency
- 8 LVDS 394 MHz DDR Tx links
- **MPW tapeout** on **Apr 2025**

ALCOR pixel architecture

Main requirements for the ePIC dRICH detector

- ➢ Provide **single-photon time tagging** of signals coming from SiPM sensors
- ➢ Cope with **SiPM DCR: 300 kHz/channel** (at max SiPM radiation damage)



pixel size: 440 x 440 μm²

- **Dual-polarity RCG input stage** current conveyor (Z_{in} = 10-20 Ω) + **TIA** with 4 gain settings → $\sigma_t \simeq$ 150 ps
- **2 leading edge discriminators** with independent (and per pixel) threshold settings (6-bit DAC) → V_{th} = 0.5 p.e.
- **4 TDCs** based on **analogue interpolation** with 20-40 ps time-bin (at 394 MHz clock frequency)
- Pixel control logic handles TDC operation, pixel configuration, operating mode and data transmission
- Test pulse injection into the analog FE or TDC + **Shutter** to inhibit events digitization and suppress out-of-time SiPM DCR hits

ALCOR BGA package

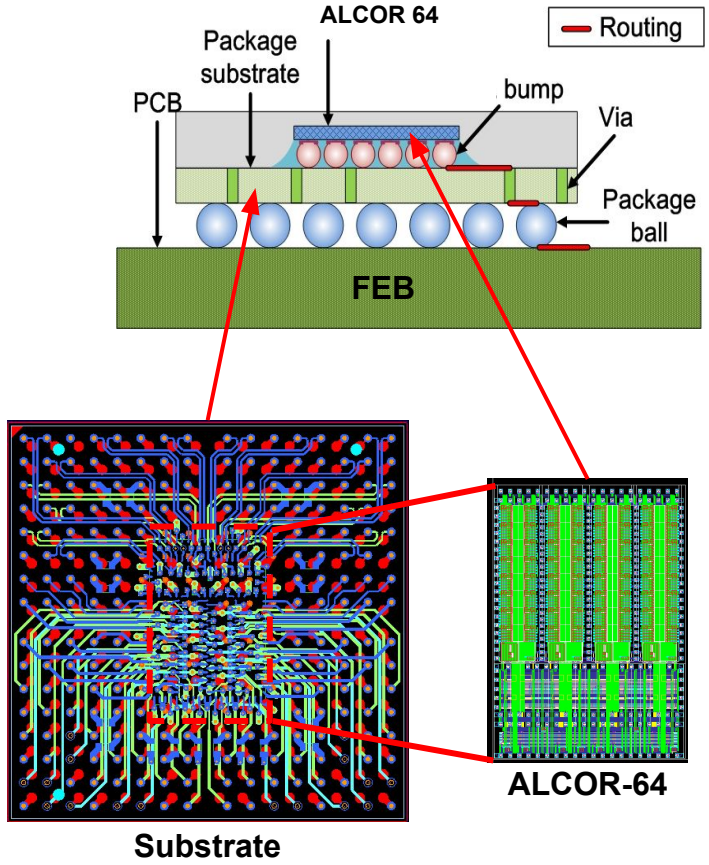
ALCOR-64 → **flip-chip BGA package**

ALCOR-64 fabricated using **MPW run**:

- Tape-out on Apr 2025
- **60 singulated dies** received in Sep 2025, **no full wafers**
- Some processes for packaging more difficult on single dies

ALCOR-64 packaging managed by vendor located in Singapore providing all services (via different subcontractors):

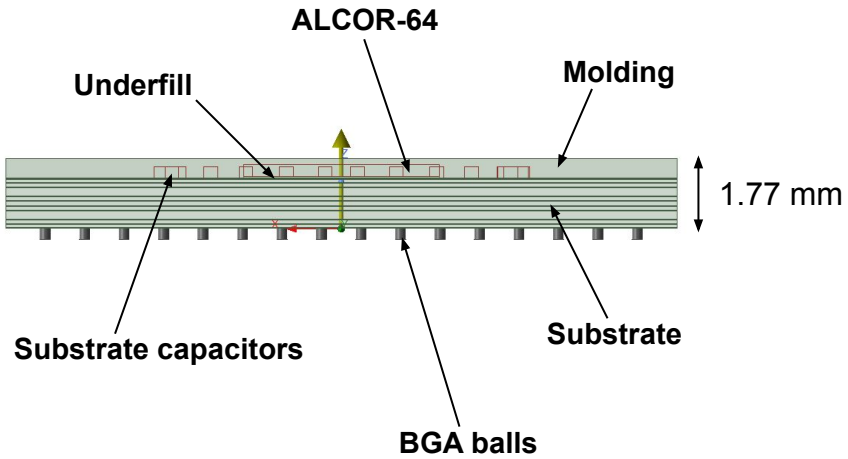
1. **Substrates** production and bumping (substrate design was done by INFN Torino)
2. **UBM** (under-bump metalization) on ALCOR dies
3. **Package assembly**: flip-chip die attach, underfill, molding, balling, etc…

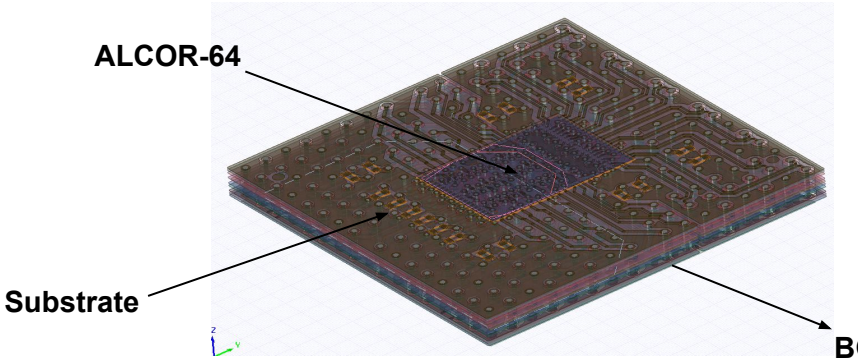


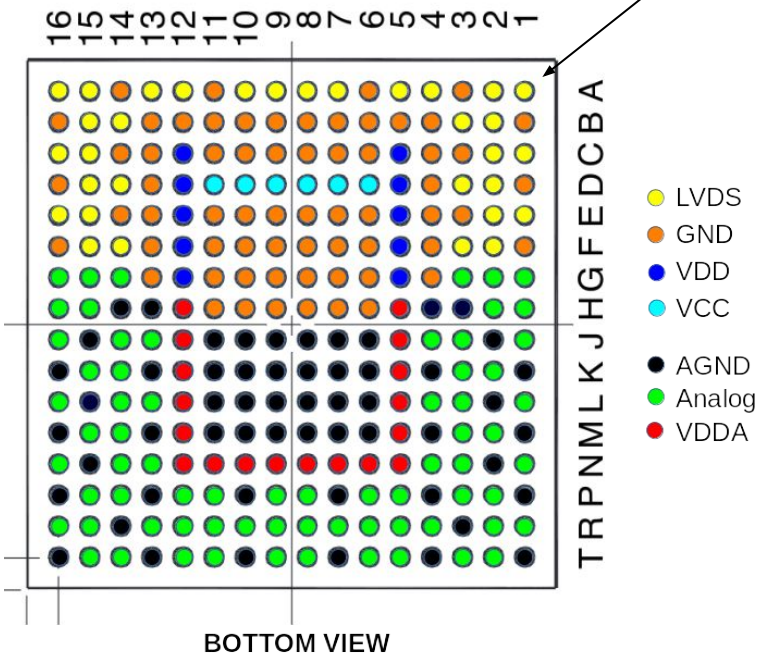
ALCOR BGA package

FC-BGA: flip-chip ball grid array

- BGA 256 (16 x 16)
- Size: 17 mm x 17 mm
- Ball pitch: 1 mm

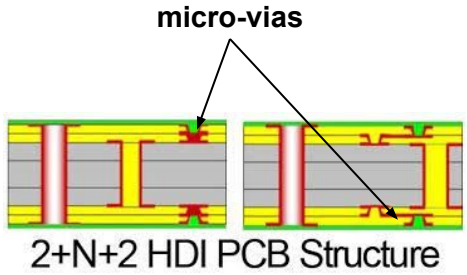


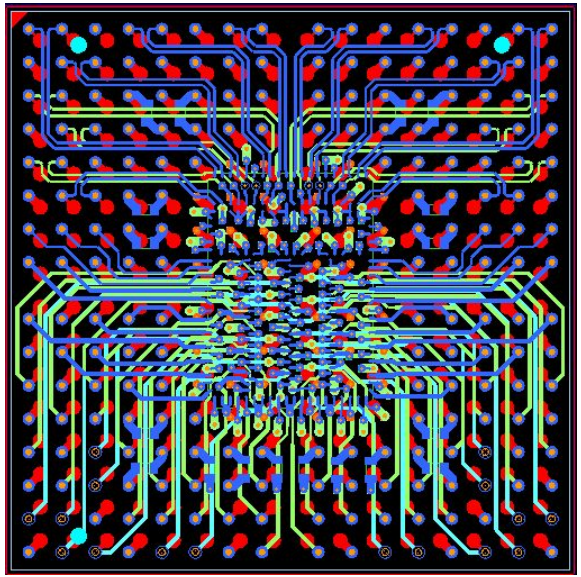




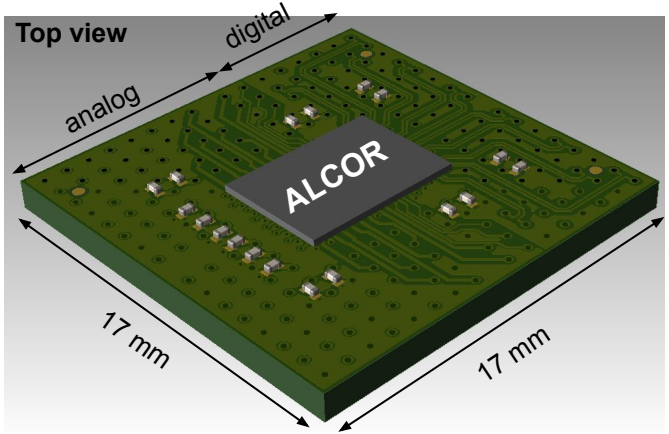
ALCOR substrate

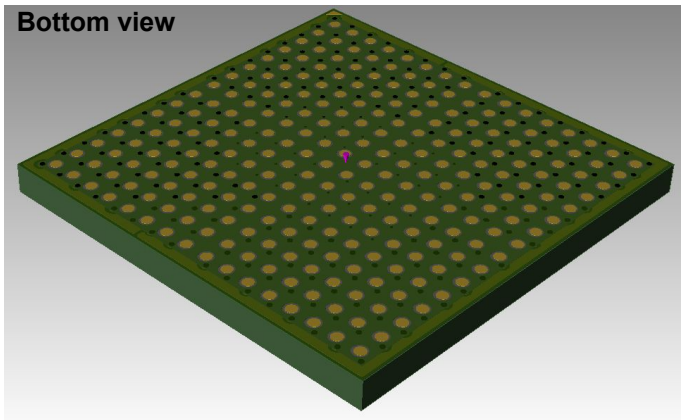
- BGA 256 Ball 17x17mm 1mm-pitch
- BT-Epoxy
- 10 Layers (2+N+2)
- Thickness: 1.27 mm
- Decoupling capacitors (0201)
- Design completed on Jan 2025
- Verification: electrical and thermal simulations



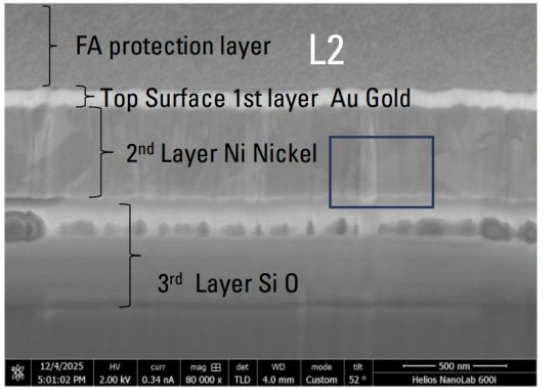


Substrate designed by INFN Torino



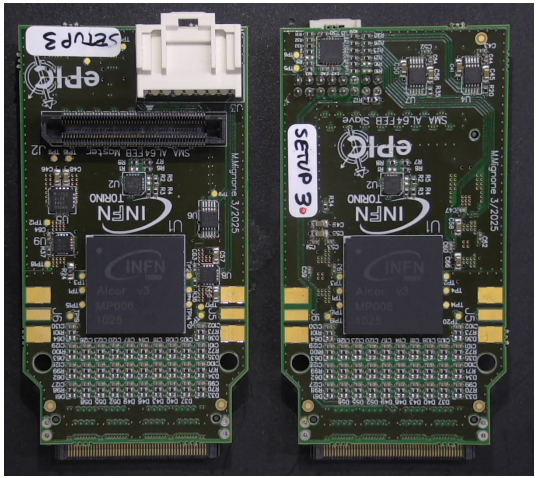


ALCOR-64 packaging status



Nov 2025: 1st Run flip-chip die attach failed due to solder overflow causing short circuits between bump pads

- **FIB dissection + SEM-EDX analysis** (Dec 2025) on one die showed that **UBM layers (Ni/Au) extend beyond the bump pads**, covering additional areas of the chip surface above the passivation layer
- This metalization **creates a wetting surface** that facilitates solder migration from the substrate-side bumps to the die, leading to **short circuits between adjacent pads**
- UBM process managed by packaging vendor (via different subcontractor)



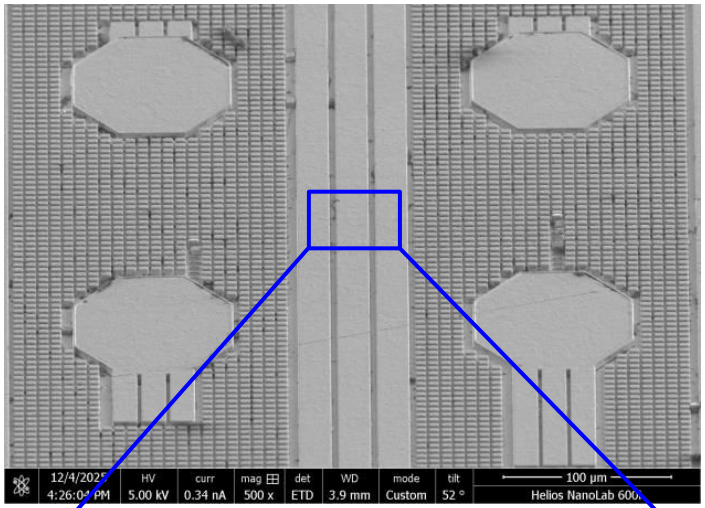
Jan 2026: packaging vendor confirmed issue on **UBM** and proposed a **recovery solution** (*gold stud bump)* to reduce/avoid solder overflow:

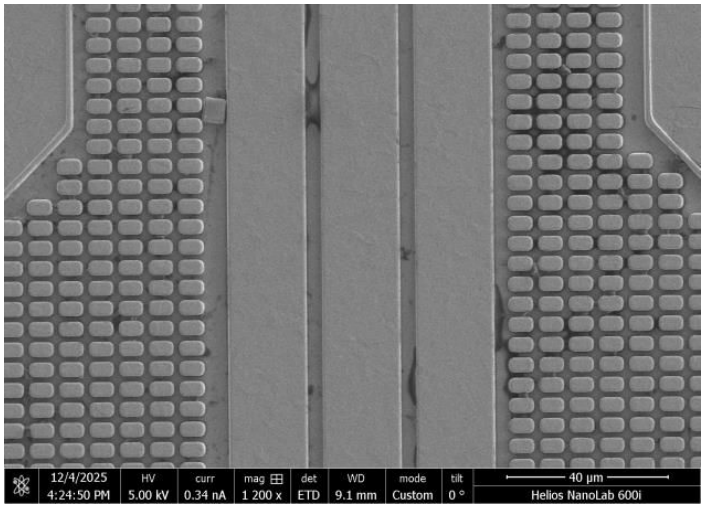
- Completed packaging on 4 ALCOR dies using recovery solution
- BGA devices received in February and assembled on 4 ALCOR FEBs

Mar 2026: Critical issues on all 4 tested devices: many short-circuits and some open-circuit on ALCOR pins

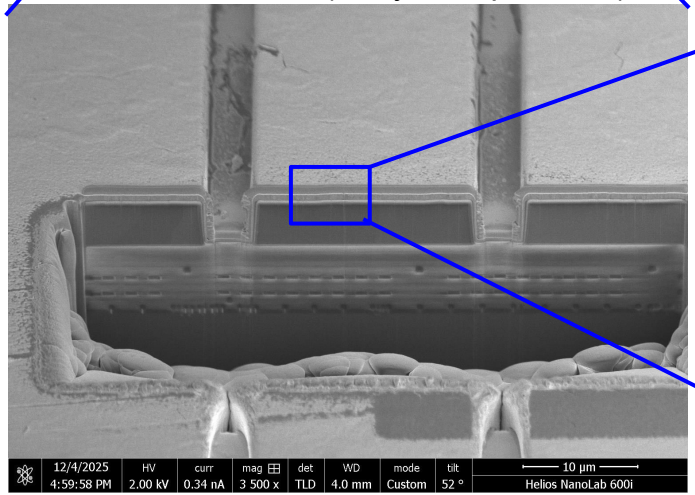
- Short-circuit pins correspond to adjacent bump pads on the chip, this spatial correlation strongly support the hypothesis that the UBM metallization between pads facilitates solder overflow, creating bridges during the reflow process

Results from FIB dissection + SEM-EDX analysis

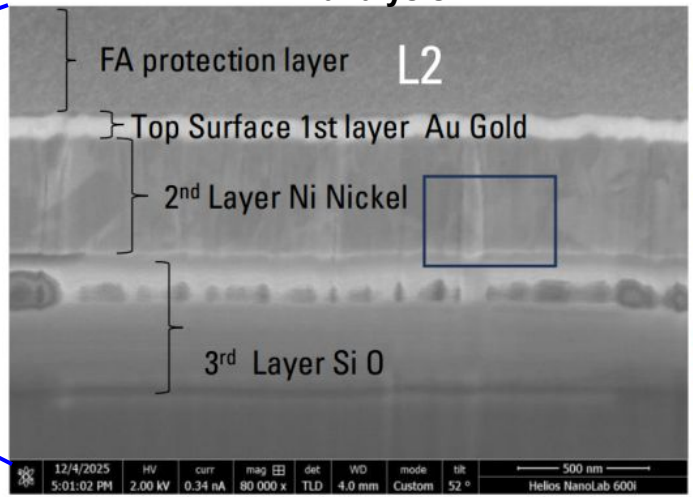




FIB dissection (away from pad area)



EDX analysis

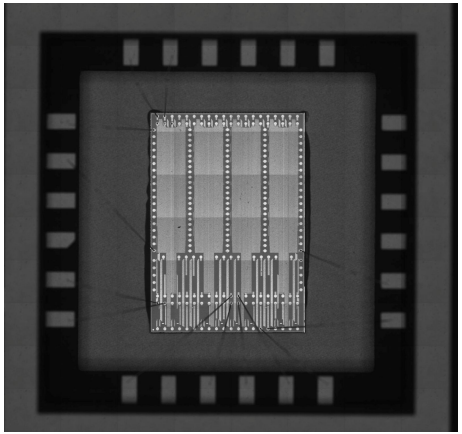


Au and **Ni** layers are from **UBM process** and they are above chip passivation layer, in an area away from bump pads

This shows that we have exposed metals between pads

ALCOR-64 packaging status

Apr 2026: **impedance measurements**, probing directly on the bump pads of the remaining bare dies in Singapore



- Check if open/short circuits are already present before the assembly process
- **Tested dies already underwent the UBM process** (we do not have any untouched dies w/o UBM)
- **Shorts already present**

If situation is not recoverable we need to define the necessary corrective actions and next steps:

- Started discussions for a **new MPW run** and **alternatives for UBM process** → next slide
- This issue introduces an important **delay** in our **schedule** → next slides

ALCOR-64 not available for the dRICH beam tests in May-June 2026: we will use the old front-end electronics based on ALCOR-32

ALCOR-64 packaging status

Alternatives for **UBM process** and **new MPW run**

- IMEC informed us that its subcontractor should be able to support Lead-Free **bumping** on our design
  - UBM + bumping
  - Information **to be confirmed** → more infos from IMEC (costs, lead times, in-house/OSAT) expected very soon
- IMEC informed us that **new Flip-Chip TLR** has been introduced by the foundry this year
  - ✓ Possibility to implement an RDL directly on ALCOR
  - ✓ Simplify BGA substrate and flip-chip assembly → improved reliability and yield
  - ✗ If new pad geometry is required to meet RDL or UBM design rules (checks ongoing), there will be new NRE costs for substrates (also *new substrate design*) and assembly → ongoing discussions with packaging vendor and within the INFN dRICH group
  - Information **to be confirmed** with IMEC and the foundry
- Timeline: UMC MPW run available on **September 11th**

ALCOR Tentative Timeline

- **FEB** and **ALCOR** are part of **INFN IKC**
- The whole production batch will be delivered in Italy for QA and integration

ALCOR-64 new MPW run

- Fabrication: Q3-Q4 2026
- Packaging: Q1-Q2 2027
- Testing: Q2-Q4 2027

ALCOR-64 production

- Fabrication (18 wafers): Q1-Q2 2028
- Packaging: Q3-Q4 2028
- Testing and FEB assembly: Q4 2028 - 2029

PRELIMINARY

DISCLAIMER NOTICE: Timeline is **PRELIMINARY** and needs to be **discussed within the dRICH Project**

➢ **Dedicated meeting in Torino on Apr 28th** to discuss about updated schedule and how to cover extra costs for new MPW

➢ **Expected iteration with INFN referees in June**

➔ PDU modules and detector boxes assembly: 2029-31

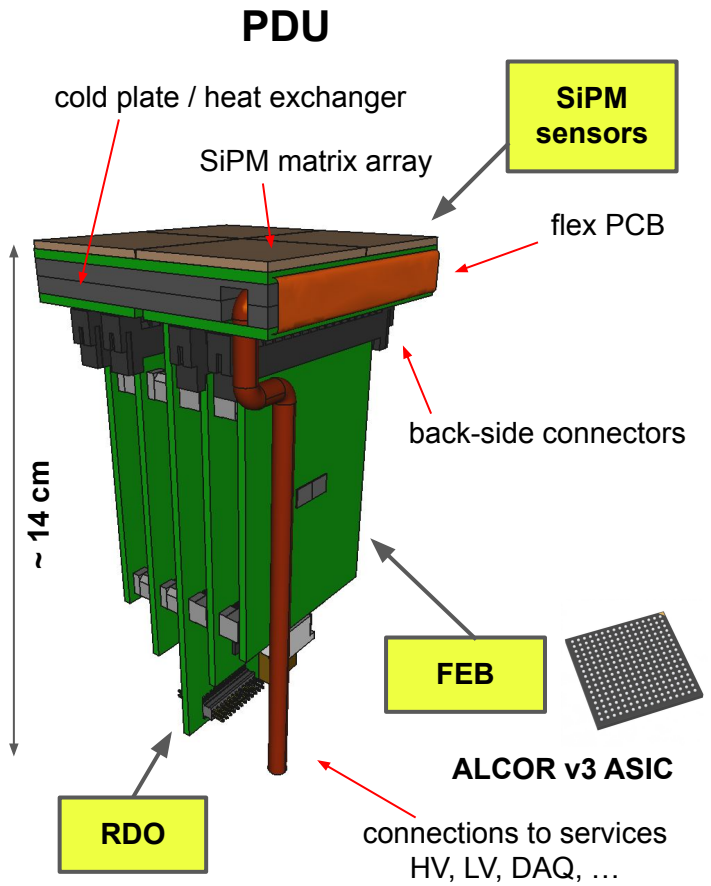
➔ Contingency time exhausted due to ASIC delay, but still on schedule

➔ Fully assembled detector boxes will be shipped to BNL to arrive ~1 yr before installation (Oct '32)

dRICH ALCOR FEB

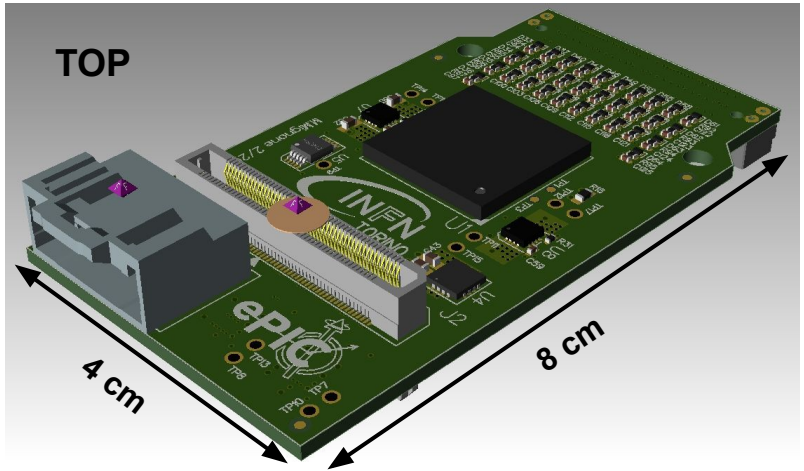
- **4 FEBs** in each PDU (**256** readout **channels**), managed by **1 RDO** (INFN Bologna)
- 2 slightly different versions, they share the ALCOR BUS connector (interface with RDO):
  - ***Master***: internal FEB
  - ***Slave***: external FEB
- FEB designed by INFN Torino, close cooperation with Bologna-Ferrara colleagues to match *RDO design, SiPMs requirements* and *space constraints*
- Design of dRICH electronics (SiPM carrier, ALCOR, FEB, RDO, PDU, detector box, LV/HV services) all done by INFN (BO-FE-TO)

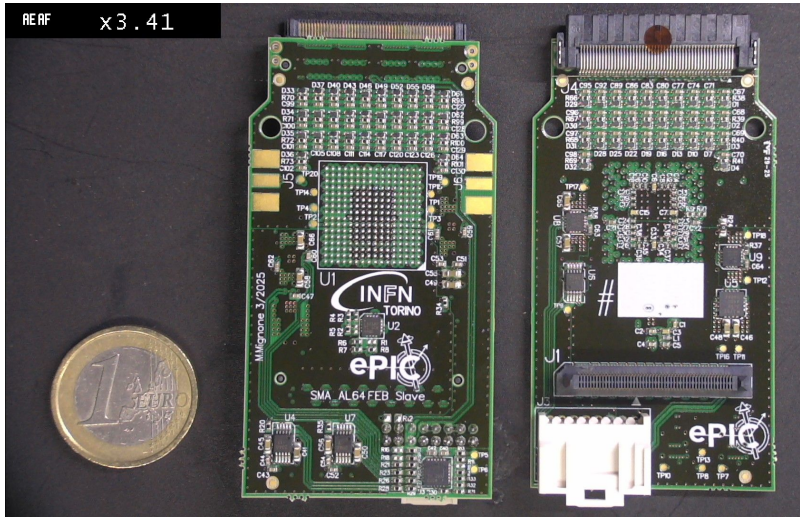
✓ **FEB design completed on May 2025**



ALCOR FEB

- Material: I-Tera MT40
- N layers: 10
- Main components: Linear Regulators, Current monitors, I2C to Parallel-Port Expander, RC high pass filter + annealing circuitry
- Connectors: ALCOR bus, Services, SiPM
- Dedicated PCB section for SiPMs HV routing
  - 2 $V_{bias/annealing}$ PCB layers/sections, each serving 32 SiPMs
  - **SiPM online annealing**: forward-bias, **I=60-100 mA** to reach **T=150°C** on SiPM matrix board
- Power segmentation: LV: 64 channels, HV: 32 channels





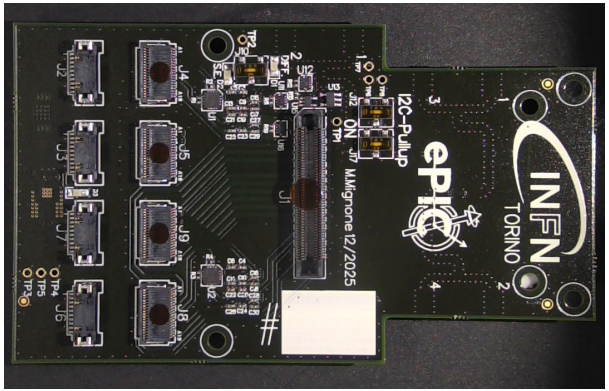
First FEB samples received on Nov 2025

2 extra SMA debug outputs to probe 2 SiPM channels without ALCOR and test annealing procedure

FEB adapter board

Adapter board to **read 2 FEBs using commercial FPGA**:

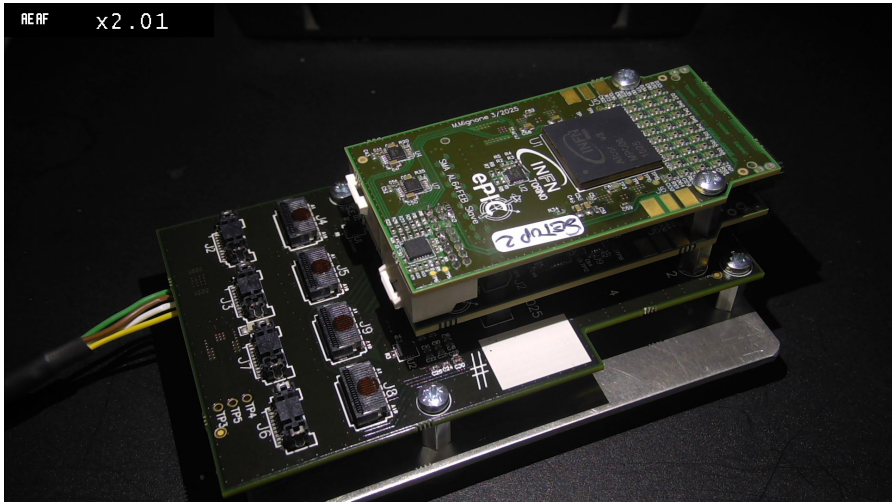
- ALCOR BUS connector: interface towards **1 Master FEB** and **1 Slave FEB**
- FEBs need also I2C power (2.5 V) and control signals (from ALCOR BUS)
- FireFly connectors: **4 FireFly** towards commercial FPGA to support readout up to 2 FEBs



➢ This adapter board will be used for **mass production QA tests**

➢ This setup allows **testing 2 FEBs in parallel**, thus reducing total test time for **mass production QA**

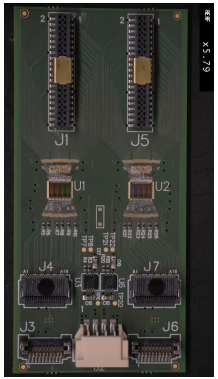
➢ 4 boards received on Mar 2026



ALCOR-32 FEB

New (temporary) FEB to use previous ALCOR-32 with new PDU design:

- Fallback solution while waiting for ALCOR-64
- Laboratory tests
- Detector integration tests
- Firmware/software development
- System demonstrations
- QA setup development



ALCOR FE-DUAL
(dRICH prototype)

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ALCOR FEB
(dRICH FEB)

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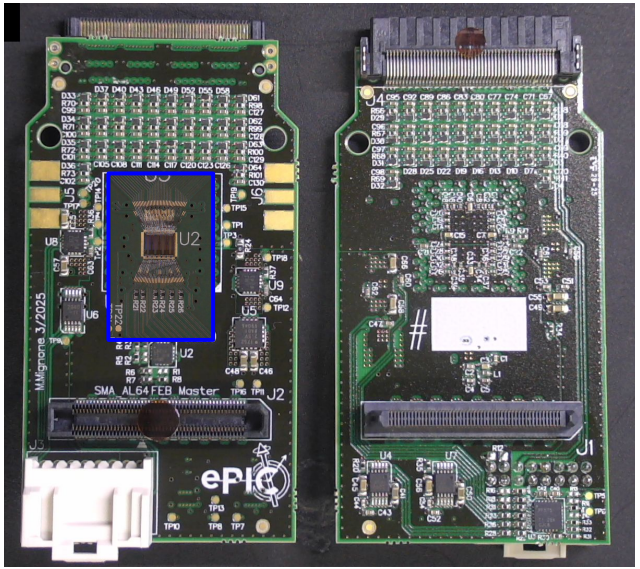

ALCOR FEB-32

Preserve maximum compatibility with the standard dRICH FEB design

- Use the same LDO power regulation scheme as the standard FEB and maintain the same signal pin out and interface logic on the ALCOR bus to minimise firmware/software changes
- Include the annealing circuitry for the SiPM channels
- Main expected limitation: board based on ALCOR-32 will likely support **32 SiPMs only**, rather than the standard **64 SiPMs**
- Design started this week

Summary

- ALCOR is a **64-channel mixed-signal ASIC** adopted for the readout of the **SiPM sensors** for the **ePIC dRICH** detector
- **ALCOR-64** includes all features and specifications required for the ePIC dRICH:
  - 64 channels, BGA package, shutter, 394.08 MHz clock frequency
  - **Packaging issues** introduce an important delay in our schedule
  - Discussions ongoing to find alternative UBM process and preparation for new MPW run
- dRICH **ALCOR FEB** and **QA/QC test-boards**:
  - First FEB samples received on Nov 2025
  - Annealing and temperature tests can be performed also without ALCOR-64
  - FEB adapter card to test FEBs standalone has been developed and produced
  - ALCOR-32 FEB will be developed as a fallback solution while waiting for ALCOR64 (design already started this week)