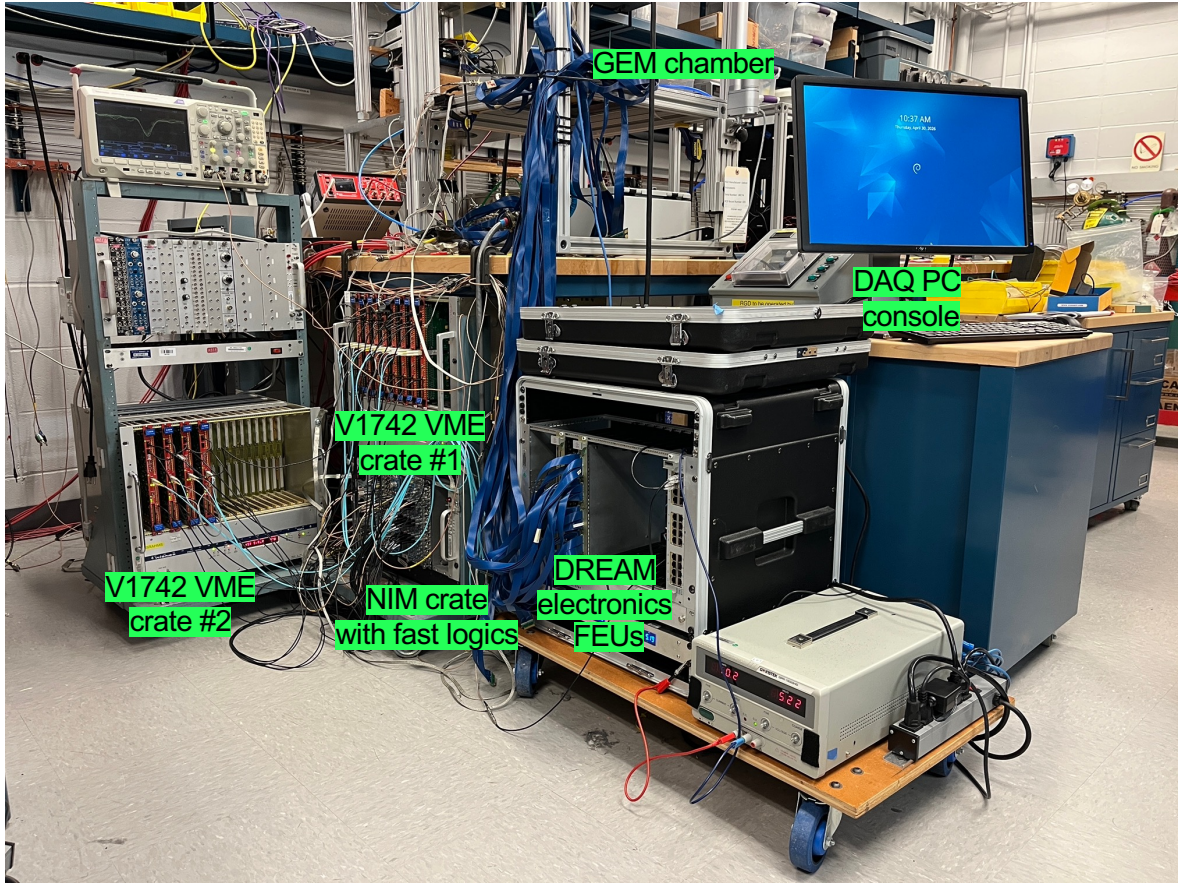
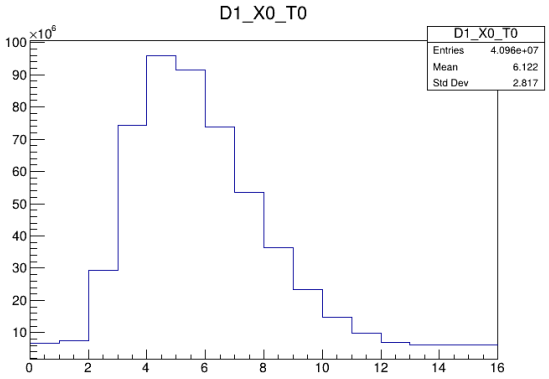
Update on readout hardware integration: V1742s

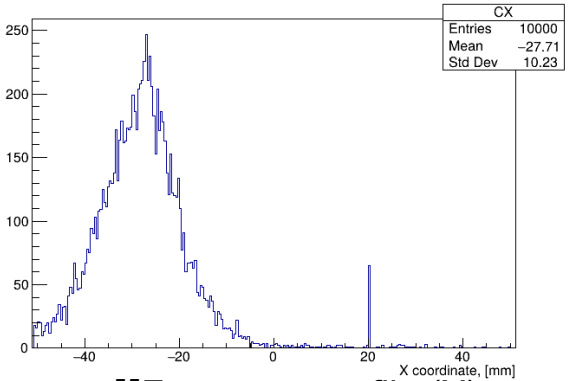


- Presently, 8+4 V1742 configuration
  - Two more on HRPPD QA stand in 2-201
  - Two more on Yifan's aging setup
  - Getting one spare @ CERN from CAEN
  - Have one spare 4-port PCIe card
- Accelerator plugin works
  - Needs testing with a random trigger
  - Use a serial port based latch reset logic
  - 4 ports of each of the two PCIe adapters are still read out sequentially
- ~180 Hz to memory, for 10+ hours
- MCX adapters will be ready today
  - So, there is still time to cable them @ BNL

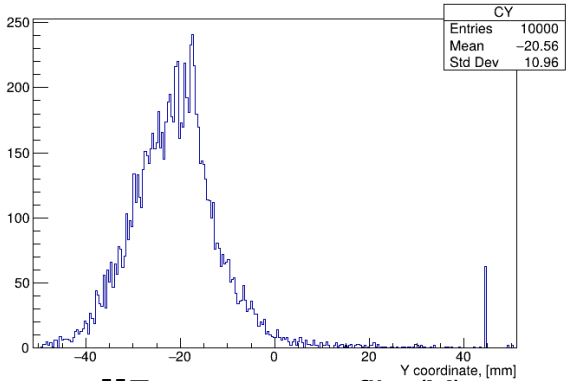
Update on readout hardware integration: DREAM



Waveform



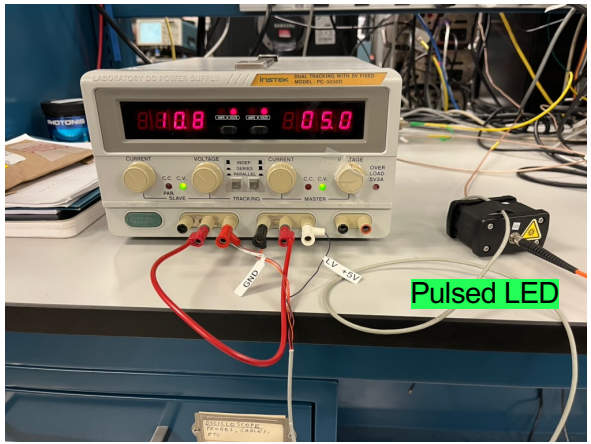
^{55}Fe source profile (X)

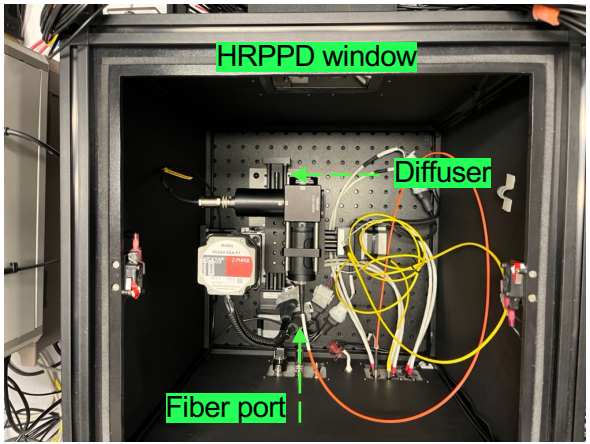


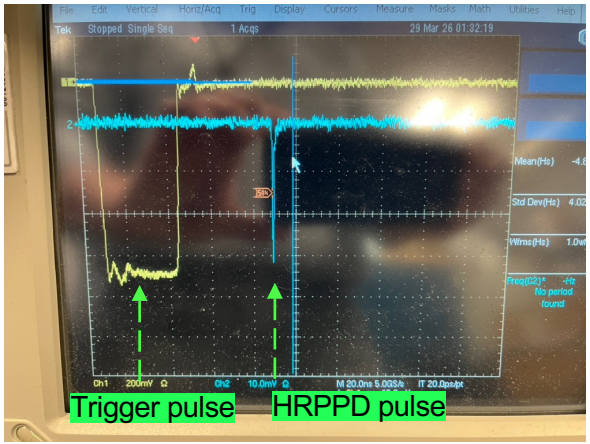
^{55}Fe source profile (Y)

- Tested all four GEM chambers, both FEUs and all 16 cables
  - Some noisy channels seen here and there; nothing extraordinary
  - Tuned configuration scripts (delays, dynamic range), pedestal extraction code, etc
- Two more spare cables were shipped back from JLab this week
- May want to ask Saclay colleagues to provide a spare FEU and a TCM

HRPPD commissioning using a pulsed LED







- Just flood an instrumented HRPPD pad area by a diffuse low intensity LED light
  - Single photon mode *per pixel*
  - Sufficient for a dead-or-alive test, a rough gain uniformity test, and a rough delay calibration
  - No motion control, no long waiting times & no laser safety issues @ CERN during commissioning
- Remove backplanes and ship HRPPDs to CERN in their original packaging
- Assemble back at CERN and *test the same way before the installation*
- A first practical use of the pfRICH light monitoring system concept