Fermilab

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Optimization of FCFD for Integration into Detector System

Sergey Los
For FCFD Design Team

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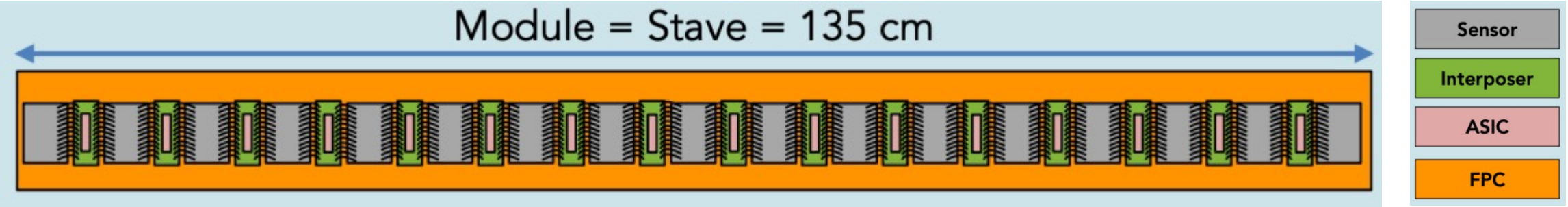
Introduction

- The preliminary conceptual design assumed in the early stages for the barrel TOF detector was based on a hypothetical 128-channel dual-sided ASIC

- As we proceeded with the design of the FCFD1.2 prototype, we carefully evaluated the options from several aspects, that will be presented today

- The new proposal adopts a modular, one-sided ASIC architecture with the following approach:
  - The 128 LGAD channels are read out using **four 32-channel** ASICs
  - Use direct wire-bonding between sensor and ASIC
  - Implement stand-alone modules as the fundamental unit

Baseline Detector Concept

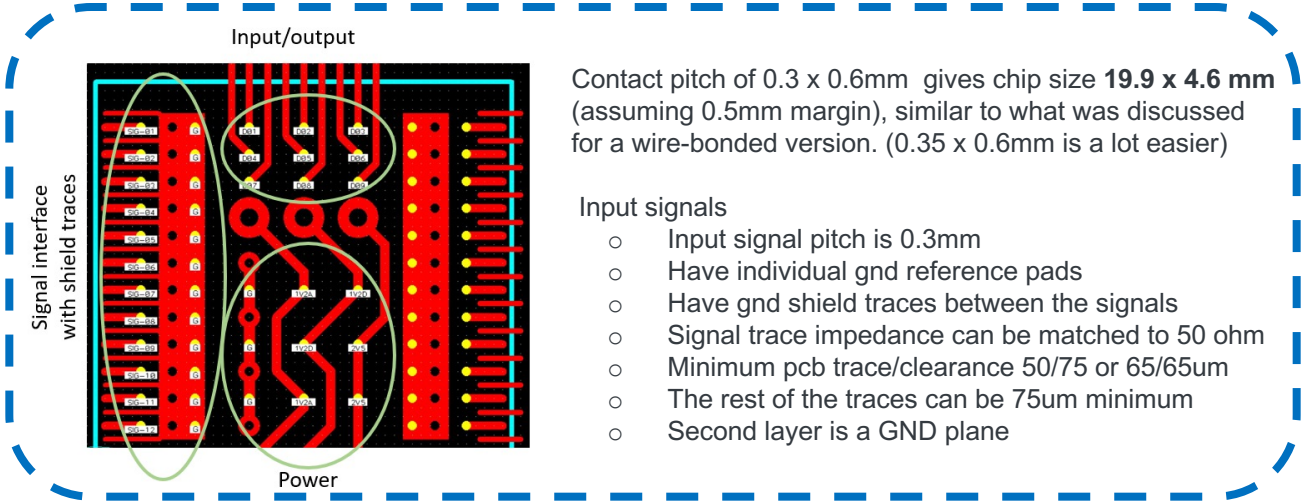


- Sensor
  - Two columns of 10mm-long strips
  - 500um wide strips, x64
  - Effective coverage 20x32mm^2
- ASIC
  - Inputs on left and right
  - 2x64=128 channels
  - Maybe BGA?
- Interposer
  - HDI to fan-in sensor signals
  - Sensor wire-bonded
  - ASIC wire-bonded or flip-chiped
- FPC
  - Power distribution
  - Communication

Assessment of the Original Concept

We considered flip-chip and wire-bonded options for the ASIC

- Both option seemed feasible
- Main concerns
  - HDI parasitics / antennas for sensor signals
  - Heavy fanning-out for direct wire-bonding
  - Potential problems with I/O signal count and ASIC power planning

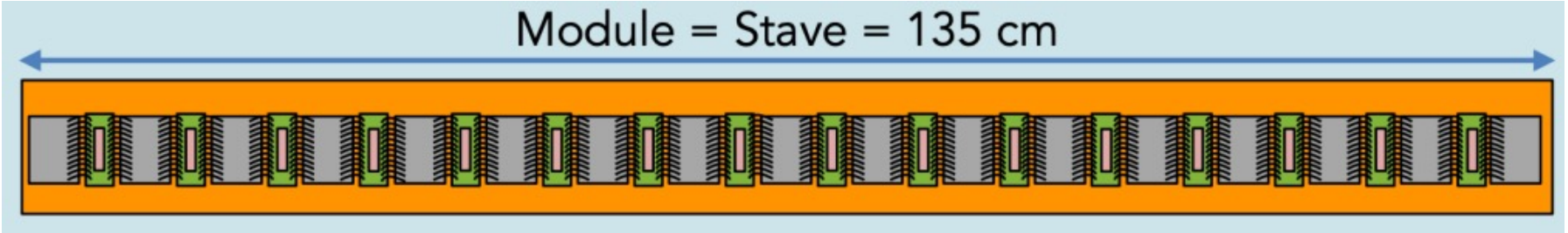


Contact pitch of 0.3 x 0.6mm gives chip size **19.9 x 4.6 mm** (assuming 0.5mm margin), similar to what was discussed for a wire-bonded version. (0.35 x 0.6mm is a lot easier)

Input signals
- Input signal pitch is 0.3mm
- Have individual gnd reference pads
- Have gnd shield traces between the signals
- Signal trace impedance can be matched to 50 ohm
- Minimum pcb trace/clearance 50/75 or 65/65um
- The rest of the traces can be 75um minimum
- Second layer is a GND plane

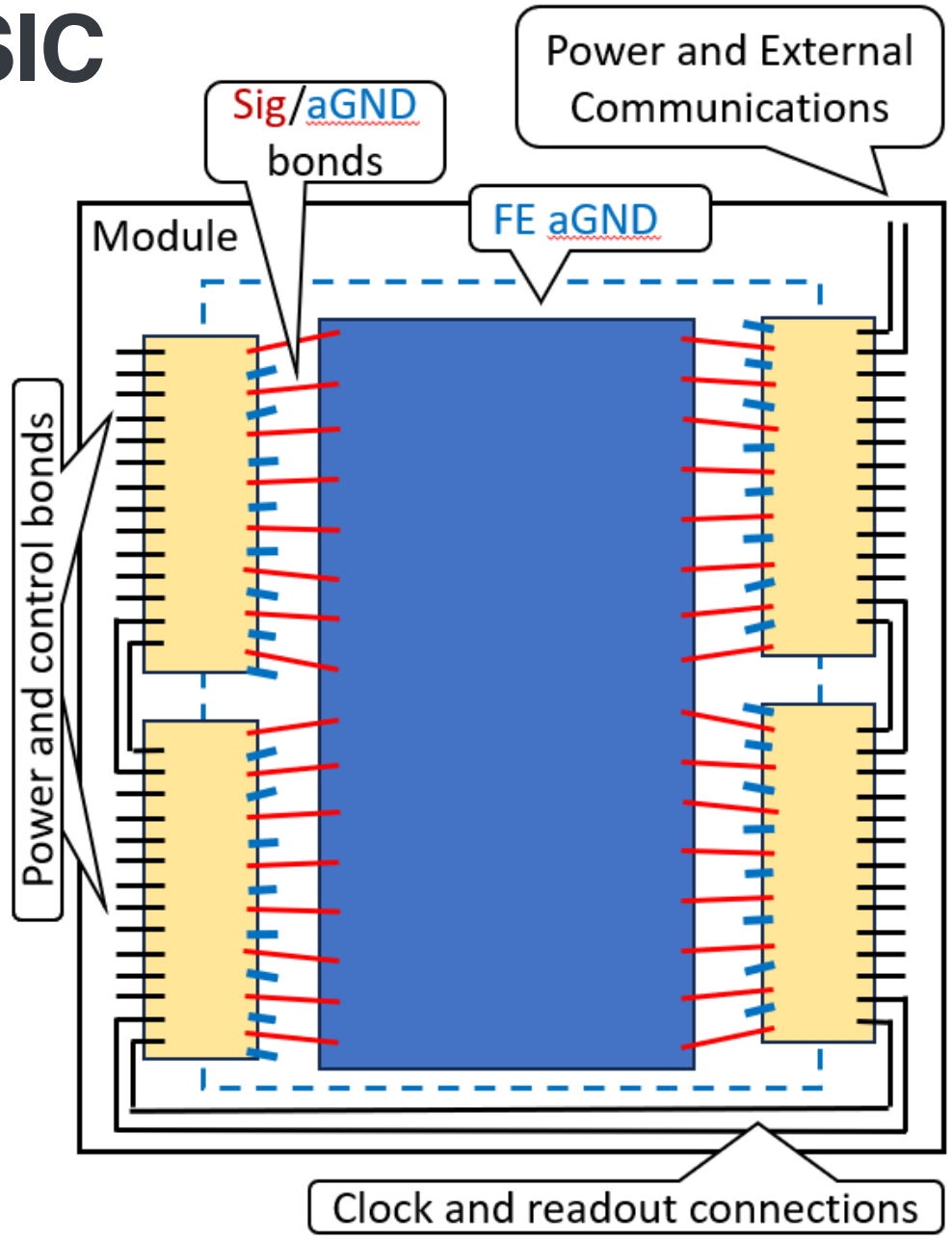
The system issues were realized a bit later

- It's hard to isolate the aGND from the dGND
  - Two haves of the sensor share same aGND (while connected to different ASICs)
  - ASIC should have two separate sets of aGND/aPWR
  - Mounting Sensors on a Flex is risky
- The whole stave is the minimal assembly unit
  - Assembly is difficult
  - Wire-bonding is difficult
  - Repairs are difficult
  - Testing is difficult



Proposal: 32-ch readout ASIC

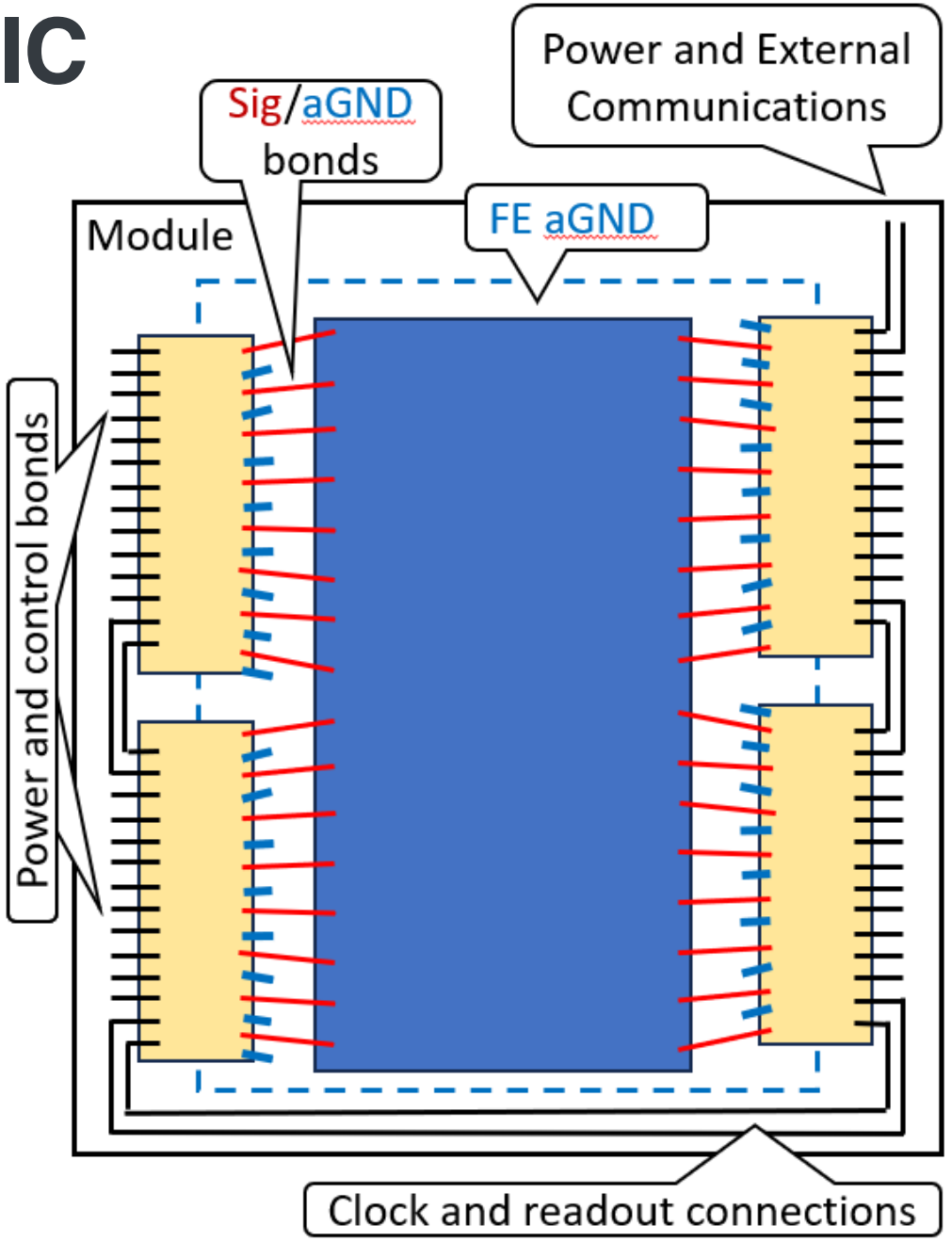
- **Each sensor has dedicated readout ASICs**
  - Simple modules for testing
  - Easy aGND/dGND separation
  - Plenty of real estate for i/o and power
  - No need for half-sensors
- **32-channel ASIC selected**
  - Practical chip size and aspect ratio 14-15 by 2-3 mm
  - Direct wire-bonding to the sensor
  - Channel pitch is slightly smaller than that of the Sensor (0.5mm) so to butt two chips along the Sensor, allowing for a small gap between them. That will cause some fanning of the signal wire-bonds, but not significantly affecting bond length
  - Reasonable fan-out angles (1mm shift for 3-4mm long bonds)
  - All 4 ASICs are connected in a single readout chain



Proposal: 32-ch readout ASIC

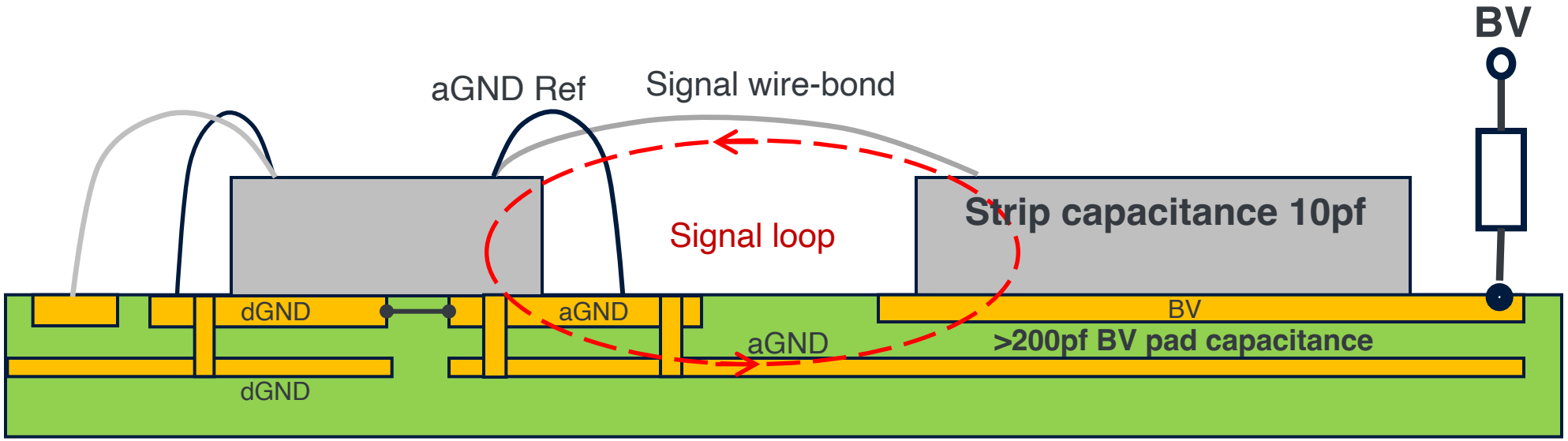
- **This proposal enables standalone modules**
- **Benefits**
  - Direct wire-bonding between the Sensor and FCFD
  - Smaller chip, higher yield
  - Ample real estate for power and control signals
  - Local analog ground improves ground loop immunity
  - Easy to combine multiple modules in a single assembly
  - No need to have half-size sensors
- **Things to watch**
  - Module width <40mm to allow for full coverage in two layers
  - That is about 9.5mm for FCFD on each side:
    - Chip 3mm
    - Sensor-ASIC gap 2-3mm
    - Back-side bonds 1mm
    - Extra routing area 2mm
    - pcb edge clearance 0.5mm

    - **Total 8.5-9.5mm**



Bias Voltage and Signal Return

- **Minimizing Signal Loop**
  - Sensor is mounted on a pcb BV pad
  - FE part of the ASIC is over a pcb aGND pad
  - aGND Ref pads are directly bonded to the pcb aGND pad
  - Second layer copper connects the ASIC aGND to the BV pad using inter-layer capacitance
  - Such layout provides the minimum impedance signal return path



Conclusion

- The **modular one-sided ASIC architecture represents a lower-risk, higher-performance, and better maintainable solution** for the barrel TOF detector.
- It simplifies signal routing, improves grounding isolation, enables modular testing and replacement, and reduces fabrication and integration risks.
    - Moreover, the available module footprint accommodates the required functionality without imposing significant constraints on detector coverage or mechanical integration.

- For these reasons, the modular one-sided ASIC architecture with 32-chanennels per ASIC is proposed as the new baseline design for bTOF detector system integration.

- A detailed discussion of the proposal, and answers to questions we received during the review is summarized in the Record of Decision Document