Electron-Ion Collider

Record of Decision

TITLE	32-channel FCFD ASIC for barrel TOF
PREPARER	Artur Apresyan
NUMBER	EIC-ROD-XX
DATE	April 26, 2026
AFFECTED WBS/PROJECT AREA	6.03.01.07 Detector Electronics
STATEMENT OF DECISION:	The FCFD detector readout architecture will transition from a **dual-sided ASIC with HDI interposer design** to a **modular, one-sided ASIC architecture with direct sensor wire-bonding** as the baseline implementation.

Description/Purpose:

This document summarizes the evaluation and rationale for selecting the optimal integration architecture for the FCFD readout system. The preliminary conceptual design that was assumed in the early stages was based on an assumption of a hypothetical **128-channel dual-sided ASIC**.

Our detailed engineering design has concluded that a design of 128-channel poses substantial risks to the project, and a more optimized configuration based on **four 32-channel ASICs arranged along the sides of the sensor with direct wire-bonding** was developed to address emerging system-level concerns.

The baseline design includes significant additional risks in signal routing, grounding, manufacturability, and assembly due to the reliance on HDI routing and large-scale integration units. These issues impact both **performance margins** and **project execution risk**, motivating a revised architecture. In contrast, the proposed modular architecture simplifies signal paths, improves grounding isolation, and enables independent module-level testing and assembly.

The new proposal adopts a **modular, one-sided ASIC architecture** with the following elements:

- The 128 channels are read out using **four 32-channel ASICs**
- Use **direct wire-bonding between sensor and ASIC**
- Implement **stand-alone modules** as the fundamental unit

Comparison of Architectures

The proposed 32-channel architecture provides significant improvements in electrical performance and system robustness by reducing signal path lengths, thereby minimizing parasitic effects and improving timing resolution and signal fidelity. The use of localized grounding enables controlled signal return paths and a clear separation between analog and digital domains, reducing noise coupling and ground loop issues that are present in the baseline design. In addition, the design enhances manufacturability and overall system lifecycle efficiency.

The smaller ASIC footprint and elimination of the HDI interposer simplify routing and fabrication, leading to higher expected yield. The modular approach enables independent testing and validation of individual units prior to integration, reducing assembly risk and simplifying debugging. It also improves reliability and maintainability through module-level fault isolation and replacement, while providing a scalable framework that supports flexible system expansion without requiring specialized sensor configurations.

The 32-channel architecture, implemented as four smaller chips rather than a single large 128-channel die, provides significant advantages in thermal management, manufacturability, and system flexibility. From a thermal perspective, multiple smaller chips increase the effective heat-spreading area on the flex substrate, as heat can dissipate laterally around each chip's perimeter; consolidating these into a single larger die would reduce the effective cooling area by roughly a factor of two, necessitating a more demanding cooling solution.

From a design standpoint, a monolithic ~32 mm chip presents substantial risks in fabrication, power distribution, and I/O pad density, whereas smaller dies offer a more practical and robust implementation. In addition, the 32-channel configuration provides critical flexibility in sensor layout, allowing variable pitch and multi-layer (staggered) arrangements that are not feasible with a rigid single-chip geometry constrained by wirebond reach.

The 32-channel option maintains a consistent I/O organization and floorplan with the 6-channel prototype FCFD1.2 that was recently submitted. The FCFD1.2 prototype can be naturally extended to 32 channels, as the I/O pads scale with channel count and the overall floorplan remains consistent. This enables reuse of the design elements and reduces integration risk.

Table 1: Comparison of Architectures between 32- and 128-channel solutions

Aspect	**Baseline (Dual-Sided + HDI)**	**Proposed (Modular One-Sided)**
ASIC configuration	128-channel, dual-sided	32-channel × 4 ASICs
Signal routing	HDI interposer fan-in	Direct wire-bonding

Signal integrity	Longer paths, higher parasitics	Short paths, reduced parasitics
Grounding	Shared aGND, complex isolation	Localized aGND, clean separation
PCB complexity	High-density routing	Simplified layout
Assembly unit	Full stave (~135 cm)	Stand-alone module
Testability	Limited	Module-level testing
Repairability	Difficult	Replaceable modules
Manufacturability	Lower yield risk	Higher yield, simpler fabrication
Mechanical risk	Flex-mounted sensors	Rigid modular structure
Scalability	Limited flexibility	Modular and scalable
Development risk	Higher	Lower

The total power consumed to read out 128 channels is about the same with both solutions (4x198=792 mW versus 793mW). A comparison of estimates of the power consumptions for the 32- vs 128-channel chips is shown in Table 2. This table compares the total power of a hypothetical 128-channel chip, without taking into account the complexities, uncertainties and risks of scaling the 6-ch prototype into a 128-channels that are discussed in this Section. We assumed that the unit power for analog components (analog_front end and TDC) will require around 10% larger power consumption in the 128-channel version, due to larger IR-drops and complexities in routing the analog power over the larger chip area.

Table 2: Preliminary estimate of power consumption of various blocks in FCFD 32- and 128-channel options. The totals are also shown for a 128- and 32-channel designs.

	Unit power(mW) (32-ch)	Unit power(mW) (128-ch)	Units in FCFD32	Units in FCFD128	FCFD32_Power(mW)	FCFD128_Power (mW)
analog_front (2.5V)	2	2.2	32	128	64	281.6
analog_front (1.2V)	1.6	1.8	32	128	51.2	230.4
TDC	0.2	0.22	32	128	6.4	28.16
eRx	1	1	2	1	2	1
eTx	2	2	1	1	2	2
Readout16	30	30	2	8	60	240
Serializer	3	3	1	1	3	3
fc_decoder	5	5	1	1	5	5
data_aligner	2	2	1	0	2	0
I2C	2	2	1	1	2	2
Total (mW)					197.6	793.16
Total (mW) for 2.5V					64	281.6
Total (mW) for 1.2V					133.6	511.56

Answers to questions asked during the change request

1. Number of Wafers - Nominal is 3.1M ch, 128 ch/chip, 180 chips per wafer, 133 wafers (w/ 30% overage).
    - The estimated die size for the 32-channel FCFD is approximately **16 × 3 mm^2**. Based on an assumed yield of ~1250 dies per 12-inch wafer, and including a **30% production overage** to account for yield losses, testing, and spares, the total requirement is estimated at **~100 wafers**.
2. Wafer Dicing - ~x4 higher costs.
    - We do not have quotations for wafer dicing for this project; however, based on prior fabrication and packaging experience, we expect this step to have a **relatively minor impact on the overall cost**.
3. Wire-bonding - higher costs as more bonds are needed. Power and interfaces are shared among 32 ch instead of 128, probably proportionally larger chip area also.
    - The 32-channel architecture provides a **simpler and more robust implementation**, particularly with respect to pad overhead for power distribution and control signals. In contrast, a 128-channel design would introduce significant challenges in both **on-chip and PCB-level power distribution**, leading to a large number of required pads. This, in turn, would make **wirebonding highly complex and potentially impractical** due to pad density and routing constraints. The 32-channel solution effectively mitigates these issues by maintaining a more manageable pad layout and interconnect scheme.
4. QA/QC - same total of #channels but more chips. Likely a bit longer to test.
    - The majority of wafer-level tests scale **linearly with channel count**, as key measurements, such as I2C configuration register verification, noise characterization, and S-curve evaluation, are performed on a **per-channel basis**. Additional test steps (e.g., power-on and basic functionality checks) scale with the **number of individual dies**, leading to an estimated **overall test time increase of ~10–20%**.
    - Probing of smaller-area dies is **operationally simpler and more reliable**, as reduced die size relaxes alignment tolerances and lowers the risk of probe misalignment, thereby improving test efficiency and yield.
5. DAQ impact - number of VTRX+/lpGBT from aggregation and/or rates.
    - The current design assumes the **same number** of VTRx+ and lpGBT as in 128-channel solution.
6. Would it be possible to mount the FCFD directly on the support structure. More specifically, I am wondering whether we could introduce an opening under the FCFD to allow direct thermal contact with the carbon support structure, thereby improving heat transfer to the cooling pipe.
    - From the perspective of a **32-channel versus 128-channel architecture**, there are **no fundamental implications for the overall feasibility** of the proposed approach.

- A primary concern lies with the **wirebonding of the full stave assembly**. Due to its large physical dimensions, performing wirebonding on such a structure using a conventional wirebonder would be **extremely challenging and likely impractical**, given tool travel limits, alignment constraints, and process stability over large areas.
- With respect to thermal management, the **power density of the FCFD does not necessitate direct thermal coupling** to the carbon-fiber (CF) support structure. Thermal modeling indicates that the inclusion of a **~0.2 mm flex layer** between the ASIC and the cooling interface results in a modest temperature increase of approximately **3-4 °C**, which remains within acceptable operating limits.

7. I also have a concern regarding FCFD operation in the BTOF system. We plan to use a long FPC bus (~1.3m), with power supplied from one side. In this configuration, a voltage drop along the bus is expected, leading to variations in the supply voltage at each chip. Could you clarify the acceptable operating voltage range for the chip? Given the large (long) geometry of BTOF, local device may be necessary to ensure a stable supply voltage to chips.
    - The expected operating tolerance for the chip power-supply voltages is **±5%**.
    - This requirement should therefore be explicitly incorporated into the **FPC bus specification**, including allowable voltage drop and distribution tolerances under nominal operating conditions.

Table 3: Answers to follow-up questions

Topic	32-Channel Assessment	Comparison to 128-Channel	Net Impact of change to 32-Channels
Number of Wafers	~100 wafers (16×3 mm^2 die, ~1250 dies/wafer, 30% overage)	~133 wafers for 128-ch baseline	**Fewer wafers needed** Smaller die → **higher yield per wafer**
Wafer Dicing Cost	Expected minor cost contribution	Similar scaling concerns	**Low impact overall**
Wirebonding Complexity	Simpler, more robust pad layout; manageable density	128-ch leads to very high pad density and routing complexity	**Major advantage for 32-ch** (feasibility + reliability)
QA / QC Testing	+10-20% total test time; per-channel tests dominate	Fewer chips but same total channels	**Slight increase in testing time**, but manageable
	Smaller dies → easier probing, better alignment	Larger dies harder to probe	**Improved yield & efficiency**
DAQ Impact	Same as 128-channel design	No change	**Neutral** (same number of VTRx+ and lpGBT)

Mechanical / Thermal Integration	No architectural limitation	Same feasibility	**Neutral**
Power Distribution (FPC Bus)	Requires ±5% voltage tolerance control	Same requirement	**Neutral**

Conclusion

The **modular one-sided ASIC architecture represents a lower-risk, higher-performance, and more maintainable solution** for the barrel TOF detector. It simplifies signal routing, improves grounding isolation, enables modular testing and replacement, and reduces fabrication and integration risks. Moreover, the available module footprint accommodates the required functionality without imposing significant constraints on detector coverage or mechanical integration.

For these reasons, the modular one-sided ASIC architecture with 32-chanennels per ASIC is selected as the new baseline design for bTOF detector system integration.

The ePIC Technical Coordination Committee (TIC) of the ePIC collaboration approved the recommendation of the Electronics & DAQ Working group on May 10th 2026 on the adoption of the 32-channel FCFD as the baseline design for the Barrel TOF system.

Approvals

NAME	TITLE	SIGNATURE	DATE
Preparer	Artur Apresyan		
Reviewer	Silvia Dallatorre		
Reviewer	John Lajoie		
Approver	Fernando Barbosa		
Approver	Rolf Ent		
Approver	Elke Aschenauer		