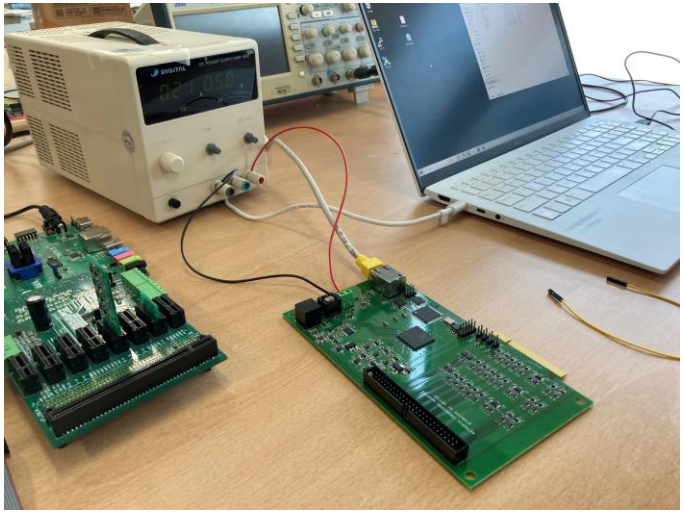
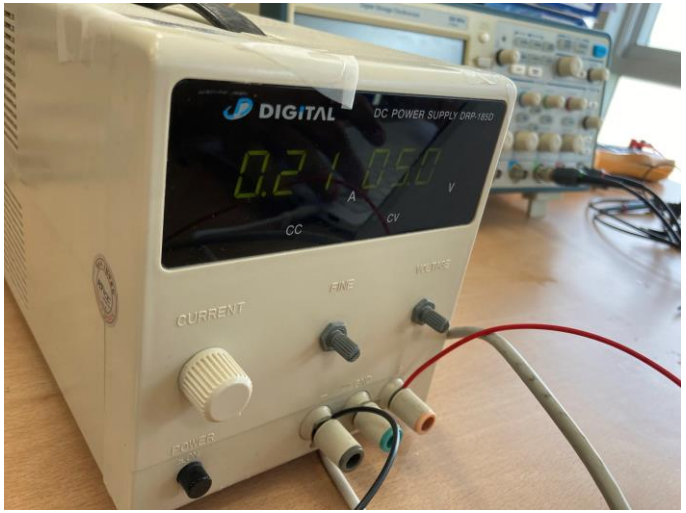
AstroPix BIC wafer/module/stave meeting, June 2nd (2026), C. Kim (PNU)

- **AstroPix-v3 study**
  - Field test of newly produced adapter card
    a. Includes circuit for electrical contact test for pins
       * partially, due to the mistake in the current probe card design
    b. Includes its own power module (receives 5 V):
       b-1. Can provide 1.2 V and 1.8 V powers
       b-2. Can provide negative bias max. -500 V
       b-3. Can measure electrical current being consumed by the chip, which enables I-V scan
    c. Field test results and to do:
       c-1. Confirmed electrical contact test capability
       c-2. Suspicion of large amount of noise being picked up – require thorough check
       c-3. Require physical calibration (by adjusting resistor) for proper I-V scan
  - QA framework development
    a. Understood my misunderstanding on the current A-STEP and its working scheme
    b. Plan to update it into two modes:
       b-1. Default: FPGA-autoread
       b-2. Low-level debug mode: FPGA bypass/no-decoding (can check raw byte stream)

Adapter Features

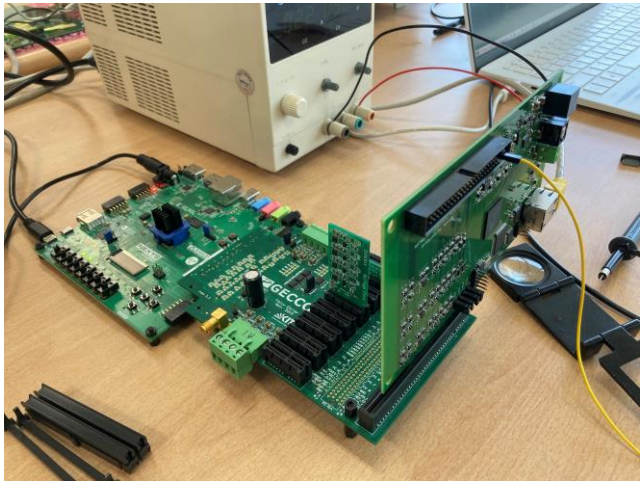




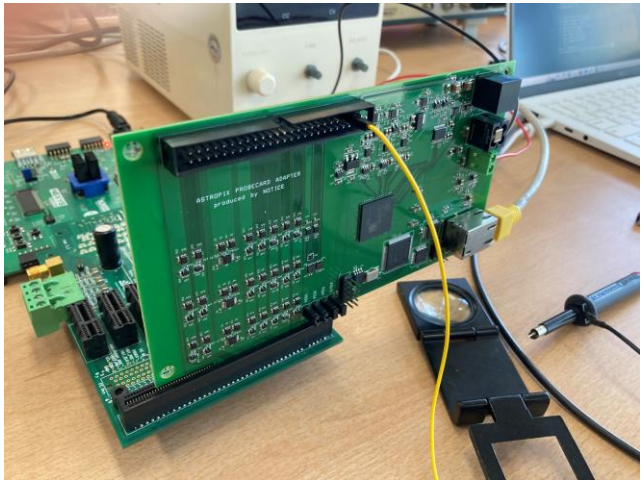
- Interconnect between the Gecco and the probe card
  a. Connection to control: via TCP/IP (ethernet)
  b. Connection to Gecco: via PICe
  c. Connection to probe card: via 50 pin cable
- Can test electrical contact (between the pads on the chip and the probe card's needle)
  * Not all v3 pins can be checked for now due to current probe card design (next page)
- Includes its own power module
  a. Can provide POW4, POW6 (1.8 V), VDD18 (1.8 V), and VSSA (1.2 V), but NOT VDD33 (2.7 V)
  b. Can provide negative bias max. -500 V

Adapter Dry run – mimic electrical contact established

Single pin contact

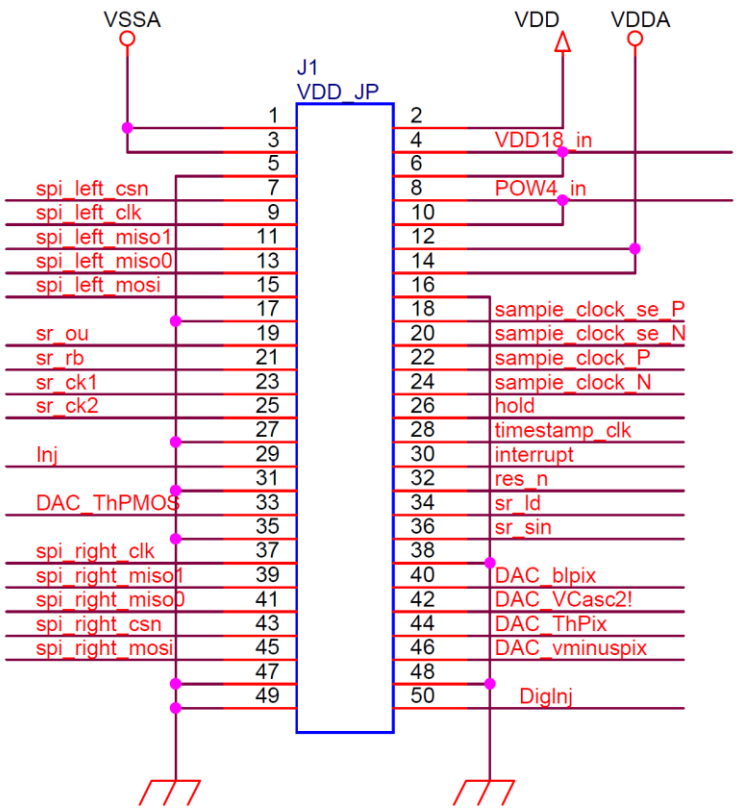


Full contact



Adapter Pins that electrical contact can be checked

50 pins connector (Gecco)

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artifacts:
  contact_bits:
    DAC_BLPIX:          { bit: 1, passed: true, required: true, … }
    DAC_THPIX:          { bit: 3, passed: true, required: true, … }
    DAC_THPMOS:         { bit: 0, passed: true, required: true, … }
    DAC_VCASC2:         { bit: 2, passed: true, required: true, … }
    DAC_VMINUSPIX:      { bit: 4, passed: true, required: true, … }
    DIGINJ:             { bit: 9, passed: true, required: true, … }
    HOLD:               { bit: 8, passed: true, required: true, … }
    INJ:                { bit: 5, passed: true, required: true, … }
    INTERRUPT:          { bit: 10, passed: true, required: true, … }
    RES_N:              { bit: 7, passed: true, required: true, … }
    SAMPLE_CLOCK_N:     { bit: 12, passed: true, required: true, … }
    SAMPLE_CLOCK_P:     { bit: 11, passed: true, required: true, … }
    SPI_LEFT_CLK:       { bit: 20, passed: true, required: true, … }
    SPI_LEFT_CSN:       { bit: 19, passed: true, required: true, … }
    SPI_LEFT_MISO0:     { bit: 22, passed: true, required: true, … }
    SPI_LEFT_MISO1:     { bit: 23, passed: true, required: true, … }
    SPI_LEFT_MOSI:      { bit: 21, passed: true, required: true, … }
    SPI_RIGHT_CLK:      { bit: 25, passed: true, required: true, … }
    SPI_RIGHT_CSN:      { bit: 24, passed: true, required: true, … }
    SPI_RIGHT_MISO0:    { bit: 27, passed: true, required: true, … }
    SPI_RIGHT_MISO1:    { bit: 28, passed: true, required: true, … }
    SPI_RIGHT_MOSI:     { bit: 26, passed: true, required: true, … }
    SR_CK1:             { bit: 13, passed: true, required: true, … }
    SR_CK2:             { bit: 14, passed: true, required: true, … }
    SR_LOAD:            { bit: 15, passed: true, required: true, … }
    SR_RB:              { bit: 16, passed: true, required: true, … }
    SR_SIN:             { bit: 17, passed: true, required: true, … }
    SR_SOUT:            { bit: 18, passed: true, required: true, … }
    TIMESTAMP_CLK:      { bit: 6, passed: true, required: true, … }
  elapsed_s:            0.037224769592285156
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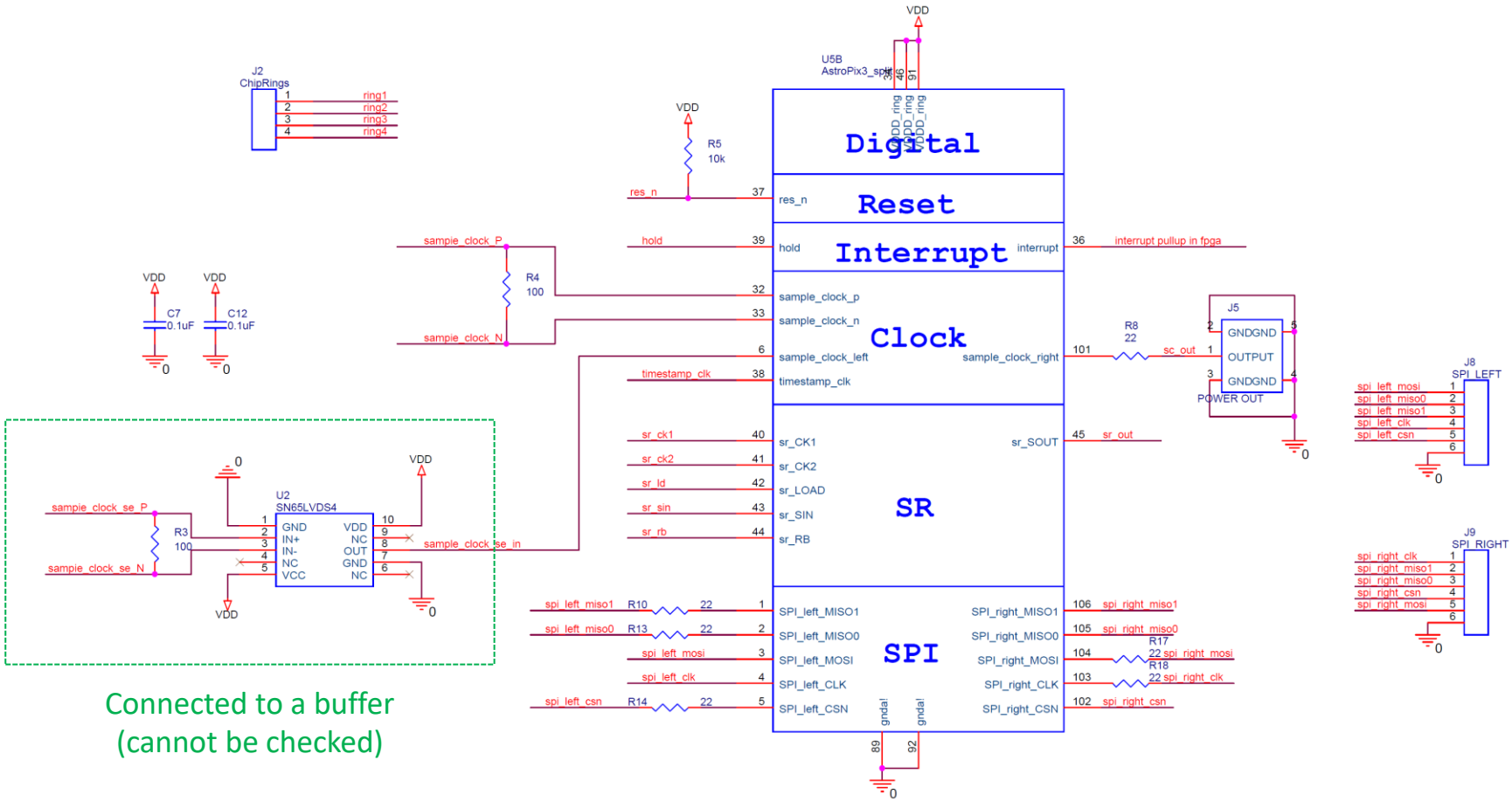
Adapter Pins that electrical contact CANNOT be checked

AstroPix-v3



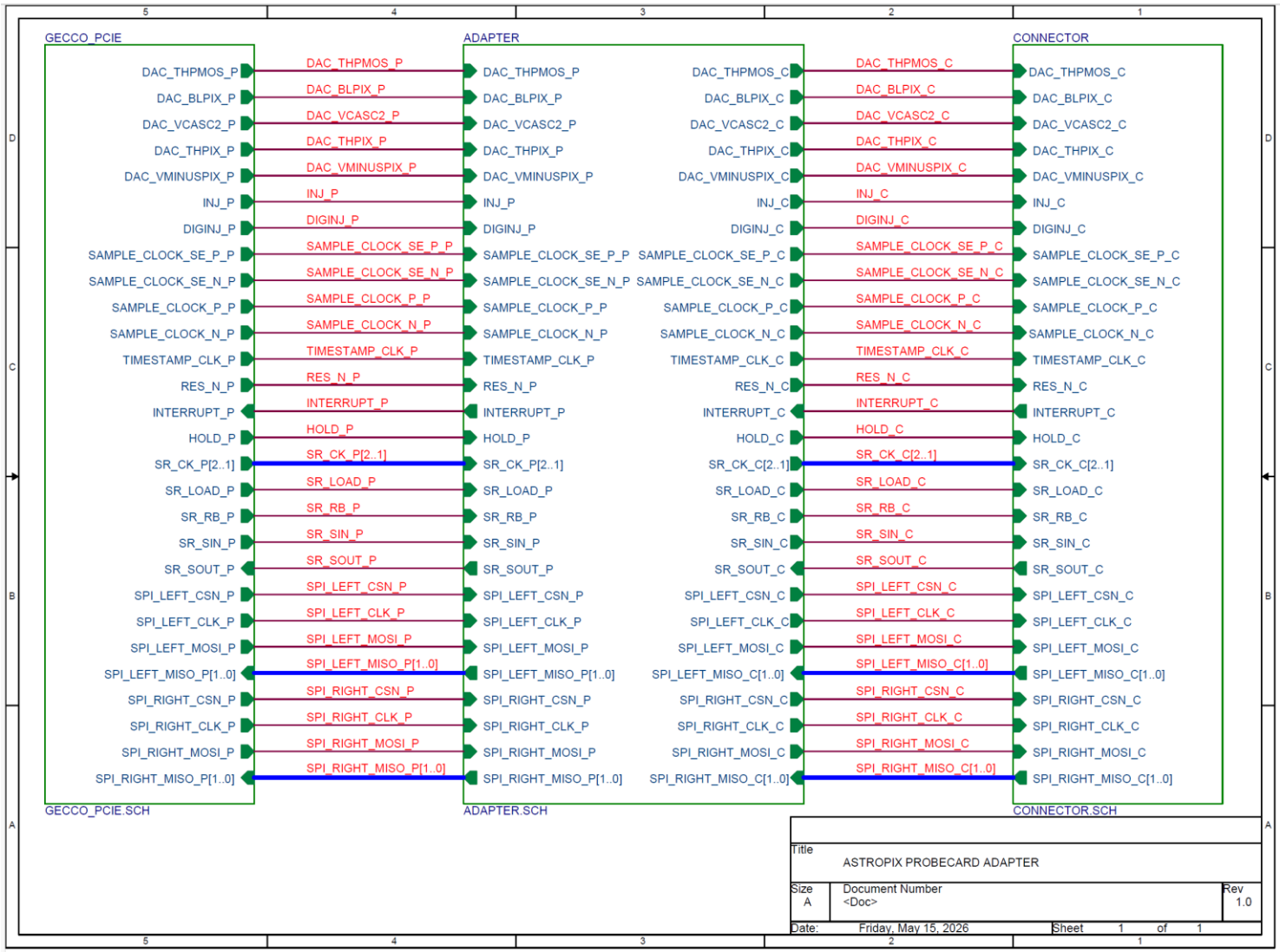
Connected to a buffer
(cannot be checked)

Adapter Done and to do

- **Field test of adapter card**
  - Done:
    a. Confirmed electrical contact can be tested, at least under mimic environment
       * both “a pin is contacted” and “all pins are contacted” cases are checked
    b. Confirmed the adapter can provide power and bias
       b-1. The chip sends and receives info (e.g., interrupt and clock) (* checked by multimeter and scope)
       b-2. DAC – bias calibrated: “ DAC ≈ 7.54434 * |V_bias| - 57.68 “
    c. I-V scan is now available (in the manner of functionality)
  - To do:
    a. Physical calibration (by replacing resistors) is required for proper I-V scan
       a-1. hv_current (consumed) = hv_high – hv_low
       a-2. Currently 1 M, 1 M, and 4.7 M Ω resistors are attached
    b. Software update for proper handling of electrical contact
    c. There’s a suspicion of large amount of noise is being introduced when the adapter is used:
       plan to check thoroughly, by comparing setups w/ or w/o adapter

LAST SLIDE

Backup Adapter – connection



Backup Adapter – GECCO PCIe side