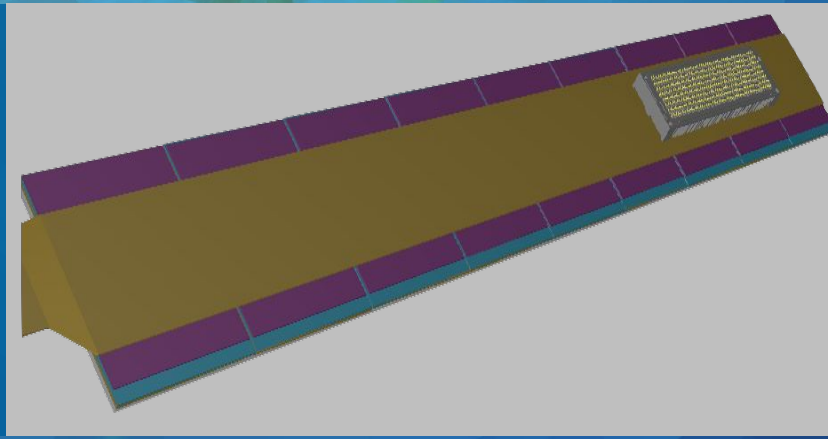
*The ePIC Barrel Imaging Calorimeter*

# Closeout - AstroPix Wafers, Modules, and Staves



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**5th BIC In-person Workshop**
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# Outline

**Thanks a lot for superb work and great discussion and support!**

- Wafer and Modules Updates
- AstroPix Calibration (System Testing + Wafers/Modules)
- Module Tooling and Preproduction Schedule
- Module Tracker Mechanics (Mechanics and Sectors + Wafers/Module)
- Wafers and Module QA/QC and document
- Tracker Readout: ESB, ETC, AstroLinx, AstroPix (ESB/DAQ + Wafers/Module)
- Open Contributions

# AstroPix Closeout & Summary

## Sensor Roadmap & Strategy

- AMS 180 nm CMOS process.
- AstroPix V5 is currently under fabrication; delivery ~October 2026.
- V6 Full size chip (2 cm x 2 cm) while preserving V5 electronics architecture and pad layouts.

## Pre-Production & Production Scaling Targets

- Pre-production timeline target runs from September 2026 through April/August 2028.
- Scope requires qualifying ~5,000 chips to build 400–450 modules, establishing 4 imaging layers across half a sector.
- Full production scale scales up to ~31,000 on-detector modules (~36,000 including yield losses) and ~360,000 chips by Fall 2028.

## Risk Mitigation & Alternative Foundries

- LFoundry technology is being investigated as an independent Multi-Project Wafer (MPW) backup path.
- Offers access to larger sensor formats and backside biasing, serving as contingency rather than an active baseline replacement.

# Detector Calibration Strategy

**The Production Scale Calibration**

- Radioactive source scans for large amount of chips through production phase is big challenge.
- Combined relative/absolute strategy.

**Baseline Charge Injection Workflow**

- V4 internal electronic injection has demonstrated consistent response.
- Primary Path: Utilize electronic injection (ToT -> mV -> Energy)

**Absolute Calibration Options**

- Batch-Wise Calibration: Perform X-ray, laser, or source scans on subset of Modules? - *Check dedicate site which can take on this task*
- On-Detector Tracking: Use MIPs to get in-situ calibration

**System-Level Priorities**

- Establish standard data sets and cross-institutional analysis criteria to maintain consistency across all distributed production sites.

# Chip QC Throughput Planning

**Throughput Requirements**

- Operations (receiving, gluing, bonding, testing) must scale up to maintain a target throughput of ~30 modules per day for 2 years.

**Chip QC**

- South Korea is primary chip QC development and shares assembly production.
- ANL will be backup QC site.

**QC Testing Infrastructure Readiness**

- Probe cards, adapter touchdown card (integrated to Probe card for v5), and automated test stands - ready for testing.
- Initial software automation scripts are being actively validated via AstroPix V3 testing.

**Yield Optimization and Logistics**

- Integrating automated optical image recognition within the pick-and-place to identify and skip defective chip slots.
- Standardized shipping, tray nesting, and handling logistics between S. Korean and USA require optimization.

# Module Assembly & Tooling Development

## Vacuum Alignment & Handling Concepts

- Prototype tooling reviewed and ready for the fabrication
- Minimizes direct chip handling
- Alignment of chip on the module base plate with 100 um gap still needs to work out
    - Pick-n-place machine to lay it down for vacuum pickup tool

## Assembly Sequence

- High-precision with chip alignment via automated pick-and-place equipment.
- Chip glueing to the well aligned module base plates
- Tooling AstroLinx placement and final wire-bonding
- Wirebonding AstroLinx to Chip

## Component Delivery Timelines & Prototyping

- Revised aluminum tracker base plates are expected near the end of July 2026.
- Tooling Fabrication Lead Times: Tooling orders require >2 months; custom gluing stencils for coverage studies take ~2 weeks.
- Mechanical exercises using mock glass and silicon dummy chips

# Adhesive & Wire Bond Protection

**Material Studies**

- Start with Araldite 2011 for chip glueing
- Encapsulation -
  - Soft Polymers: Evaluating soft silicone options. e.g., Sylgard
  - Hard epoxies. e.g., Stycast - 2850FT (heat cure 1-2 min with catalyst).
  - Intermediate Formulations: Semi-soft compound variants are being sourced to find an optimal mid-point – Dymax 9000 (UV Cure)

**Process & Dispensation R&D Tasks**

- Testing hard options first to test the limit.
- Testing mechanical tilt techniques during dispensation to ensure uniform, void-free coverage across wire-bond sweeps.
- Building structural mock-ups to evaluate physical wire-bond strength.

**Technical Evaluation**

- High Voltage (HV) Isolation: Verifying the dielectric strength of the glue interface to prevent bias shorting against aluminum bases
- Glue coverage: Stencil thickness variations to check glue coverage.

# Tracker Mechanics & Tray Integration

**Module locking**

- Direct tray gluing - hard to rework
- A wedge/cam geometry ('quarter-turn T-hole') accessed from bottom
- Foam padding placed over connectors to avoid force from deformation of sector

**Interfacial Thermal & Tolerance Constraints**

- Full-rail contact is evaluated - reduced area due to tolerance specially when at different angles
- Given the 2 mW/cm2 heat dissipation target - physical thermal mock-ups needed.

**Extrusion Vendor Constraints**

- Extrusion vendors cannot build a full-width tray profile.
- Two-piece tray split down a longitudinal center joint.

# Envelopes, PCB Quality Control, & Risks

**Clearance Envelope Deficits**

- The current ~1 mm tray-to-drawer - tight tolerance stack-up
- Protecting wire bonds from contact needs more like 1 mm of additional clearance envelope.

**AstroLinx PCB Quality Control Mandates**

- High Voltage Breakdown: Mandatory continuity and high-voltage spark testing across 100% of production boards.
- Signal Integrity Validation: Batch-wise high-frequency loss testing utilizing dedicated coupons placed on each 4-panel block.
- Contamination Testing: Enforcing multi-stage ultrasonic cleaning, clustered cleaner lines, and mandatory cross contamination tests.

**Critical Path Risks**

- AstroLinx procurement P.O. has not been released - we should anyway go for current AstroLinx
- Rapid testing feedback is needed before finalizing the layout for the astropix V5.

# Tracker Readout

**ETC, ComPair2 FEE**

- Read out 20 lanes of 20 Astropix chips in daisy chaining
- Open questions - follow-up in subsequent meetings
- Event Rate, Pin-out,

**AstroLinx**

- AstroLinx for AstroPix v3 is under fabrication

**ESB**

**DAQ**

- From RDO (ETC) TO DAM - Data protocol
- Testing still need access to digital data directly for QC testing

# Tracker Readout

- **Interface coordination:** Highest priority is alignment between **ESB, ETC, AstroPix, AstroLinx,** and calorimeter electronics teams.
- **Prototype strategy:** Early ETC prototype hardware is encouraged to support integration and reduce schedule risk.

## Priority Actions

- Organize electrical engineering coordination meeting (before end of summer)
- Adam & Blake to define ETC interface requirements with ESB
- Continue development of preliminary electrical architecture
- Prepare subsystem QC documentation using project templates

## Key Decisions

✔ Electrical interfaces precede mechanical integration
✔ Small technical workshops preferred over large meetings
✔ Early prototypes are acceptable and beneficial
✔ Interface definition is the highest near-term project priority

# Open Presentations and AstroPix - Today

| | | |
|---|---|---|
| 08:00 | **AstroPix multi-chip/multi-layer testing**<br>*D172, Building 241* | *Bobae Kim*<br>08:15 - 08:30 |
| | **SiPM Gain Test and LMS Development Status at KNU**<br>*D172, Building 241* | *Shin Hyung Kim*<br>08:30 - 08:45 |
| | **SiPM Summing Board Test at KNU**<br>*D172, Building 241* | *Shin Hyung Kim*<br>08:45 - 09:00 |
| 09:00 | **Light Guide Tests at KNU**<br>*D172, Building 241* | *Bogyeong Seo*<br>09:00 - 09:15 |
| | **Light Guide Tests at UofR**<br>*D172, Building 241* | *Emily Pepper*<br>09:15 - 09:30 |
| | **Fiber QC at ANL**<br>*D172, Building 241* | *Noémie Pilleux*<br>09:30 - 09:45 |
| | **Fiber Mesurements at UofR**<br>*D172, Building 241* | *Zisis Papandreou et al.*<br>09:45 - 10:00 |
| 10:00 | **AstroPix**<br>*D172, Building 241* | *Richard Leys*<br>10:00 - 10:25 |
| | **AstroPix performance updates**<br>*D172, Building 241* | *Adrien Laviron*<br>10:25 - 10:50 |

# Schedule and deliverables

**AstroPix Wafers**

- Test Setup fully commissioned - June 2026??
- Commissioning of chip test stand (v3) - July 2026 —> Can we test few v3 chips this month?
- **AstroPix v3 chip testing - Aug 2026**
  - We had 80 chips in plan to do QC for PED - Is it still possible? (end of Aug 2026, 10-20 chips??)
- AstroPix v5 wafer delivery (6 wafers) **- Oct 2026 (expected)**
- AstroPix v5 chips available after dicing - Nov 2026
- AstroPix v5 carrier boards - Aug 2026 - (KIT designed the board, few final changes remaining)
- v5 Design validation (Pre-Final) - Dec-Feb, 2026
- **Design and Fabrication v5 probe card - Early Aug to early Oct 2026**
- Chip test setup commissioning for v5 - Feb 2026
- Finalize AstroPix QC procedure - June 2027
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- v5 preproduction wafers available - Jun 2027 (submission Jan 2027)
- v5 QC on first 20 wafers - July 2027
- Finish v5 chip QC - Dec 2027  (5 months for 6000 chips)
- AstroPix v6 design - April 2027
- AstroPix v6 fabrication - Nov 2027 (submission in Jun 2027)
- AstroPix v6 design validation and QC - Feb 2028

# Schedule and deliverables

**AstroPix Modules and AstroLinx**

- AstroLinx for v3 - July 2026???
- Readout adaptor board - received at OkState??
- Flex jumper - received OkState??
- First module assembly with v3 chip - July 2026 (Hand assembly??)
- QC’ed v3 module - Aug 2026
- Module assembly tooling available - Aug 2026??
- 6 modules with AstroPix v3 - Dec 2026
- Wirebond potting (encapsulant finalization) - Dec 2026
- 6 v3-modules loaded and tested on Stave - Jan 2027
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# Schedule and deliverables

**AstroPix Modules and AstroLinx**

- AstroLinx for AstroPix chip v5  design - Sep 2026
- AstroLinx v5 fabrication (qty 50??) - Dec 2026
- Assembly tooling updates design and fabrication - Oct 2026 and Jan 2026
- Test fixtures for AstroLinx QC - Jan 2027
- Second batch of AstroLinx v5 fabrication - Feb 2027 and so on (400?)
- End of AstroLinx v5 delivery - Sep 2027
- If needed update AstroLinx for v6 - June-Dec 2027
- Production database - Sep-May 2027
- First Module assembly with v5 chip - Jan 2027
- One Stave ready (12 modules) - Feb 2027
- First Tray ready (6 Staves, 72 modules) - Oct 2027 (after receiving full v5 preproduction chips in June 2027)
- Finish Preproduction v5 Assembly - April 2028
- Finish QC of v5 modules - May 2028
- Assembly of 3 staves using AstroPix v6 chip - Mar 2028 to May 2028 (accomodate during v5 assembly)
- Stave loading using v5 modules - start Nob 2027 till Jul 2028
- Finish v5 module Tray QC and deliver - Aug 2028

# Summary of Near-Term Action Items

- Module Base Plates (Kevin): Confirm delivery timeline for incoming aluminum plates (estimated July end).
- Machining Prototypes: Cut 3 short dovetail-into-module and 3 I-beam double-module lengths for UCSC - Done
- Thermal Bench Testing (ANL): Experimentally verify thermal conduction efficiency across normal vs. inverted tray layouts.
- Araldite 2011 Curing (UCSC / ANL): Curing duration tests and verify electrical isolation performance. Kirsten will build stencils for this study (design and 3D print??)
- Encapsulant Evaluations (UCSC): Initiate formal comparison testing across Sylgard, Stycast, and Dymax materials - Ordered
- Module tooling fabrication (first version) - Expecting quotation this week
- HV wirebond break test at Argonne - will do it at the end-of life of astroPix v3 9chip PCB boards
- HV insulation between chip and Al base plate - Argonne can start it once receive few stencils different coverage
- QC test stand commissioning and automation
- QC Documentation Compilation: Rough draft of Module QC prepared (Need to polish text), AstroLinx and Wafer QC discussed during workshop (when to expect?)

# BACKUP