# FPC design and simulation

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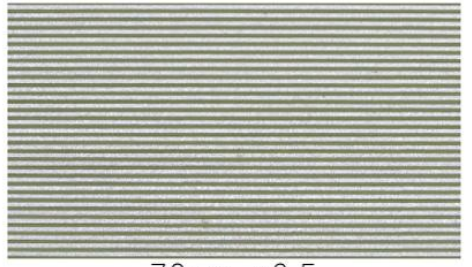
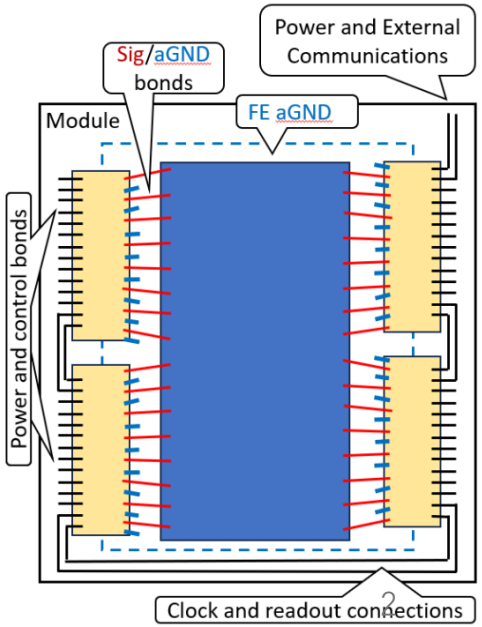
# Introduction


70um_x0.5


70um x5.0

- Several updates were reported in the past few months
  - Mechanical test for Long FPC:
    - 70um Line& space is feasible
  - Updated ASIC design : IO I/F is the same

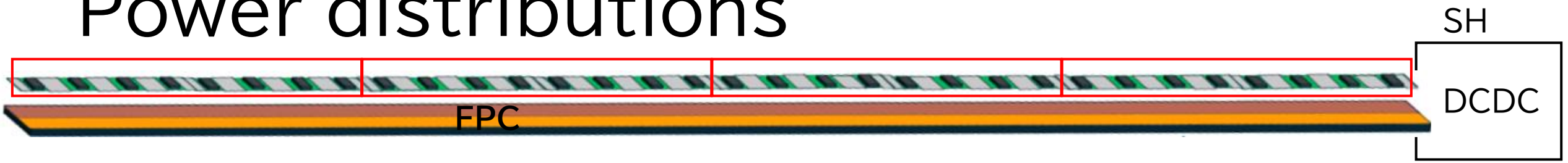
4 ASICs surrounding the sensor




- Re-consider FPC design

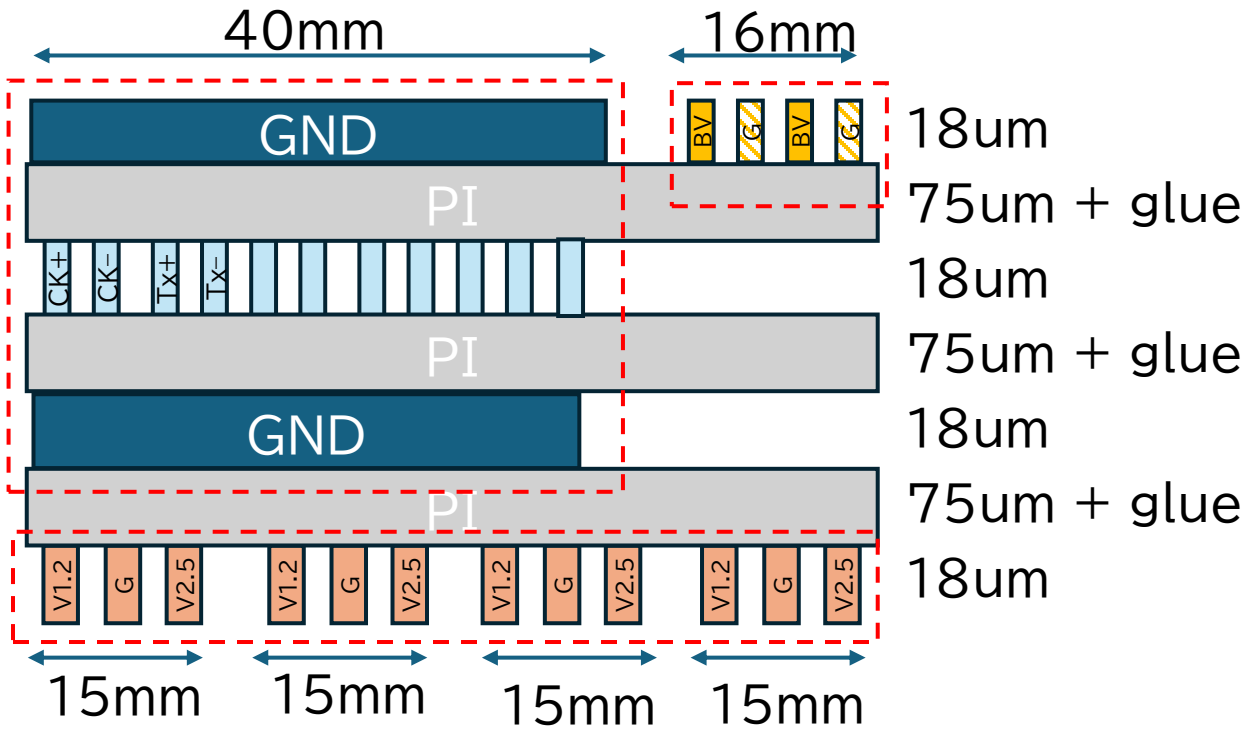
- Simulation for signal Integrity

# Power distributions

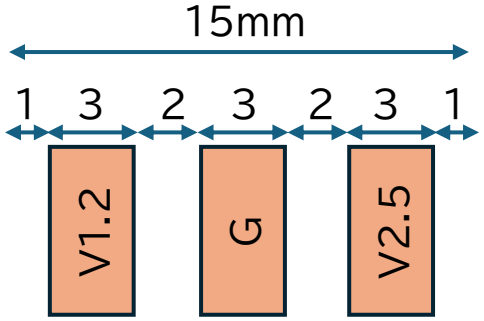



- 4 separate LV lines for a stave
  - Power lines are shared with 2 stavelets
  - Power consumption for ~4.8 W for 2 stavelets (single lines)
    - Assuming 600 mW/ASIC (128ch) -> 4 ASIC/stavelet x 2 slavelets = 4.8W
- Bias voltage lines for each stavelet?
  - If so, 8 BV lines -> 16mm width needed
    - Line&Space = 500um+500um
- Signal Lines = 160 ~ 220 (70umx70um Line&Space) = 21 ~ 31mm

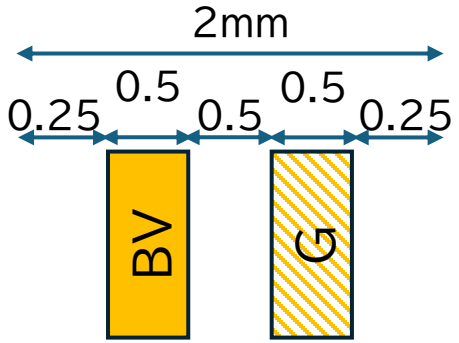
# Layer Structure




LV for a stavelet

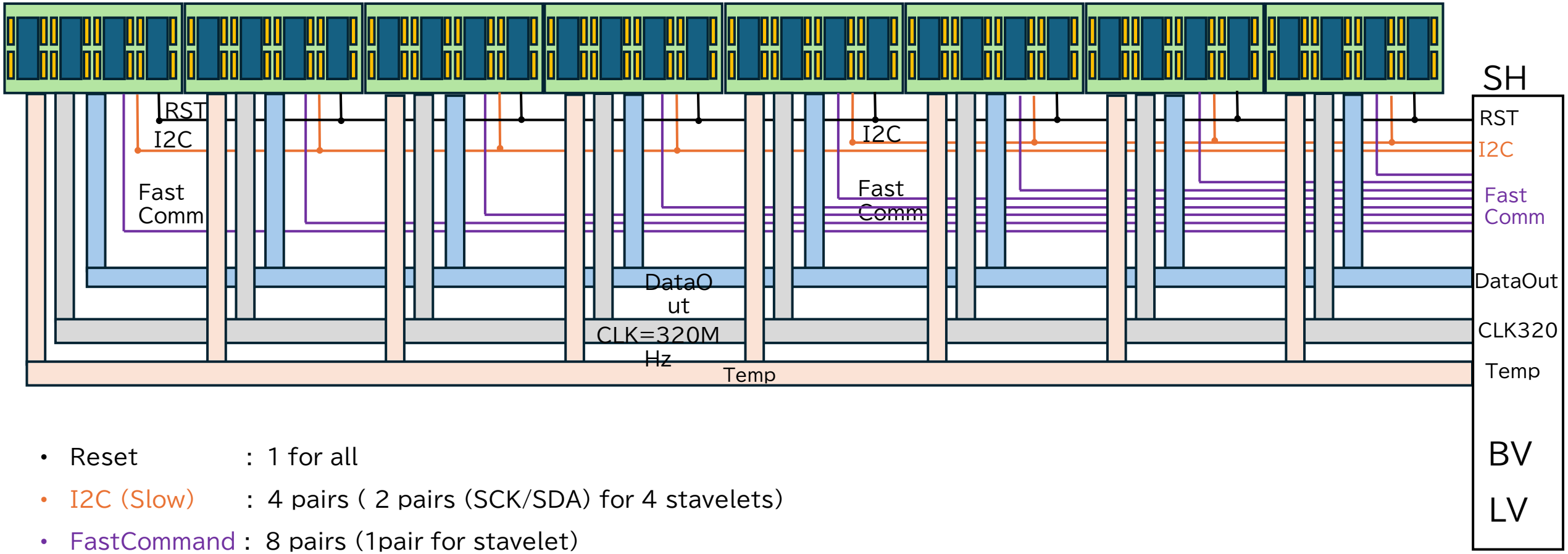



BV for a stavelet




- 4 Cu layers for a FPC
  - 1st Layer: GND + HV(+GND)
  - 2nd Ly: Signal,
  - 3rd Ly : Signal GND
  - 4th Ly : LV Power (1.2V and 2.5V)
- Cu thickness:18um
- Line & Space
  - Signal : 70&70 um
  - HV + GND:  1mm & 1mm = 18mm
  - LV + GND:  3mm & 2 mm

# Signal Line Routing




- Reset : 1 for all
- I2C (Slow) : 4 pairs ( 2 pairs (SCK/SDA) for 4 stavelets)
- FastCommand : 8 pairs (1pair for stavelet)
- DataOut : 32 pairs (320Mbps)
- CLK320 : 32 pairs (320MHz)
- Temperature : 32 pairs ?

# Signal Lines = 108 Pairs + 1
= 217 lines → 31mm width

More realistic design is on-going

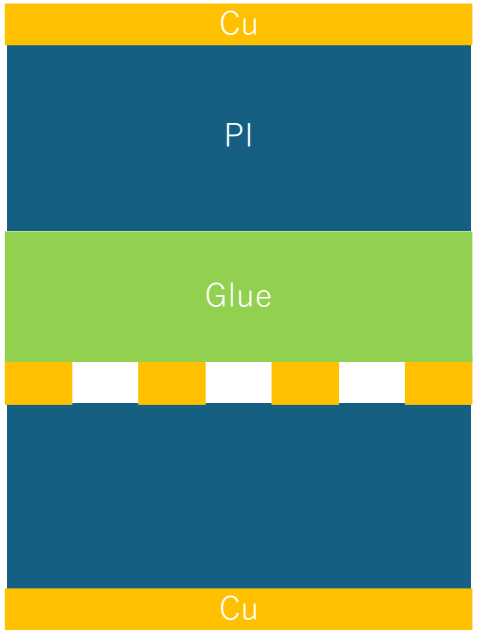
# Signal simulation for long FPC

- Clock/signal  integrity is most important for TOF

- What we verify through the simulation
  - Impedance with 70um/70um L & S
    - Zdiff = 98 ohm
  - Eye-diagram
    - Jitter could be estimated
  - S-parameter
    - Reduction, reflection、
    - Cross-talk to/from neighboring line
- We could successfully procure the appropriate FPC material in Japan
  - Panasonic R-F775 :  Cu: 18um,  PI : 75um thick

- 1st  FPC simulation with a simple assumption
  - Streight line with 135cm long
  - Designed Layer structure and line/space

Strip line structure
(Covered by top and bottom




R-F755:  PI:75um,  Cu: 18um
PI er = 3.2

Glue sheet：YBL-000-OL、50um
er=2.5

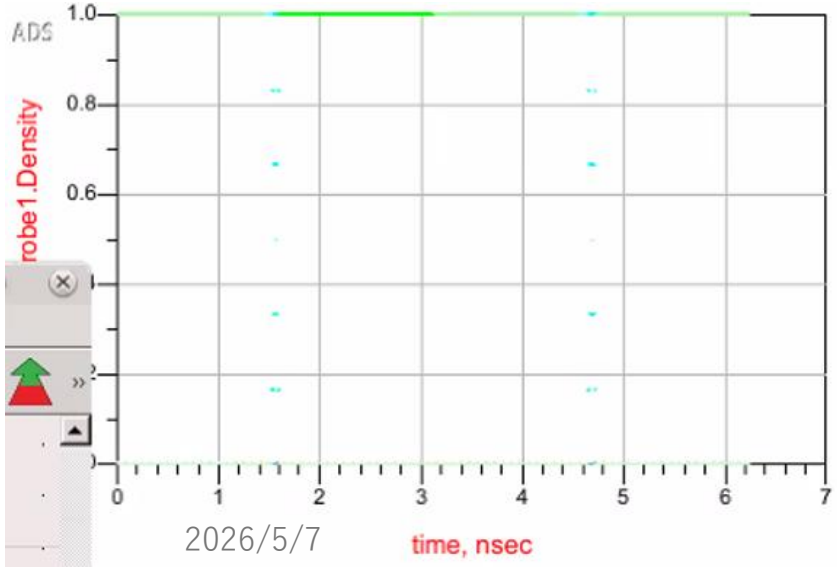
R-F755:  PI:75um,  Cu: 18um

Line width：70um, space btw lines：70um

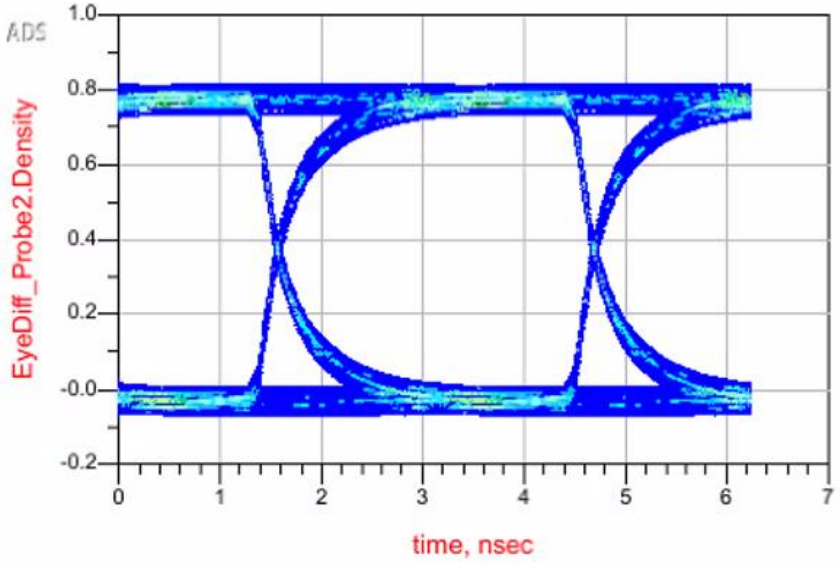
# Simulation results

- 1st version SIM done with very simple assumption
  - EM simulation of FPC
- Input: Left
  - 3.125ns pulse (= 320Mbps) with 20ps rise time
  - Random pattern and Clock pattern tested
- Output :
  - Middle:  Random bit pattern
  - Right  : Clock pattern
- Jitter (right)
  - Jitter is width at the crossing of the pulse
  - Looks small for the clock pattern.
  - Extracting the jitter quantitatively

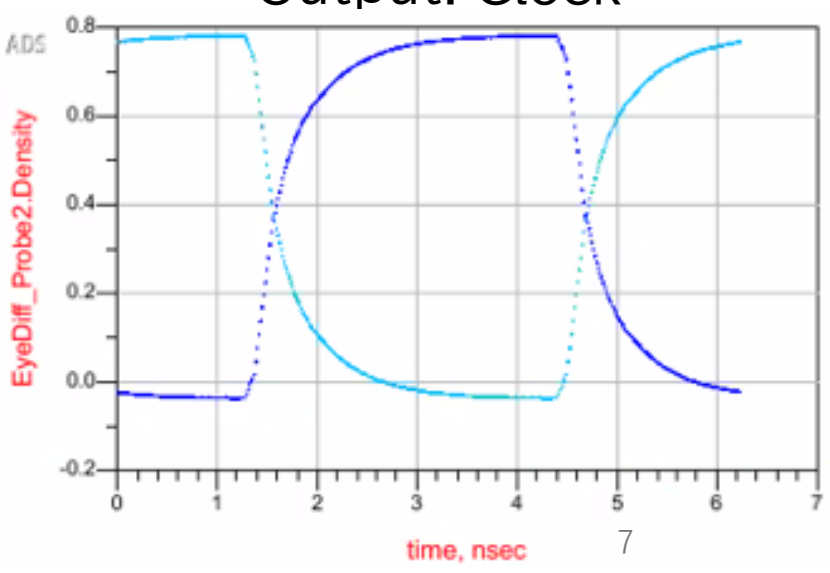
Input




Output: Random

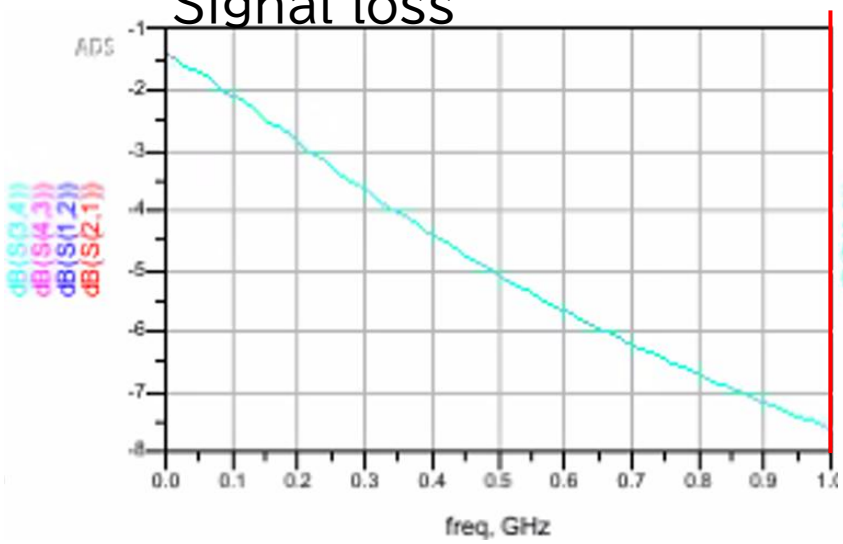



Output: Clock

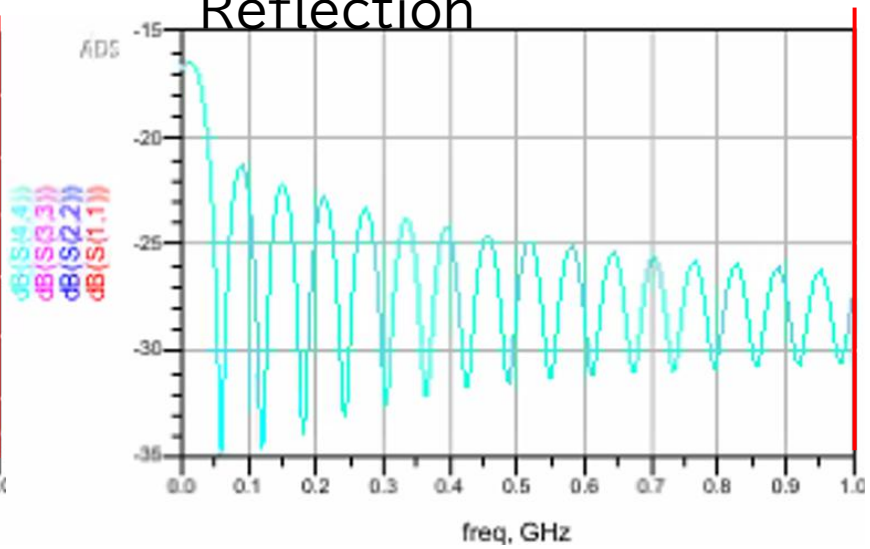


# Signal loss and reflection

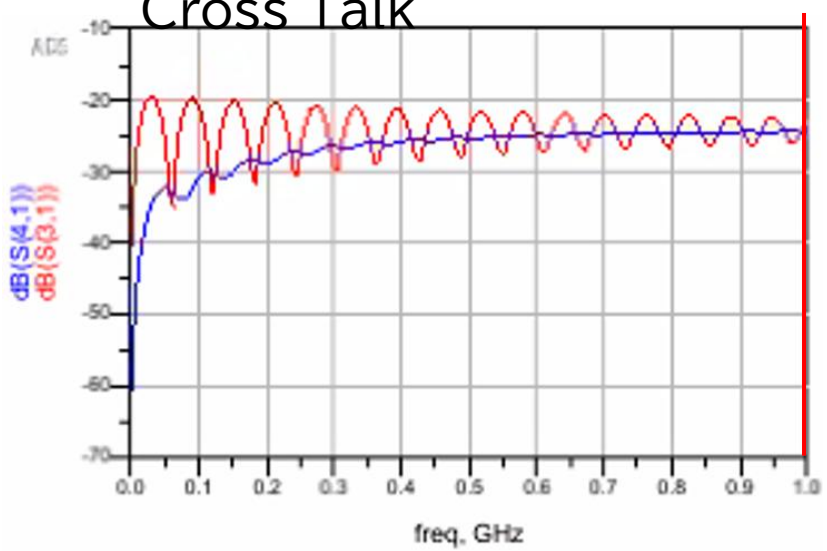
Signal loss




Reflection




Cross Talk




- Evaluate the distortion at 0.8~1GHz (2.5 x reference freq. (320MHz))
  - Signal loss : -7.5 dB = 42%
  - Reflection : -28 dB = 4%
  - CrossTalk : -25 dB = 6%
- These values are good enough for 320MHz clock
  - This is ideal case (simple straight line), redo with the realistic condition
  - lpGBT can use “pre-emphasis” which help the pulse shape
  - Need the driver characteristics of the FCFD driver

Pre-emphasis of lpGBT

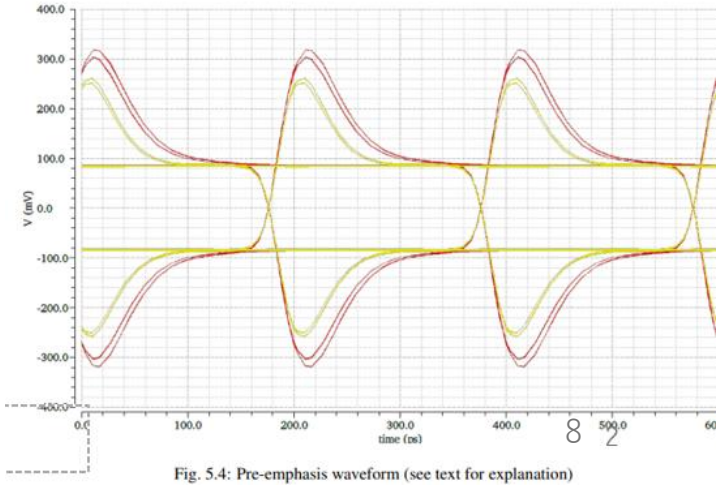



Fig. 5.4: Pre-emphasis waveform (see text for explanation)

# Summary

- FPC design reconsidered
  - 70/70um line & space
  - 4 LV lines & 8 HV lines
  - Signal lines with the stripline structure

- Ideal simulation performed for 135cm FPC
  - signal loss → 42%,  reflection → 4%, crosstalk → 6%
  - Pre-emphasis can help the signal transmission

- Next step
  - Redo with the realistic configuration
    - Signal transmissions with the BUS structure
      - Reflections might have a bigger effect
    - Need the driver info for the FCFD ROC