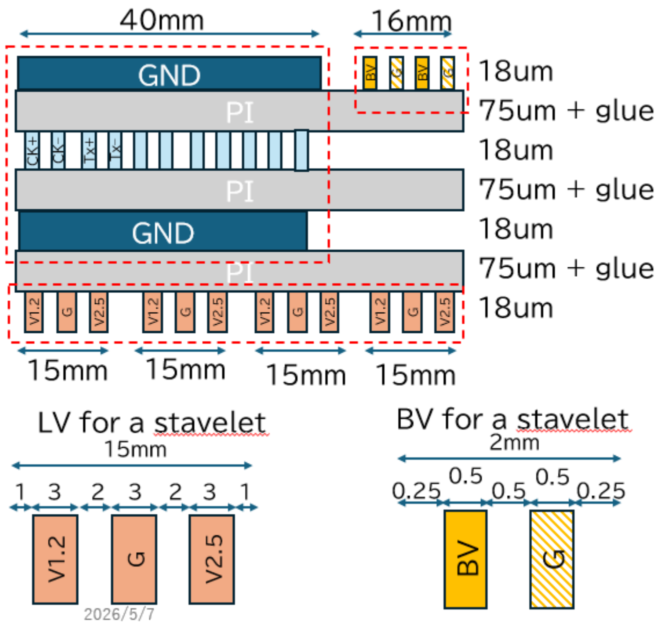
FPC documents

Takashi Hachiya
Nara Women's University

Introduction

- I showed FPC design last week and got useful feedback and comments.
  - Document, Wiring

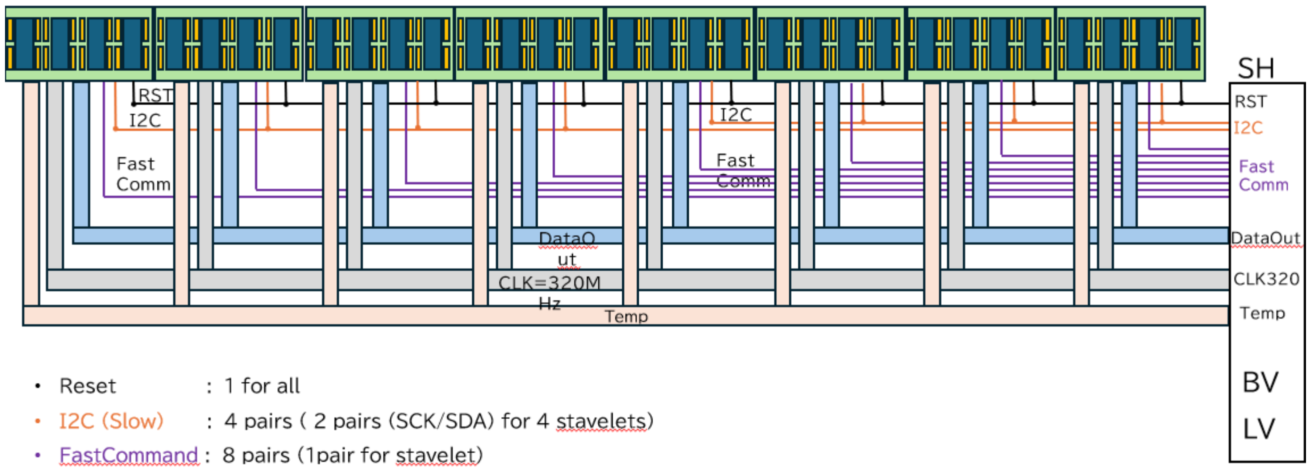
Layer Structure



- 4 Cu layers for a FPC
  - 1st Layer: GND + HV(+GND)
  - 2nd Ly: Signal,
  - 3rd Ly : Signal GND
  - 4th Ly : LV Power (1.2V and 2.5V)
- Cu thickness:18um
- Line & Space
  - Signal : 70&70 um
  - HV + GND: 1mm & 1mm = 18mm
  - LV + GND: 3mm & 2 mm

2026/5/7 4

Signal Line Routing



- Reset : 1 for all
- I2C (Slow) : 4 pairs (2 pairs (SCK/SDA) for 4 stavelets)
- FastCommand : 8 pairs (1pair for stavelet)
- DataOut : 32 pairs (320Mbps)
- CLK320 : 32 pairs (320MHz)
- Temperature : 32 pairs ?

Signal Lines = 108 Pairs + 1
= 217 lines → 31mm width

More realistic design is on-going

2026/5/7 9

Information Required for FPC Design

- The size of FPC is approximately **135 cm in length** and **6 cm in width**. To proceed with the design of the FPC for the EPIC TOF detector, it is necessary to define the communication specifications, power distribution, connection methods, and mechanical constraints in advance. In particular, the design must consider high-speed signal integrity, low material budget, and the effects of voltage drop and noise in long flexible cables.

1. Communication Specifications

- The communication architecture between the ASICs and the FPC must be clarified.
- The following signals are currently assumed:
  - CLK (Differential, 320MHz)
  - DataOut (Differential 320Mbps)
  - FastComm (Differential 320Mbps)
  - I2C (CLK, SDA, single-end, 1Mbps)
  - Reset (Asynchronous)
- The design requires information on: Number of signal lines, Differential or single-ended signaling, Termination scheme , Data rates, ASIC I/O specifications. The total number of routing lines on the FPC will also depend on how signals are organized at the interposer side, such as bus sharing or daisy-chain configurations.
- Since the detector performance strongly depends on timing resolution, the clock quality is particularly important. The target clock jitter should be kept below approximately 10 ps.

2. Power Distribution

- The FPC must provide stable power delivery to both ASICs and sensors.
  - The ASICs require: 1.2 V, 2.5 V
  - the sensors require a high-voltage bias supply (BV).
- The following information is required for the power design:
  - Current consumption of each power rail
  - Allowable voltage drop (5% tolerance at ASIC)
  - Trace width and copper thickness
  - Power and GND distribution scheme
- Special attention is required for the relationship between signal return paths and power-ground structures. It is necessary to determine whether separate grounds are required for the 1.2 V and 2.5 V domains, and whether analog and digital grounds should be separated.

3. Temperature Measurement

- Since the performance of AC-LGAD sensors is sensitive to temperature, the temperature should be monitored with appropriate granularity.
- A thermistor (temperature sensor) may be attached to each AC-LGAD sensor for local temperature monitoring.

4. Connection Specifications

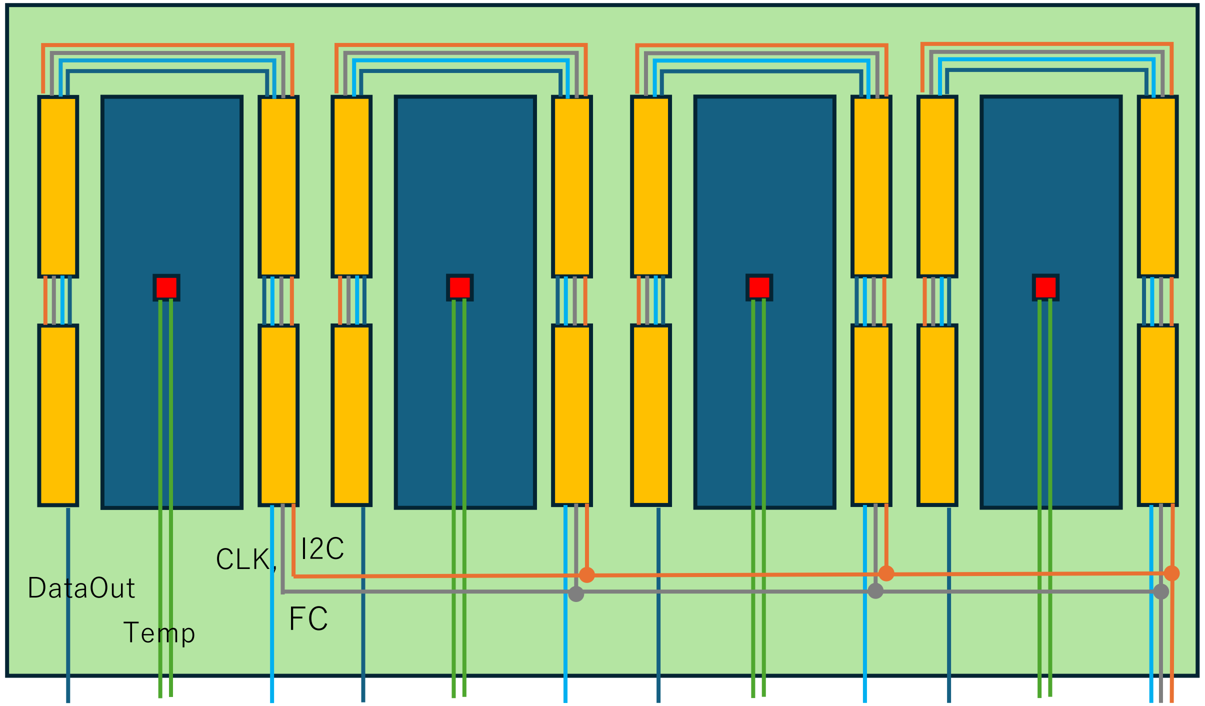
- The connection interfaces between the FPC and detector components must be defined.
- These include:
  - Interposer connection
    - Wire-bonding pad layout
  - Connection to the Service Hybrid (SH)
    - Connector specifications
- The connection locations and pitches strongly affect routing density and assembly feasibility and therefore should be defined early in the design phase.

- ### 5. Mechanical and Assembly Requirements

- Mechanical constraints and assembly conditions for the FPC must be specified.
- Major items include:
  - FPC dimensions
  - Layer stack-up
  - Flatness requirements
  - Assembly constraints
  - Radiation tolerance
  - Low material budget requirements
- Since minimizing the material budget is important for TOF detector performance, optimization of copper thickness, dielectric thickness, and GND structures is required.
- Link to document :

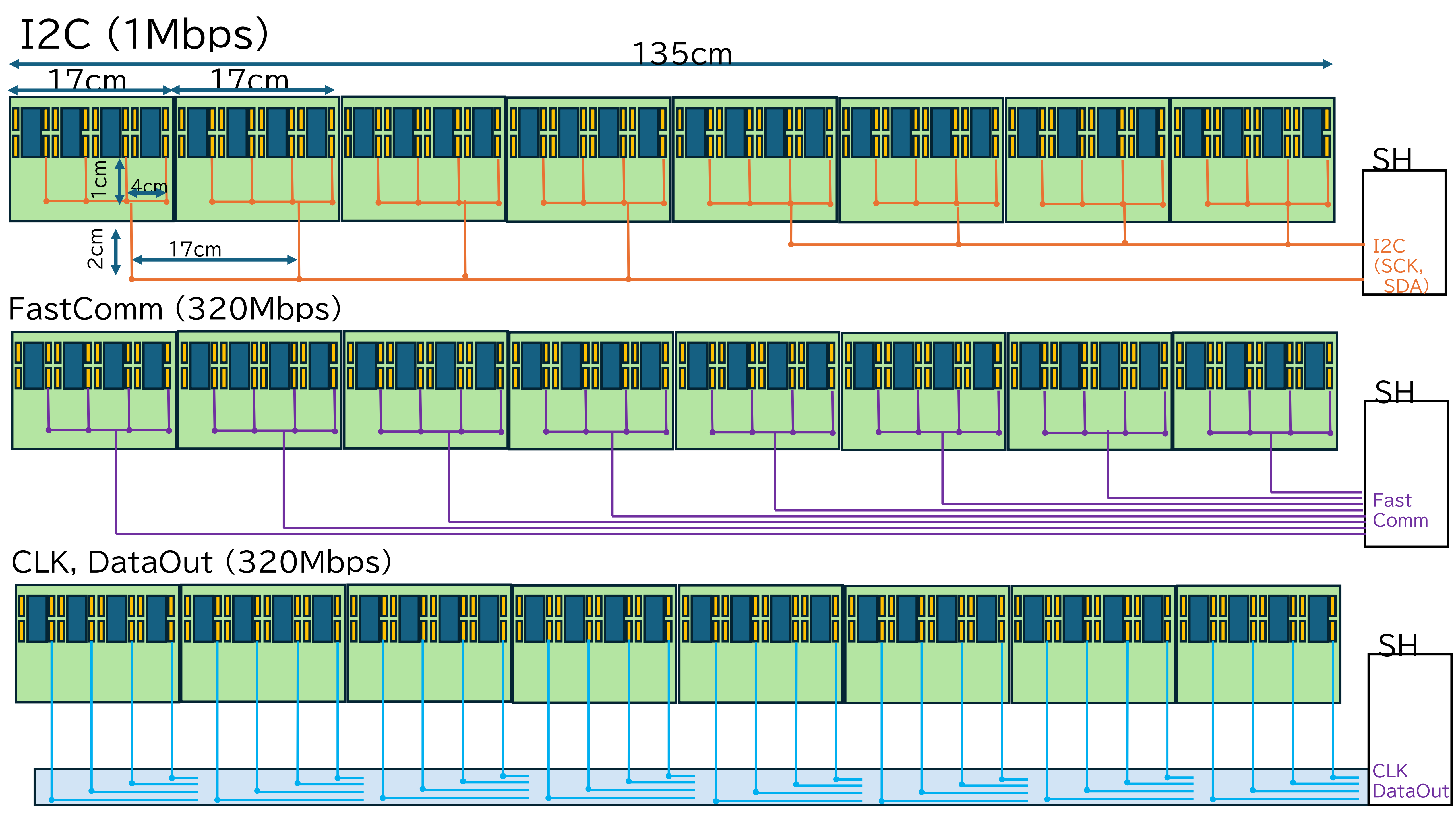
https://docs.google.com/document/d/1gJO5AsvFQypVvU2cHV11WHy5QTBQ1Opm3aAoIuFGR0E/edit?usp=sharing

Line routing in stavelet (I thought)



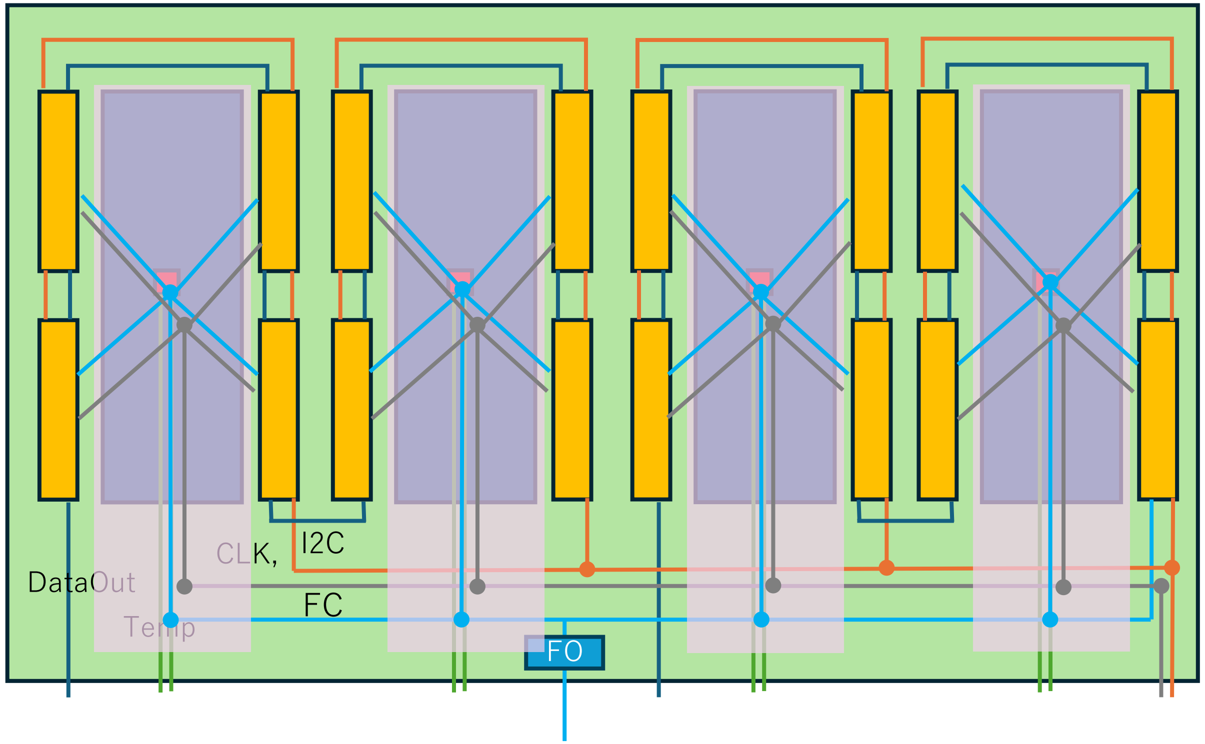
- Per ASIC (128ch =4 x 32ch FCFD connected)
  - CLK (320MHz)
  - DataOut (320Mbps)
- Per stavelet (share to 4 128ch-ASIC) – bus in IP
  - FastComm(FC, 320 Mbps)
- Per 4 stavelets : bus in IP
  - I2C (1Mbps)
- Per Sensor
  - Temperature monitor (by Thermistor?)

- Only wire bonding pads + passive devices (such as bypass capacitors and termination registers)
- No active device is mounted on interposer
  - No buffer, no fanout, no LDO to reduce extra parts and materials



I2C (1Mbps)
135cm
17cm
17cm
1cm
4cm
2cm
17cm
SH
I2C
(SCK,
SDA)
FastComm (320Mbps)
SH
Fast
Comm
CLK, DataOut (320Mbps)
SH
CLK
DataOut

Proposed idea by Artur

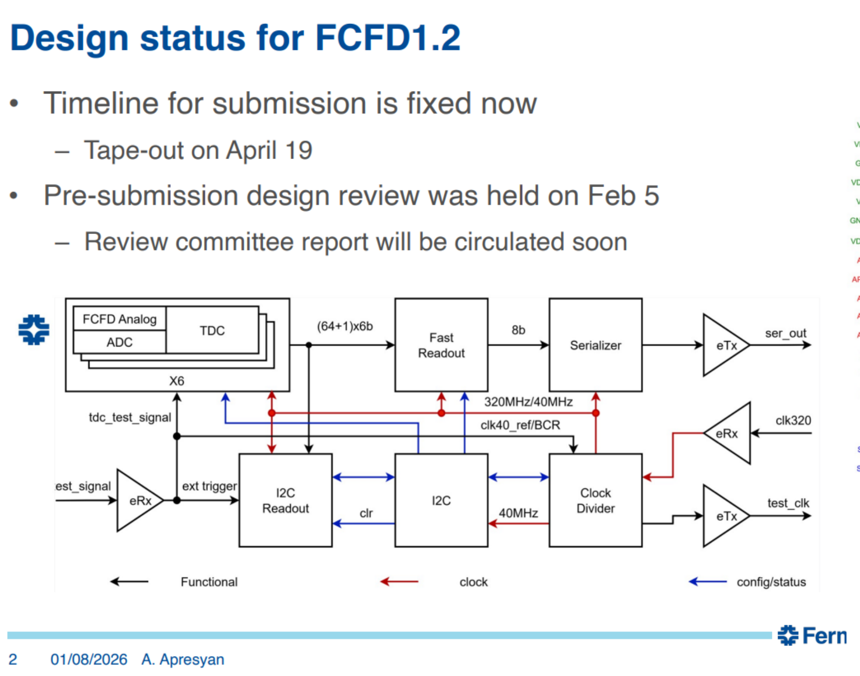


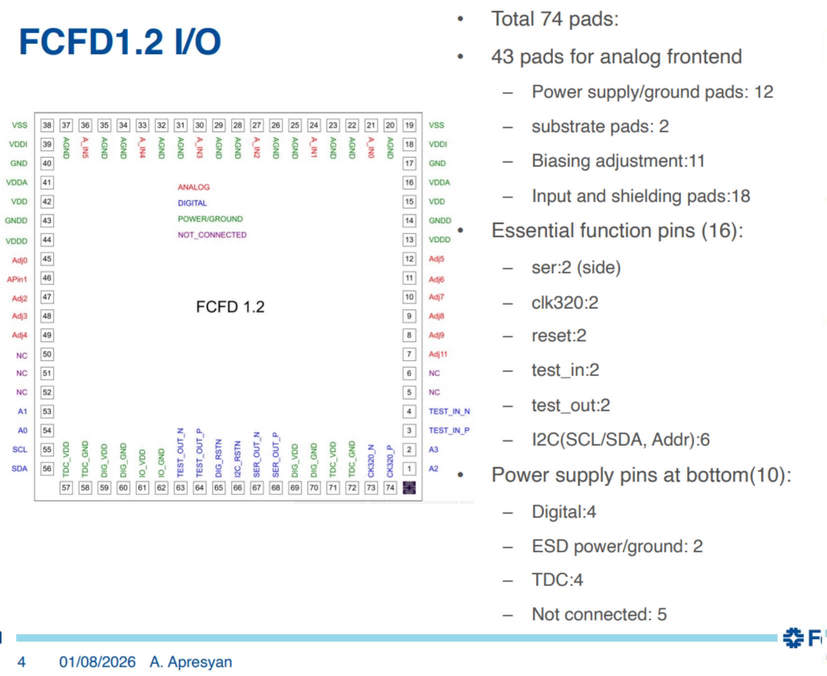
- In the FCFD architecture, we instead prefer:
  - one shared data port among **four** ASICs,
  - and a **multi-drop approach** for the clock input.

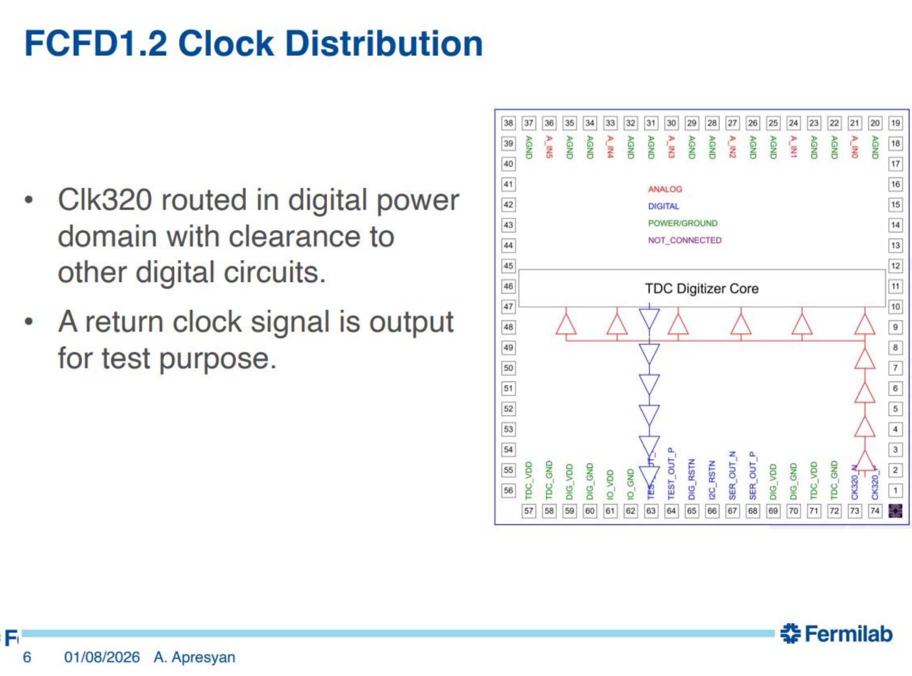
- The question regarding whether it is feasible to combine data outputs from 8 × 32-channel FCFD ASICs is therefore directly relevant to the intended architecture.

- To reduce clock/fast comm line in FPC
  - One clock input to stavelet and split by FanOut

- Good to discuss and test using the prototype
  - OK to mount extra active device ?



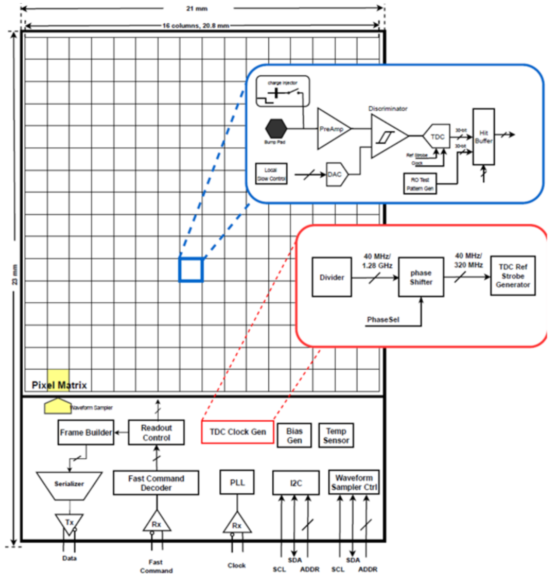


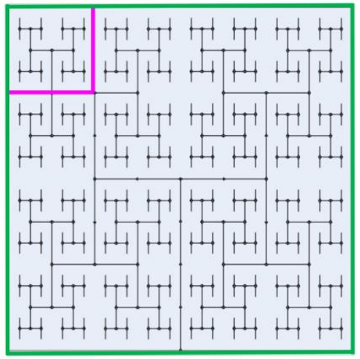


https://indico.bnl.gov/event/31523/contributions/119840/attachments/68729/118039/FCFD_status_02_2026.pdf

- FCFD ROC v1.2
  - Pin assignment found and two reset PIN (DIG-RSTN, I2C-RSTN). Two line needed?
  - No daisy chain in v1.2 ?
  - Not equal length wiring of the clock network

ETROC





- Dear Takashi,
- We discussed your presentation [1] with Sergey and Datao, and we have a few suggestions and comments, that I summarize below. As I mentioned today, it would be great to summarize the FPC requirements and specs into a document that is shared among various stakeholders, to make sure that all needs are summarized.
- The current FPC concept appears to assume that each 32-channel FCFD ASIC requires:
  - a dedicated clock input, and a dedicated data output.
- Under this assumption, a single lpGBT would not provide sufficient connectivity:
  - one lpGBT provides 32 clock outputs, but only 28 data inputs.
  - As currently envisioned, the data-port allocation is therefore not feasible.
- In the FCFD architecture, we instead prefer:
  - one shared data port among **four** ASICs,
  - and a **multi-drop approach** for the clock input.
  - Both approaches can be evaluated with the FCFD1.2 ASIC
- The proposed detector layout consists of:
  - 8 stavelets (Modules), each Module containing 4 sets of:
    - 2 × 64-strip sensors, and
    - 4 × 32-channel FCFD ASICs.

Same with my thought

- This architecture already implicitly assumes:
  - Multi-drop clock distribution, and shared/single data-channel operation.

each clock for a 128chASIC

- The question regarding whether it is feasible to combine data outputs from 8 × 32-channel FCFD ASICs is therefore directly relevant to the intended architecture.
  - From our perspective, this **should be feasible**.
- We suggest reducing the number of CLK lines to:
  - one clock line per stavelet/module,
  - followed by a local 1-to-4 fanout stage.

New idea

- The local clock fanout could be implemented using:
  - an active buffer, or
  - potentially a passive fanout approach, provided the transmitted clock amplitude is increased appropriately to preserve signal integrity.
- There is also one fast-command signal shared across the stavelet:
  - this implies that a multi-drop LVDS signal would pass through 16 ASICs.

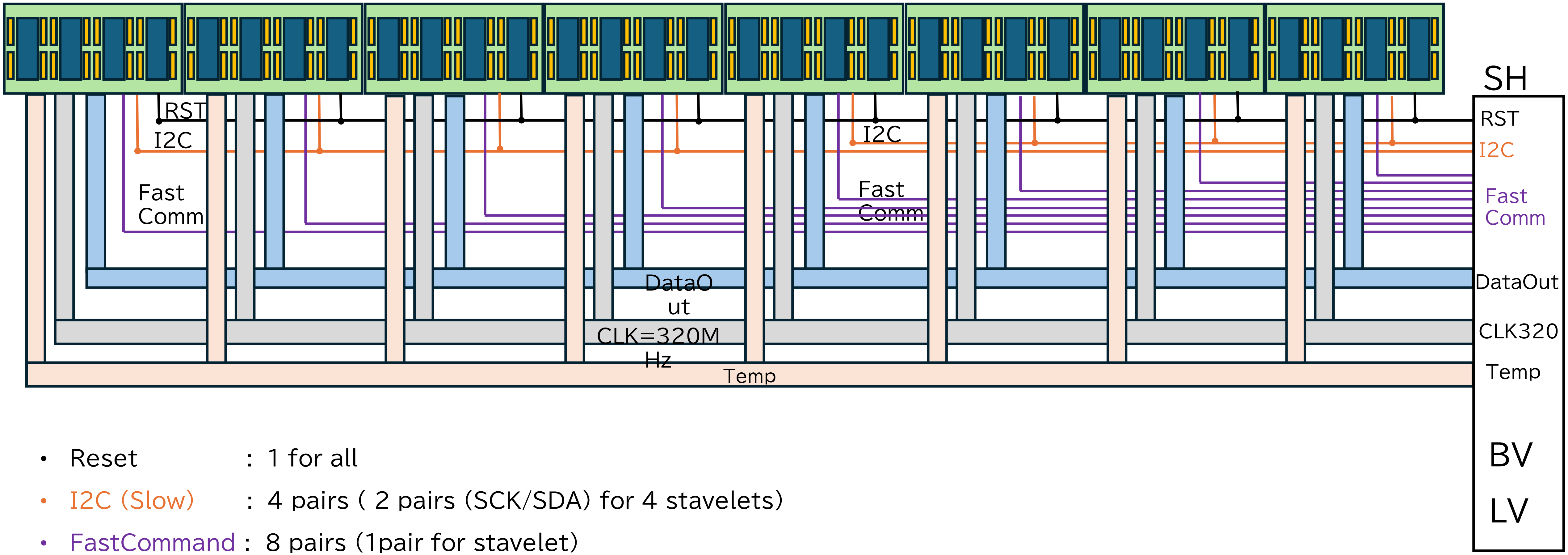
Same with our design

- Since one lpGBT provides 16 ePort Tx channels, it may be advantageous to:
  - use two fast-command lines per stavelet/module,
  - unless the remaining ePort Tx channels are needed elsewhere.

2 fast-comm per stavelet. New idea

- Even with a single fast-command line, we believe it should still be feasible to:
  - multi-drop one line across 16 FCFD ASICs,
  - using a serial-parallel distribution topology designed to spread reflections in time and preserve signal integrity.
- We are using the eTx module, which is effectively the same as the ePort TX implemented in the lpGBT.
  - The lpGBT documentation can therefore be used as a reference for the driver characteristics.
- I am also attaching the power consumption estimate for a 32-channel FCFD chip below, someone asked for it in today's meeting.

Signal Line Routing



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