

FCFD Variant Update

ASIC Monthly Update

2026-06-04

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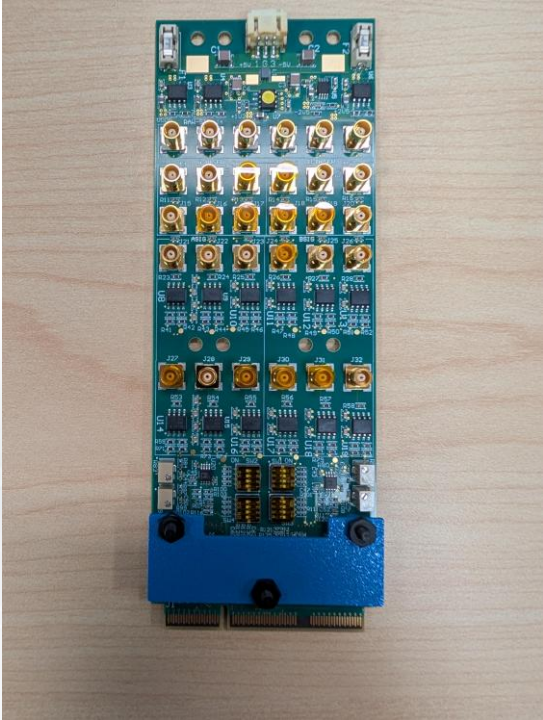


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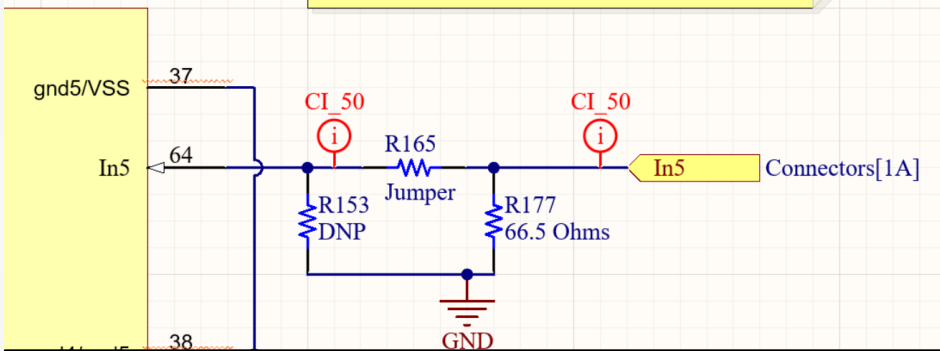


FCFD Front End Board Status

- All 6 boards are wirebonded as of late May
 - 1-2 boards with Alexander at CERN
 - 1 board at JLab
 - Remaining boards at BNL
- Assembly issues
 - Wrong power IC – 2.5V regulators populated with wrong part
 - Impedance matching
 - Issue: The boards would not detect any charge with the termination resistors installed, but upon removal the chip worked as expected
 - The termination resistors on each FCFD input are directly ground referenced
 - The FCFD inputs are DC biased, and most likely the resistors are impacting this bias
 - Solution: Need AC termination to prevent reflections if they appear as an issue during testing
 - Unused inputs on the FEB were not grounded
 - Design mistake
 - Required creative grounding to prevent charge buildup on ungrounded pads
 - HRPPDs at CERN – sensors were shipped to CERN for beam testing



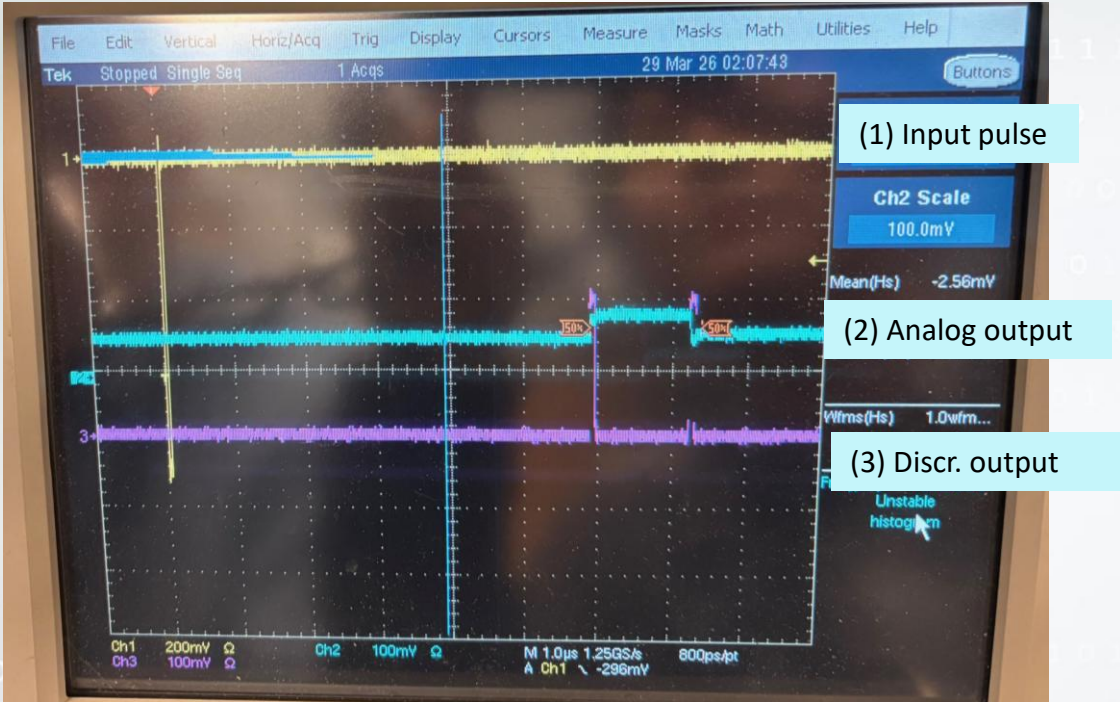
FCFD Variant FEB



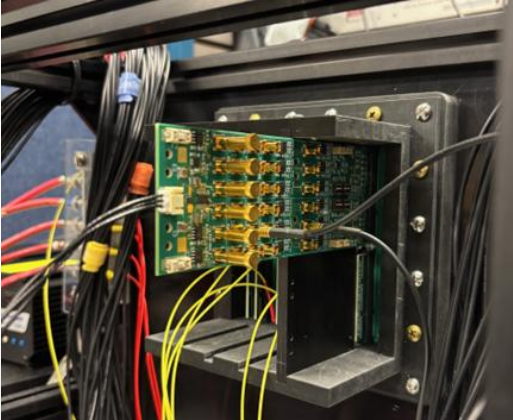
Termination resistor

Current testing status

- Initial outputs from FCFD looked OK, although timing may be off due to the test setup
- BNL was able to run 1 test of the discriminator before packing up HRPPDs on May 8
- Testing will not resume until July
- BNL/JLab will perform charge injection testing while waiting for HRPPDs once boards complete



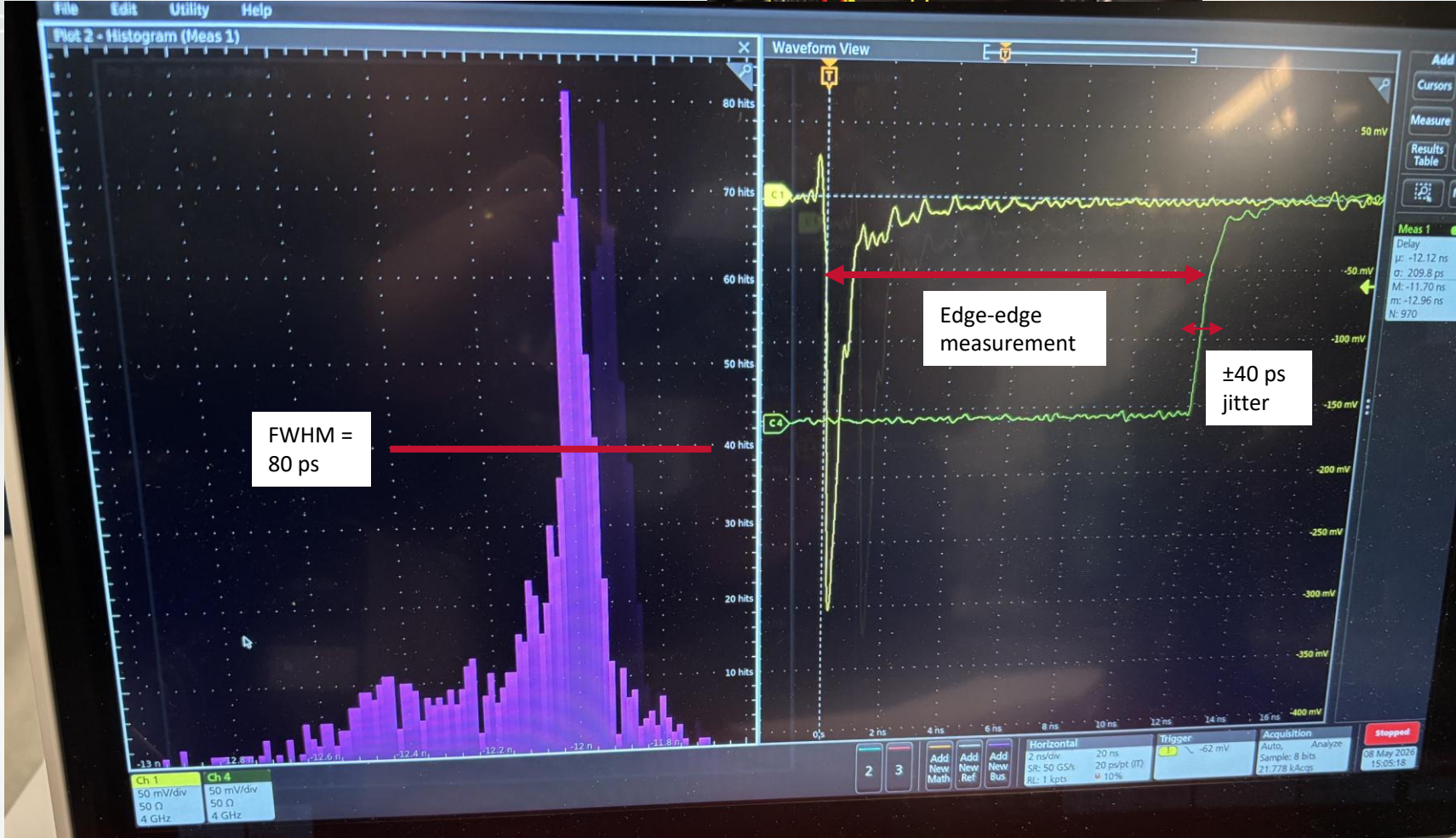
Laser Testing with HRPPD



- Test setup:
 - Yellow is photodiode measurement split from laser
 - Green is CFD output of ASIC
 - Histogram records response time difference of photodiode from CFD
 - ~20k events recorded
 - Laser was not exactly centered on pixel, diffused over area - Lead and tail ends could be small signals, noise, dark pulses

Results

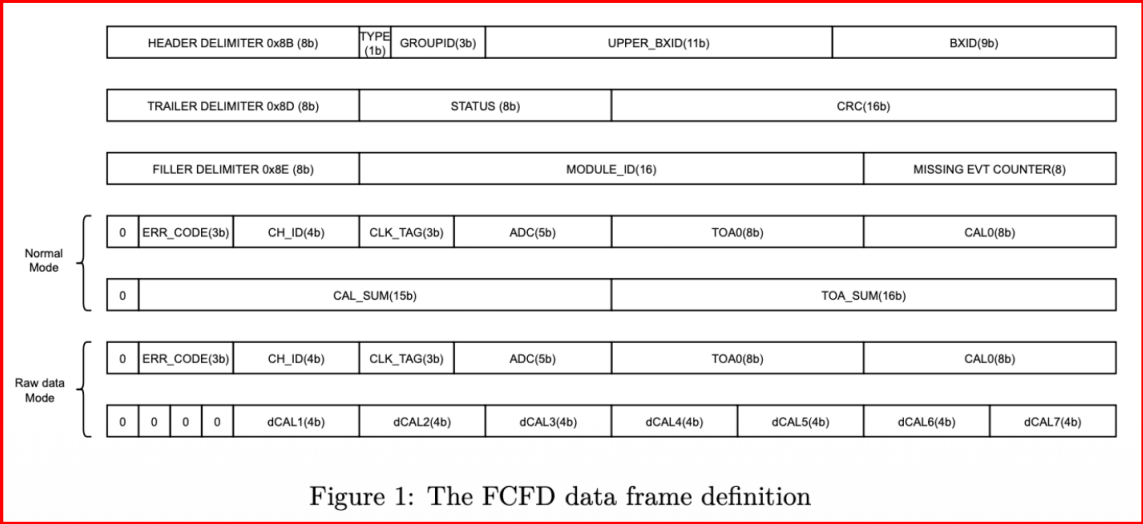
- FWHM = 80 ps
 - 6 bins above line
 - Each bin is 13.3 ps, 3 bins per division
 - Each division is 40 ps
 - Std dev = ± 35 ps
- Seems promising as a first run but obviously much **more testing is required**
 - Need to assess gain and noise impacts



Data format and rate from 32ch-FCFD

- My previous estimate: 12bit/hit
 - 5 bit ADC + 5 bit TDC + 20% header
- (semi-)official number: 160 bits/hit (max)
 - 5 bit ADC + 8bit TDC + other info = 64 bits/ch
 - Header(H) + trailer(T) + filler (F) = 96 bits/ch
 - H+T+F may be merged for channels hit at same time.
- Number is consistent with statement also presented.
 - $130\text{kbps} / (30[\text{Hz}] * 32 [\text{ch}]) = \sim 135 \text{ bits}$
- Using Brian's average hit rate, it means:
 - 200Mbps per HRPPD, 13.3Gbps from pFRICH as whole.
 - Will need at least two sets of lpGBT+VTRX+.
 - Max rate from a pad is 20kHz \rightarrow 3.2Mbps/pad \rightarrow 102Mbps/32ch.
 - It still fits to FCFD data bandwidth of 320Mbps/chip
- Power estimate won't change.
- To be checked: Can the FCFD analog part handle 20KHz pulse rate? They assume 100Hz per channel...

Data format was presented for the first time.



• Assuming a hit rate of 30 Hz, the raw data rate per chip is approximately 130 kbps, which is far below the 320 Mbps bandwidth of a single ELink.

Bandwidth of lpGBT + VTRX+ with FEC10 encoding is 7.68Gbps. (10.24Gbps mode)

Next Steps

- Timing testing will resume in July
 - Continuing to vary gain and other parameters
 - While waiting, charge injection test board will be used to measure parameters once manufactured
- Wish list so far
 - Increase dynamic range
 - Input protection from overcharge
 - Alternate packaging and assembly to wirebonding
 - pfRICH - ~2200 units, hpDIRC - ~2300 units
 - Potentially shift input impedance profile
- Meet with FNAL group for initial feedback

QUESTIONS?

Appendix

hpDIRC

- Signals are mostly one or two photon
- Signals on detector may vary due to gain variations and non-uniformity of the PMT

- Two groups of signals
 1. Single photons for Cherenkov ring imaging from aerogel
 2. Cherenkov hits from direct hits in the PMT window
- For category 1:
 - Single photon per pad: signal in ~ 10 pads per event per particle
 - Resolution about 30-40 ps for single photons
 - Gain may be 10^5 or 10^6 , still need to be determined (Once the gain is selected, it will be the same for all devices)
 - The readout chip needs to handle gain variations of $\sim x2-3$ due to MCP and field variations
- For category 2:
 - Localized within ~ 10 pads
 - Some pads will see signal an order of magnitude higher than Category 1

Specifications for pfRICH and hpDIRC

Detector	Channel Capacitance	Channel Rate	Time Resolution	Time Measurement Dynamic Range	Charge Measurement Dynamic Range	Charge Measurement Resolution
pfRICH	~10 pF	~10 kHz	~40 ps @ 100 fC	100-1,200 fC	100-10,000 fC	TBD
hpDIRC	~10 pF	~10 kHz	~40 ps @ 100 fC	100-1,200 fC	100-1,200 fC	TBD

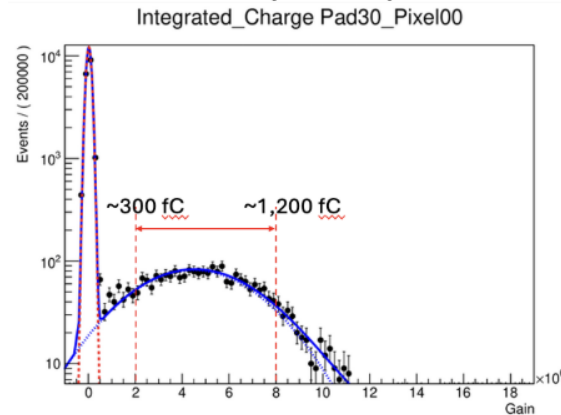
- Assumptions that went into this table
 - Gain of 10^5 corresponds to 16 fC
 - pfRICH region of operation defined with RED arrow below.
 - Low end of 100 fC to account for **x3** gain variations
- We circulated the above proposal to the detector experts
 - Next steps would be to test with the upcoming prototypes and see how well the CFD approach works for these detectors
 - Modified version will be needed to accommodate for MCP signals

Requirements/Specifications – 21 April 2025

ROC Specifications for pfRICH and hpDIRC

Detector	Channel Capacitance	Channel Rate	Time Resolution	Time Measurement Dynamic Range	Charge Measurement Dynamic Range	Charge Measurement Resolution
<u>pfRICH</u>	~10 pF	~10 kHz	~40 ps @ 100 fC	100-1,200 fC	100-10,000 fC	TBD
<u>hpDIRC</u>	~10 pF	~10 kHz	~40 ps @ 100 fC	100-1,200 fC	100-1,200 fC	TBD

- Assumptions that went into this table
 - Gain of 10^5 corresponds to 16fC
 - pfRICH region of operation defined with RED arrow below.
 - Low end of 100 fC to account for **x3** gain variations from Alexander statement that *“Gain will vary by a factor of 2-3 from pixel to pixel”*



- Latest - From meeting on 11 April 2025 with pfRICH and hpDIRC.