

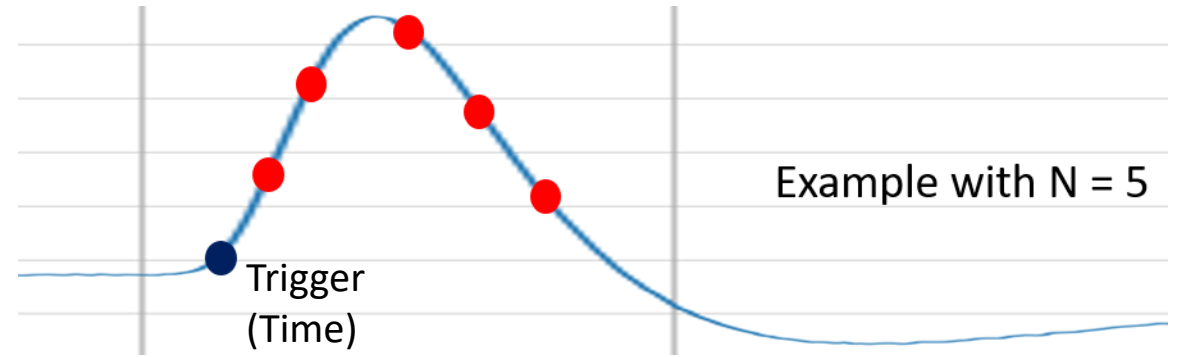
## CALOROC status

June 2026

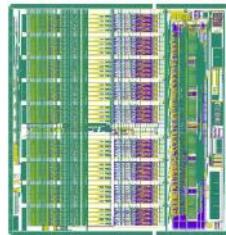
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Ecole Polytechnique – CNRS

## ❑ CALOROC main changes:

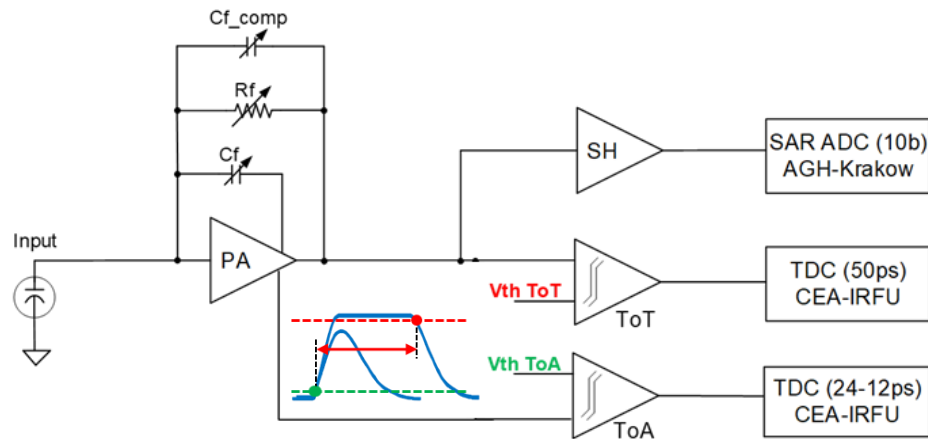
- ❑ Released in 2 versions: CALOROC-A and CALOROC-B
- ❑ New 6-layer substrate – BGA (common)
- ❑ New digital processing (common)
- ❑ New testboards (common)



**CALOROC 1A**  
CMS front-end  
Low SiPM capacitance



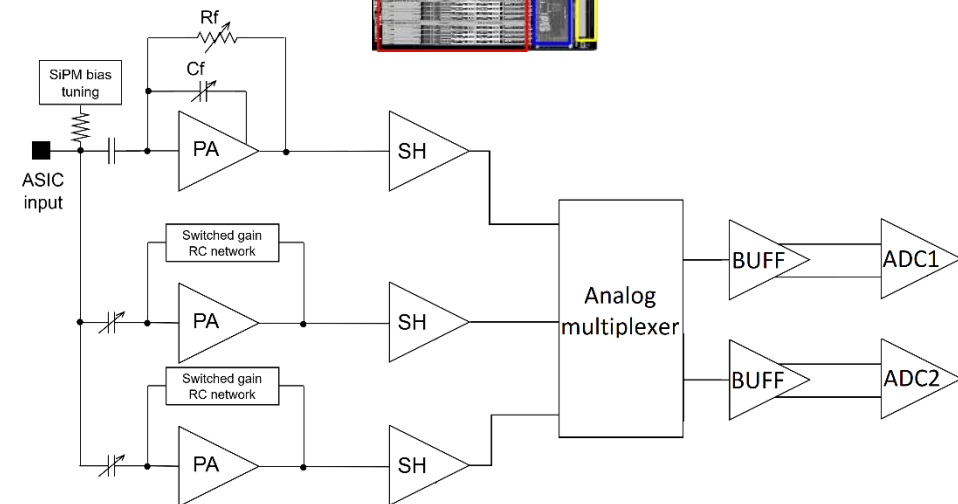
Measurements possible



**CALOROC 1B**  
New switched-gain front-end  
High SiPM capacitance



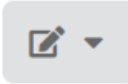
Measurements in progress




- Added documentation related to questions asked
  - Datasheet, waveforms, serial tests statistics


## Presentation of CALOROC

🕒 50m





**Orateurs:** El Berni Mowafak (OMEGA In2P3), Frederic Dulucq (OMEGA - Ecole Polytechnique - CNRS/IN2P3)

 CALOROC1B\_datas...

 Dumas\_2025\_J.\_Ins...

 FD\_260513\_CALOR...

 FD\_260513\_CALOR...

 FD\_Waveform\_only\_...



May 13: datasheet caloroc-b added (v1.3)



Updated slides with some answer to comments:

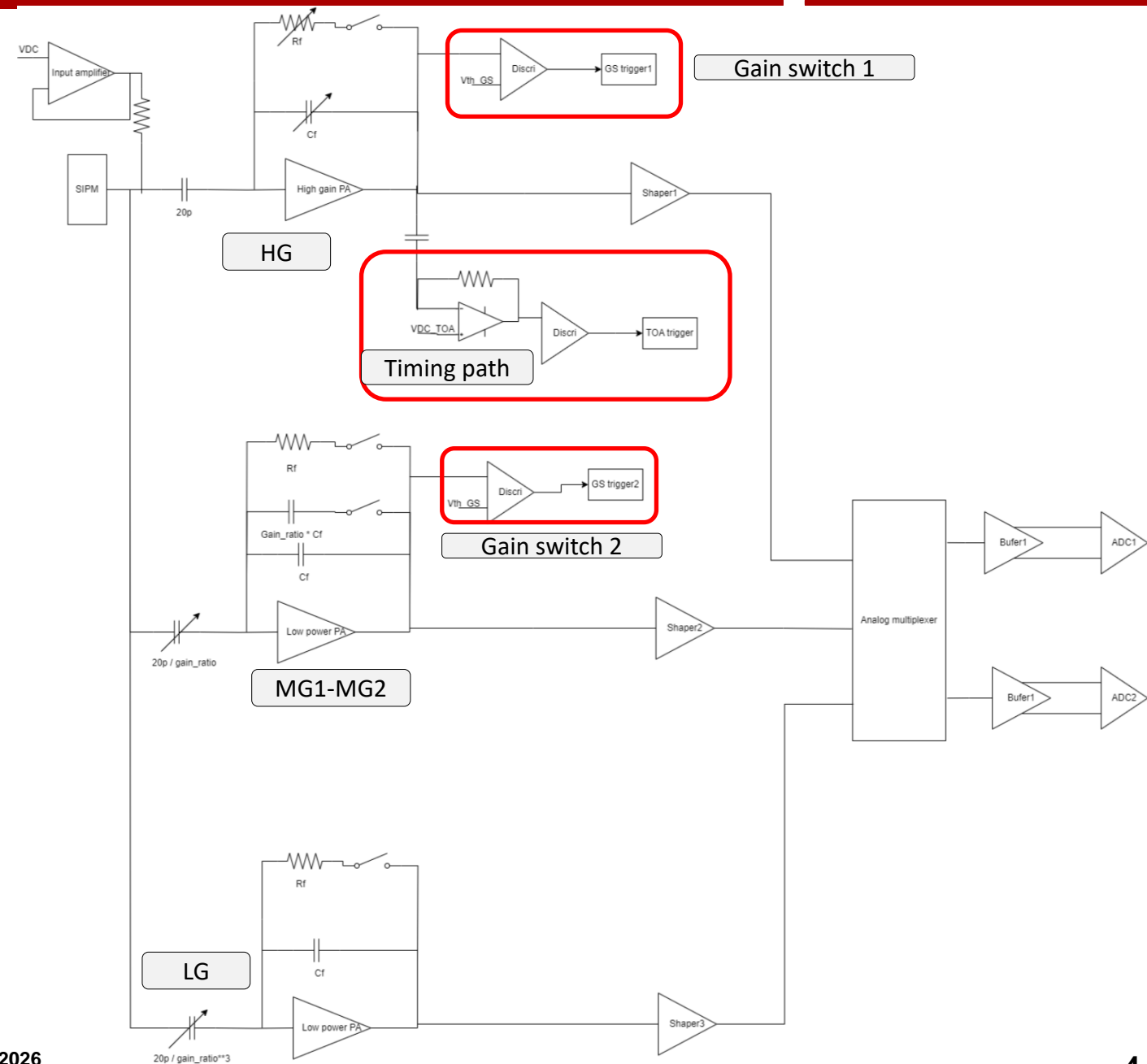
May 21: added in backup slide (#27) the gain switching mechanism

May 26: added twepp conference paper for the time to baseline information (related to hit rate and waveforms)

May 27: added in backup slide (#28) robot testing statistics + failing nature

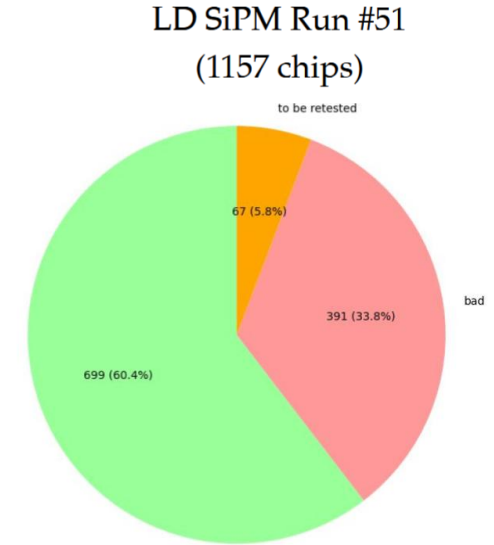
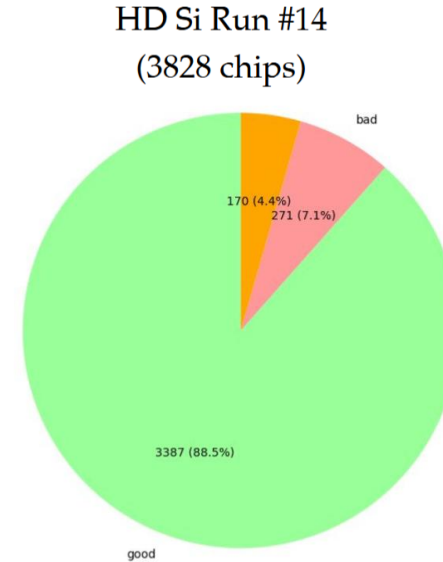
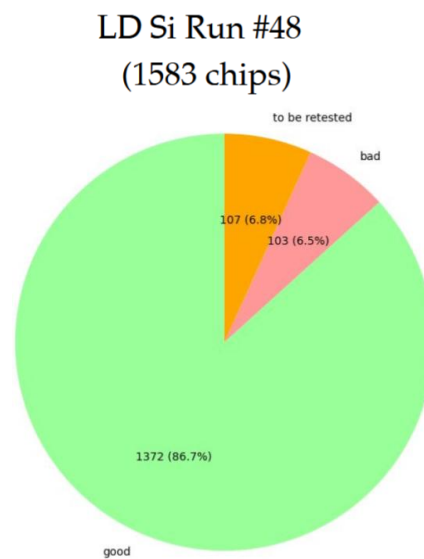
June 2: added slides with waveforms at the ADC input (different charges + gain switching activated)

- ❑ Switched gain mechanism based on:
  - ❑ 1 High-gain preamp also connected to timing path (top)
  - ❑ 2 switched-gain preamp (middle)
  - ❑ 1 low-gain preamp (bottom)
  
- ❑ Switching is based on 2 discriminators:
  - ❑ Latched outputs gives the overall gain active
    - ❑ 00 high gain
    - ❑ 01 medium gain 1 (before switching)
    - ❑ 10 medium gain 2 (after switching)
    - ❑ 11 low gain
  
- ❑ Automatic reset is done after 75-100 ns after first comparator fired



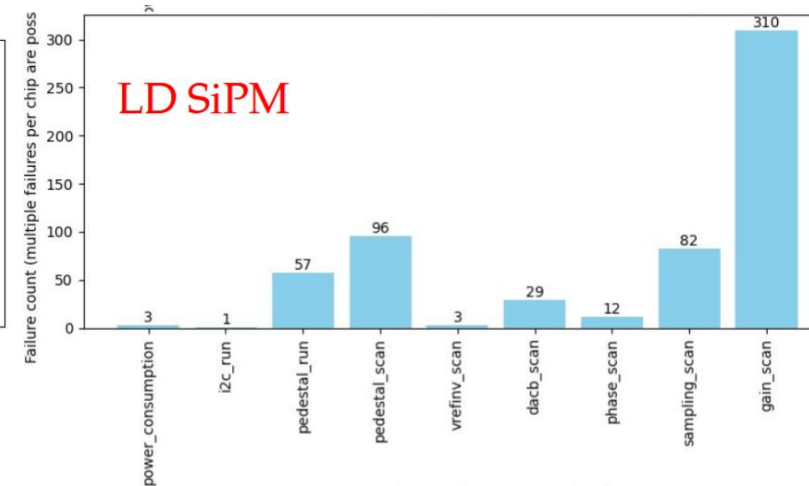
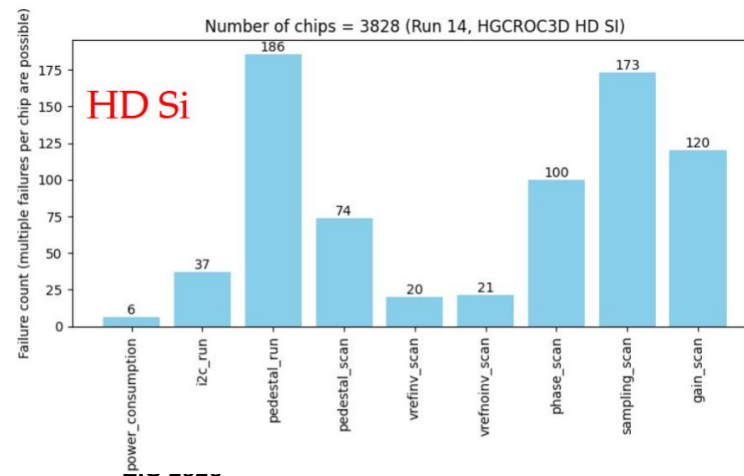
## Statistical analysis (LLR):

- HGCROC yield > 85%
- H2GCROC yield > 60%
- Expected value for CALOROC-A



## Nature of failing tests (LLR):

- Pedestal run (check ADC pedestal and noise)
- Sampling scan (check ADC and TDC shapes)
- Gain scan (check dynamic range / linearity)
- SiPM fails mostly due to the gain scan
  - threshold tuning ?

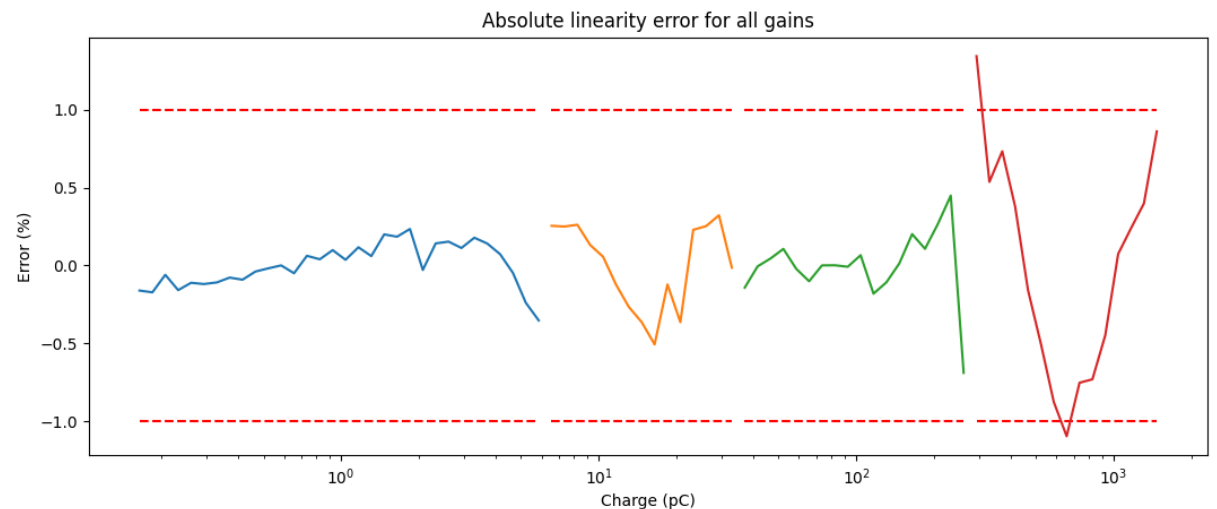
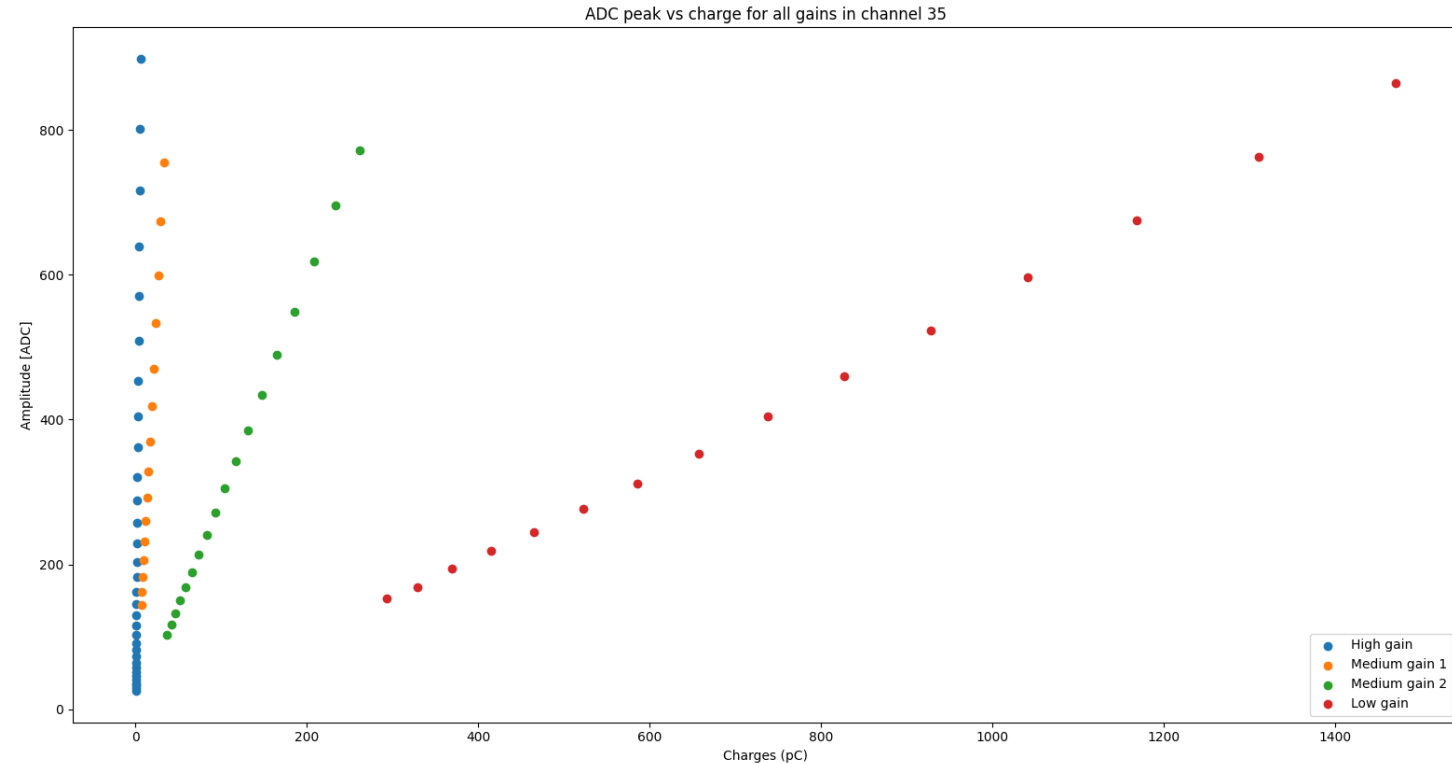


## External charge injection setup:

- 2.2nF detector capacitance
- 330pF injection capacitance
- Rise time: 2ns with a 8.25ns low pass filter

## Results:

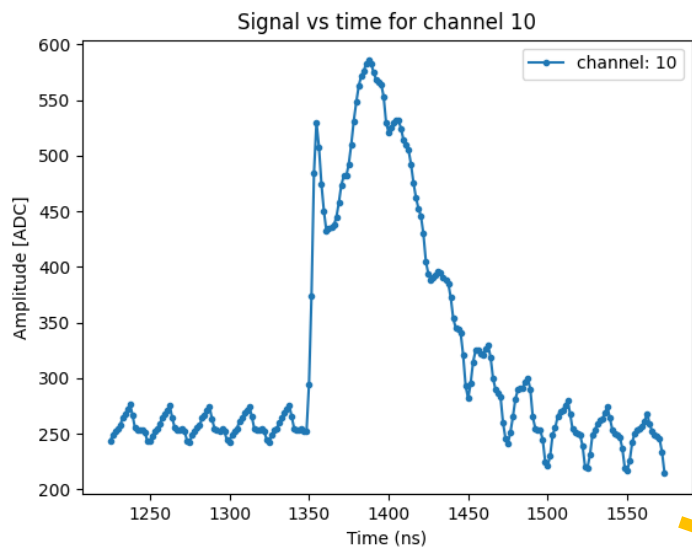
- Dynamic range of up to 1.47nC
- Linearity error of less than 1% for all gains except the low gain
- Linearity error close to 1% for the low gain



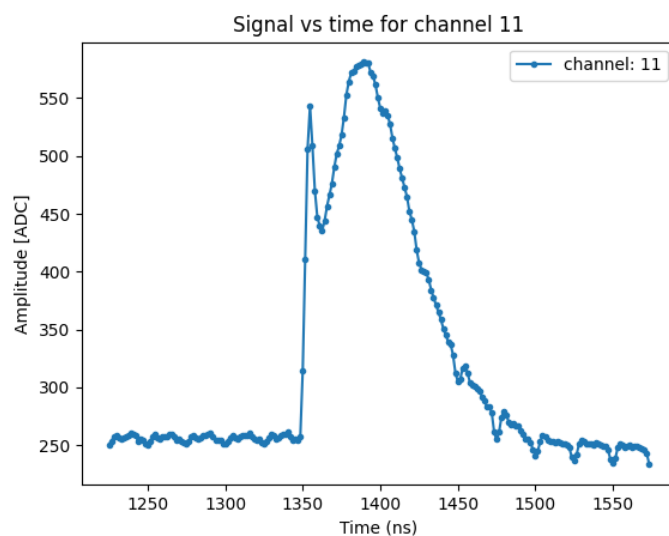
# Noise study (related to timing measurement)

- ❑ Noise versus testboard layout:
  - ❑ Strong dependency with layer used for routing
  - ❑ 3 different configurations for input signals (PCB layout)

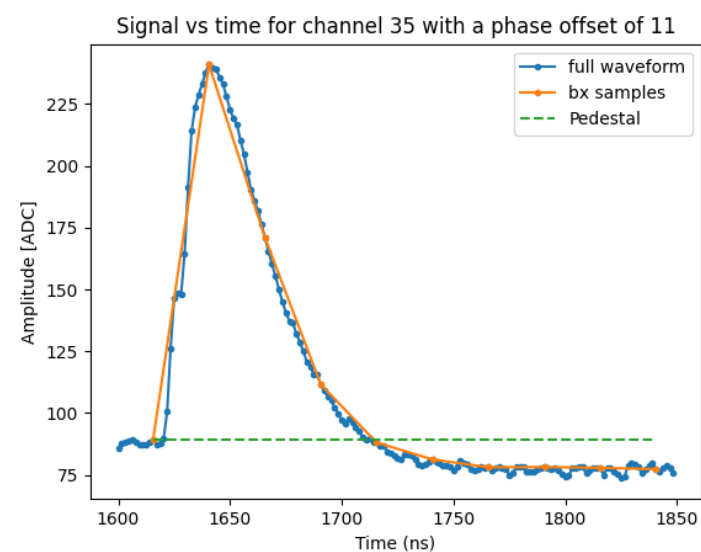
ASIC input #10 between GND and Digital supply



ASIC input #11 between GND and Analog supply



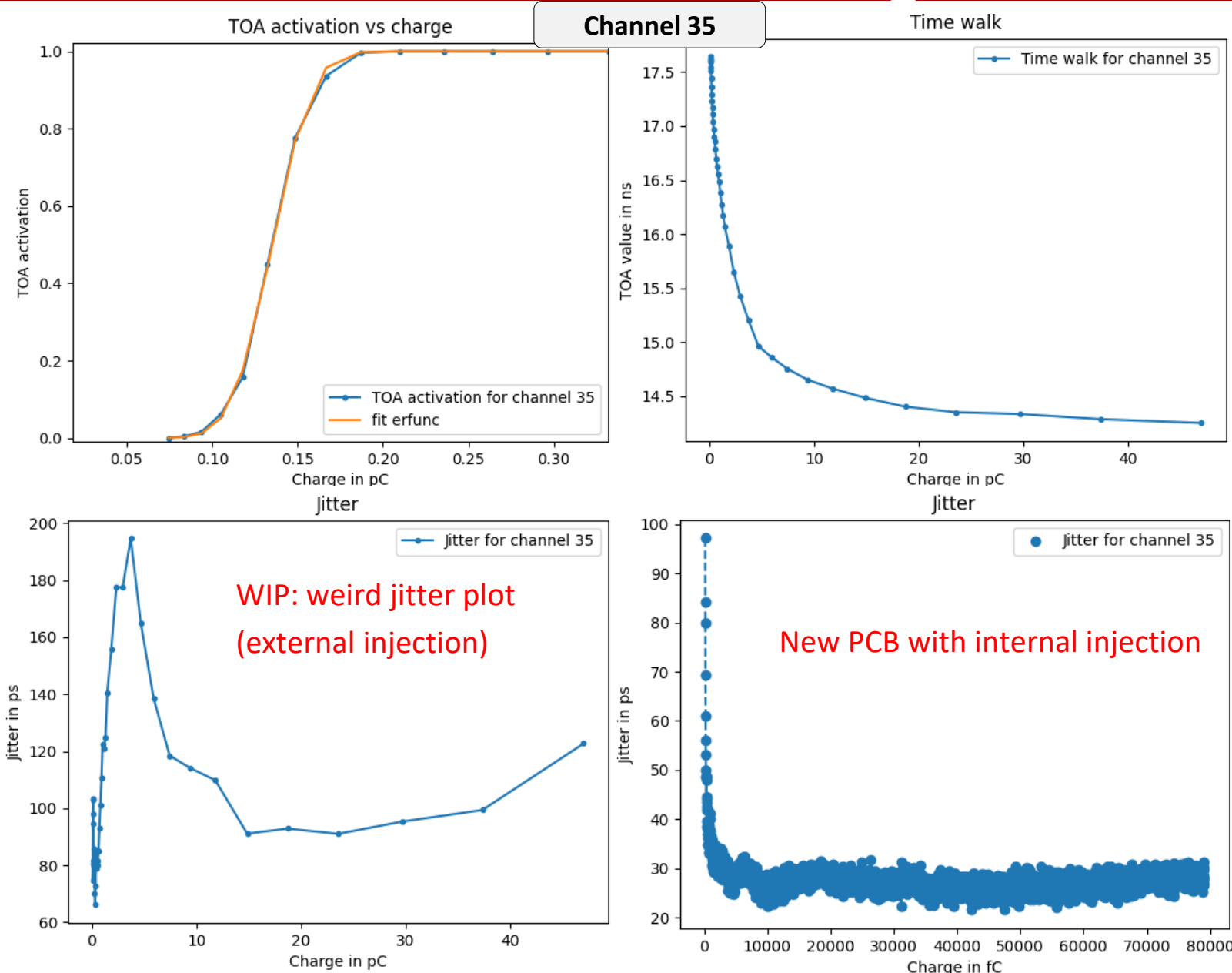
ASIC input #35 on top layer (between GND and "air")



Noise divided by ~ 3

Divided by ~ 3

- External injection setup:
  - 2.2nF detector capacitance
  - 49pF injection capacitance
  - Rise time: 2ns with a 1.23ns low pass filter
- External injection results:
  - TOA threshold at 180fC
  - 3ns Time walk
  - Weird Jitter behavior
  - Jitter and threshold is quite sensitive to the clock phase.
- Internal injection results (Old PCB):
  - TOA threshold at 200fC
  - 4.5ns Time walk
  - Similar jitter behavior
  - Jitter and threshold is quite sensitive to the clock phase.
- Internal injection results (New PCB, different configuration for the high-pass filter):
  - TOA threshold at 200fC
  - 2.5ns Time walk
  - Normal Jitter waveform



## ❑ Switched gain waveforms:

- ❑ See slides in CALOROC review indico
- ❑ Time to baseline study (always less than hit rate, see paper)
  - ❑ Time constant  $Cd * Rin$

## ❑ Noise measurements w.r.t testboards

- ❑ Crosschecks ongoing but promising !
- ❑ Need second “optimized” testboards
  - ❑ Also possible to measure on FEB with CALOROCs

## ❑ Other topics

- ❑ ASIC QR code proposal for packaging (delay for remaining packaging)
- ❑ Moving testboard reference clocks to 39.4 MHz
- ❑ **Not tested**: zero suppress, BIST, I2C daq readout
  - ❑ But I2C over fast commands **tested** @ LLR

