eRD109 update: dRICH RDO

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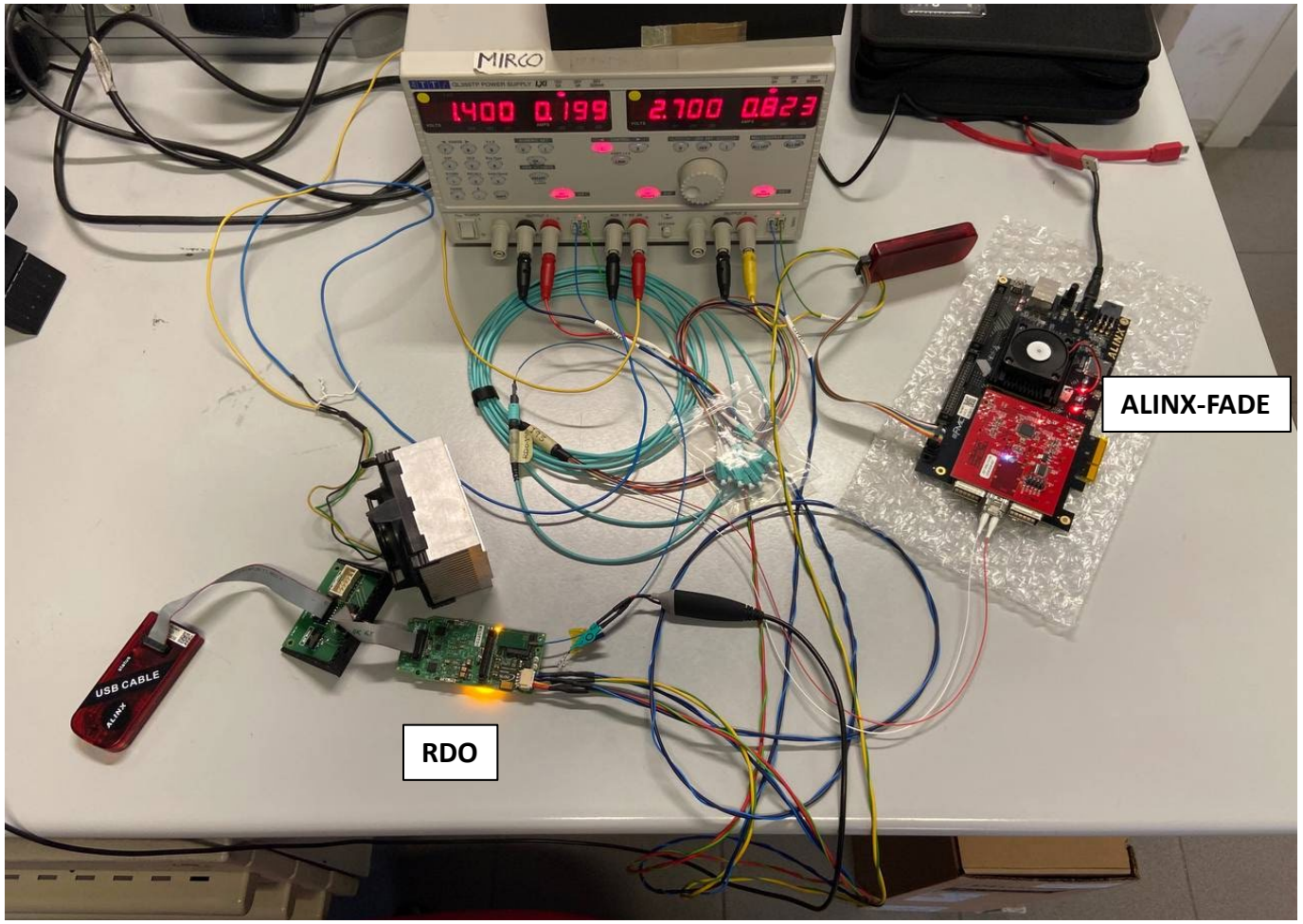
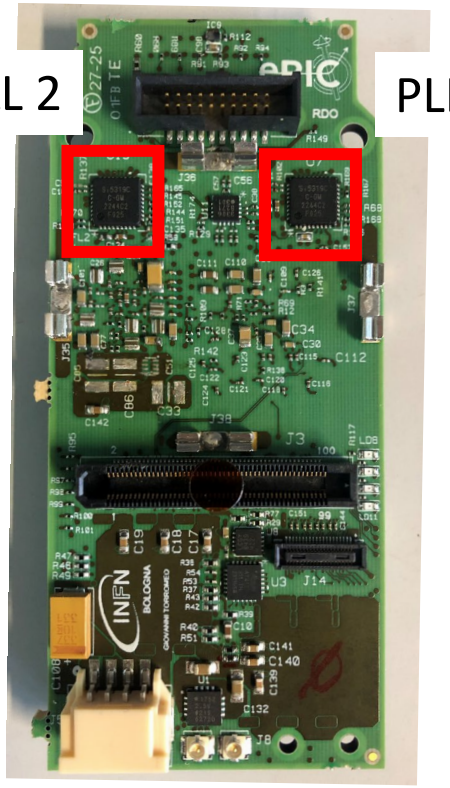
ePIC DAQ meeting
06 June 2026

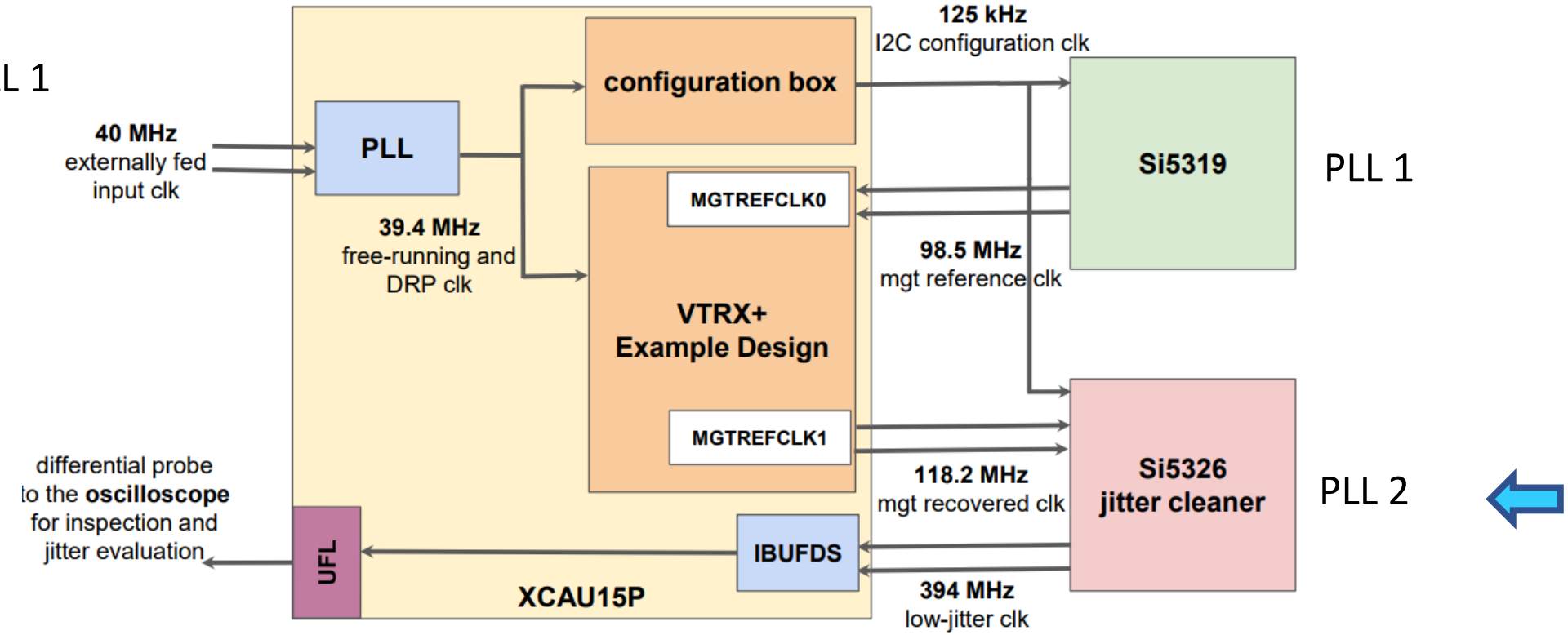
RDO – Alinx setup



- data transmission on the high-speed link between RDO -Alinx-Fade works fine:
  - **10 Gbps uplink**
  - **2.5 Gbps downlink**

RDO – Alinx setup: clocks

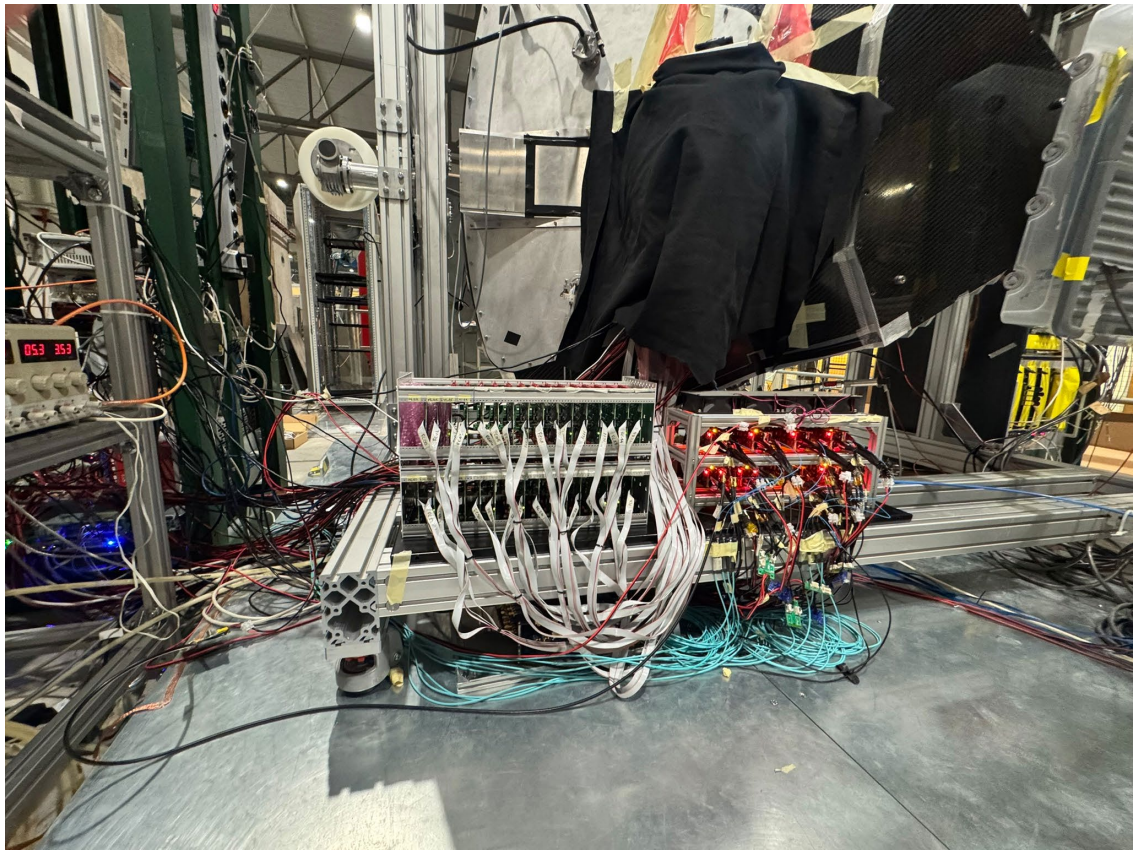


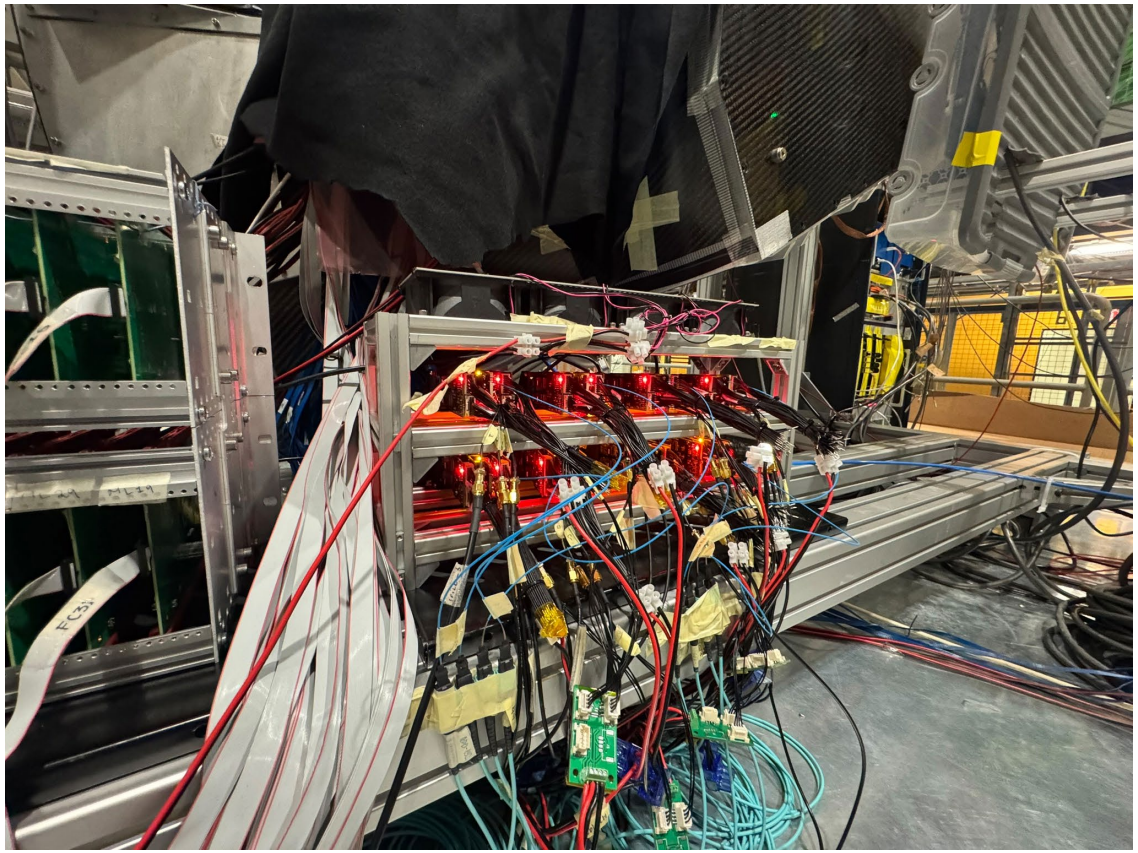


NEW: PLL 2 has been programmed via I2C and used to provide the 394 MHz clock to the Artix US+ FPGA. This clock will then be distributed to the Alcor chips.

Test beam at SPS now

From May 15th **all RDOs** have been used to equip the dRICH prototype:
in these days, all 8 RDO's are used at a test beam at SPS





Beam available from yesterday (3 June 2026)

Next steps

- now studying the Aurora protocol and planning to interface the Felix board soon