DC|DC POWER BOARD V1

for

ACLGAD ASIC & READOUT BOARDS

BROOKHAVEN NATIONAL LAB

CERN bPOL48V BASED CUSTOM 30W LOW VOLTAGE REGULATOR BOARD

Report by Tim Camarda (BNL)

Contributions and Acknowledgments on slide 12

Requirements & Specifications for fTOF….

Physical & Electrical

Parameter	Requirement	Actual	Notes
Topology	Stepdown Buck/non-isolated		Input power isolated
PCB Footprint ☑	103mm x 22mm (62mil PCB)		22.7cm^2
Power Density ☑	~1.36W /cm^2 (8.54W/ in^2)		10W / channel V_{OUT} = 1.2V, I_{OUT} = 8.3A
Input Voltage Range	☑ 13V – 15V_{IN}	14V	V_{OUT} = 1.2V 11.7 : 1 conversion ratio w/ 14V_{IN} ~8.5%$_{DUTY}$ → ~86$_{ns}$ on-time @1MHz 40$_{ns}$ bPOL48V minimum
Output Current	☑ 8.3A or 10W/channel	8.3A	83% of max current
Maximum Rated Output Current	☑ 10A$_{MAX}$ 12W/ch	10A	nominal 8.3A (10W/ ch)
Input Under Voltage	☑ < 13V_{IN}	~12V	bPOL48V requires V_{IN} > 12V
Load Regulation	☑ 1.0%	<0.5%	1A to 10A load$_{MAX}$
Output Noise & Ripple Pre-LC filter (25MHz)	☑ < 1%	0.7%	< 8$_{MV\ p\text{-}p}$ bulk capacitance (pre-filter)
Output Noise & Ripple post-filter	☑ 0.1%	0.15%	Typically achieved with Linear Regulation & PSRR but not an option here Should improve w/ 5th order filter or even with addition of decoupling on ASIC board
Transient Response	☑ 1.0%	0.4%	recovery band

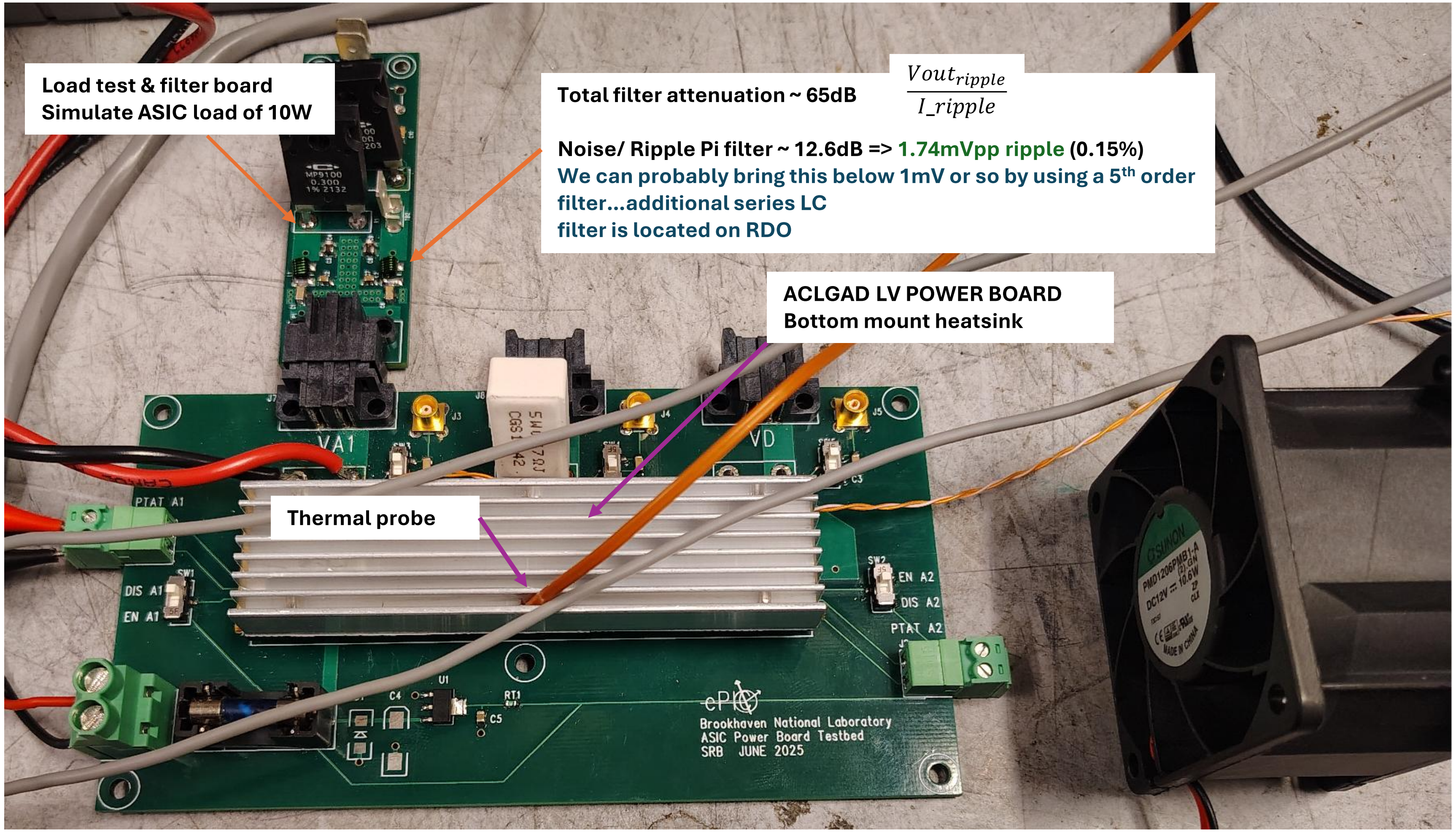
Efficiency & Environment

Parameter	Requirement	Notes
Efficiency	70%$_{@10W}$	Measured Efficiency$_{PEAK}$ >78.8% Efficiency$_{10W}$ ≈ 68.9% @ F_{SW} = 1MHz
Operating Temperature	0°C to 50°C	Without derating
Maximum Tj_{BUCK}	< 80°C	35°C$_{AMBIENT\ INNER\ DETECTOR}$
Maximum Tj_{GaN}	< 100°C	35°C$_{AMBIENT\ INNER\ DETECTOR}$

☑ Tested to spec

30W ACLGAD LV POWER BOARD
Load, Thermal & Output Ripple Testing

Report by Tim Camarda, BNL



LOAD & THERMAL TESTING

CH1A = 1.2V, 8.3A = 10W
CH2A = 1.2V, 8.3A = 10W
CH3D = 1.2V, 8.3A = 10W

After 1 hour:
Heat Sink w/ small fan: 40°C
PTAT (bPOL48 internal): 60°C
Inductor: 50°C

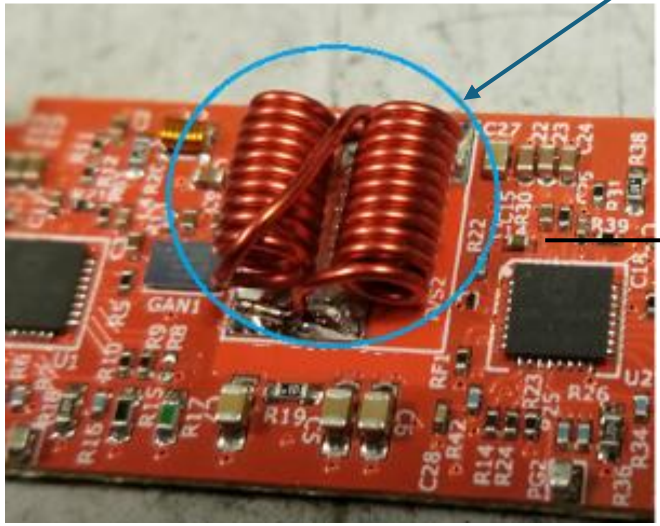
Power Efficiency => P_{IN} / P_{OUT} 68.9%

Inductor construction…

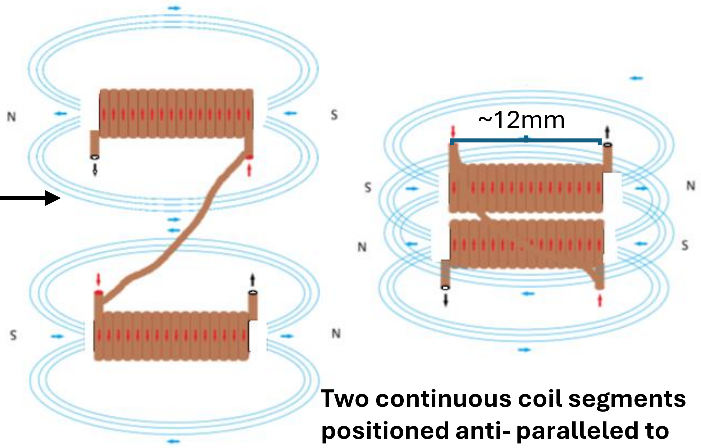
The switching inductor is confined to a L=12mm x W=10mm x H=9mm footprint on the PCB.

~260nH to 300nH 10A air-core inductor wound in anti-parallel with 18AWG magnet wire: 10x turns/ side

12mm x 10mm space
Note: height restriction is ~ 9mm



100mm x 20mm PCB, 2oZ copper top / bottom



Two continuous coil segments positioned anti- paralleled to each other.

The inductor value in Henrys is chosen to balance practical physical size, Inductor ripple and losses. *We try to achieve a ripple current between 30% to 50%*

Inductor ripple I = $L * \frac{di}{dt}$ → $\Delta I_L = \Delta t \; / \; L = \frac{12.8V * 86E-9}{268E-9} = 4.09A = 41.0\%$

$V_{IN} - V_{OUT}$ sw time

Inductor in Henrys

of 10A load

Power inductor design criteria

- saturation current
- low DCR
- core loss (non for air)
- EMI containment
- Ripple current

Inductor DC resistance = ~4.4mΩ

$P_{LOSS\ INDUCTOR\ DC} = I^2 * R_{DC} = 8.3^2 * 4.6E\text{-}3 = 0.3W$

$P_{LOSS\ INDUCTOR\ AC}$ =

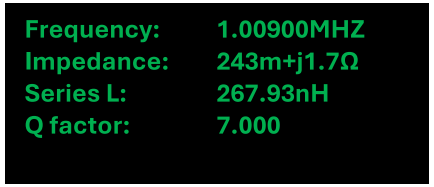
$I_{RMS\_AC} = \frac{\Delta I_L}{\sqrt{12}} = \frac{4.09\ A}{3.464} = 1.180\ A \Rightarrow P_{AC\_loss} = (I_{RMS\_AC})^2 \times R_{AC} \Rightarrow$

$P_{AC\_loss} = (1.180\ A)^2 \times 0.243\ \Omega$

$$P_{AC\_loss} = 1.392 \times 0.243 \approx 0.340W$$

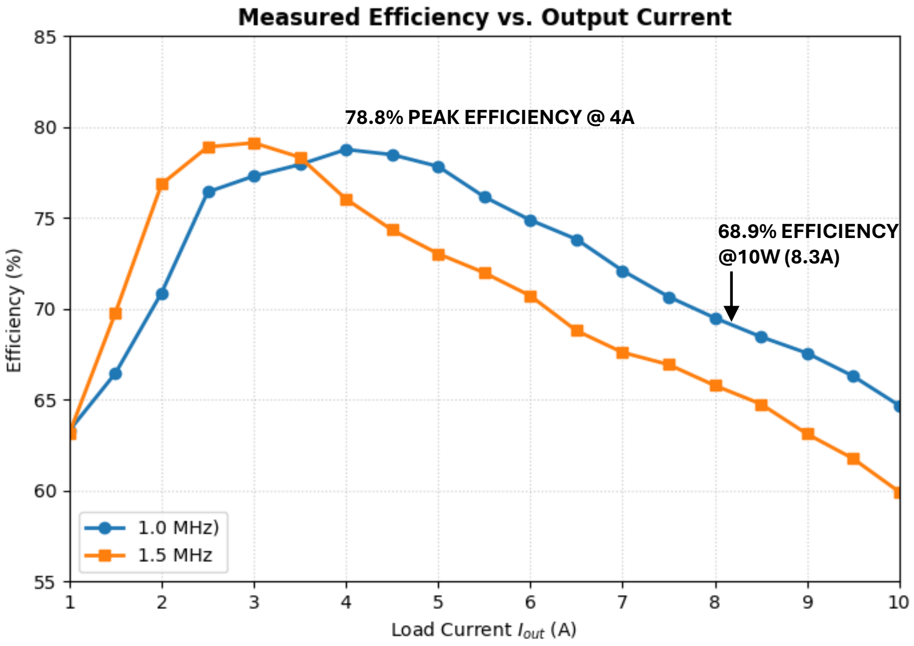
$P_{LOSS\ INDUCTOR\ DC+AC} = 0.30W + 0.340W = 0.640W_{TOTAL\ INDUCTOR\ LOSSES}$

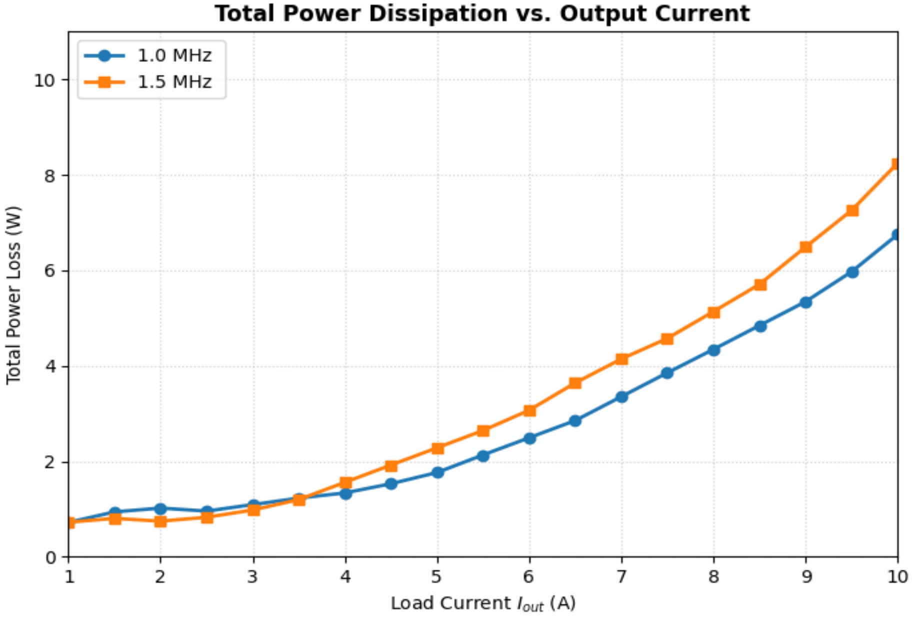
0.640W / 10W = 6.4% $_{\text{INDUCTOR LOSS}}$ **(not too bad for high frq buck converters)**



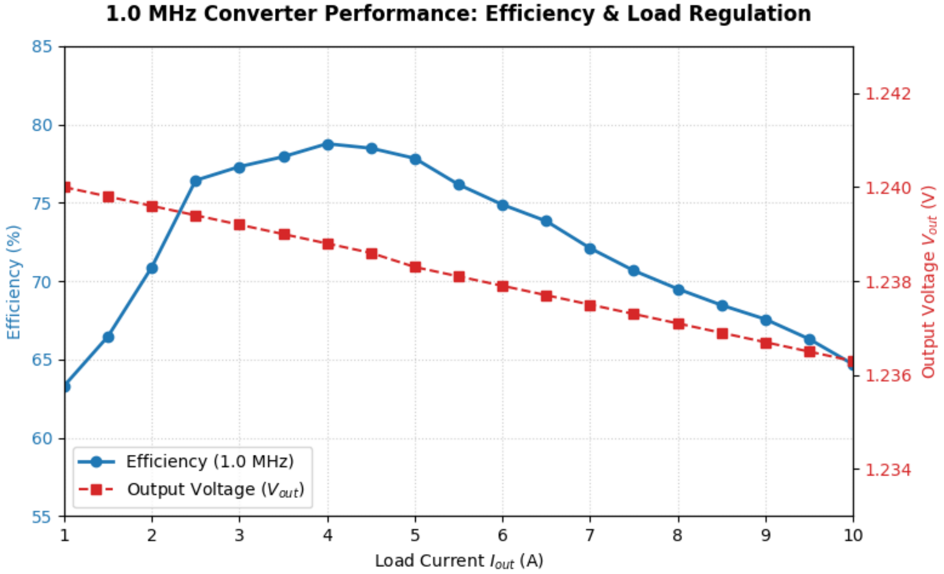
VNA measurement profile for 270nH air-core inductor @ 1.0MHz

Power Efficiency…





Peak Efficiency$_{1.0MHz}$:	**78.8%**
Efficiency$_{10W}$:	**68.9%**
Load Regulation:	**0.30%**
Inductor:	**268nH air-core**
$V_{IN\text{-}REMOTE\ SENSE}$:	**14.0V**
Cable Length V_{IN}:	**60$_{FEET}$**



1.0 MHz Fsw Efficiency vs load current
V_{OUT} vs load current

- **Efficiency is dominated by *switching losses* as evident when increasing F_{SW} from 1.0MHz to 1.5MHz**
- **As per inductor loss calculation in slide five, inductor looses decrease with F_{SW} increase**
- **However, switching losses increase with higher F_{SW}**
- **Conclusion: Optimized switching frequency seems right about 1.0MHz**

Noise/ Ripple measurements…

NOTE: Noise & Ripple measurements combined
No significant measurable difference above 25MHz

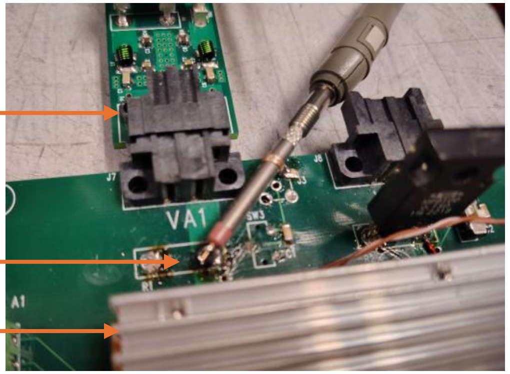
	Value	Mean	Min	Max	Std Dev
2 Peak−Peak	537.7µV	575.1µ	486.9µ	700.5µ	80.02µ

Baseline noise w/ DC converter turned off

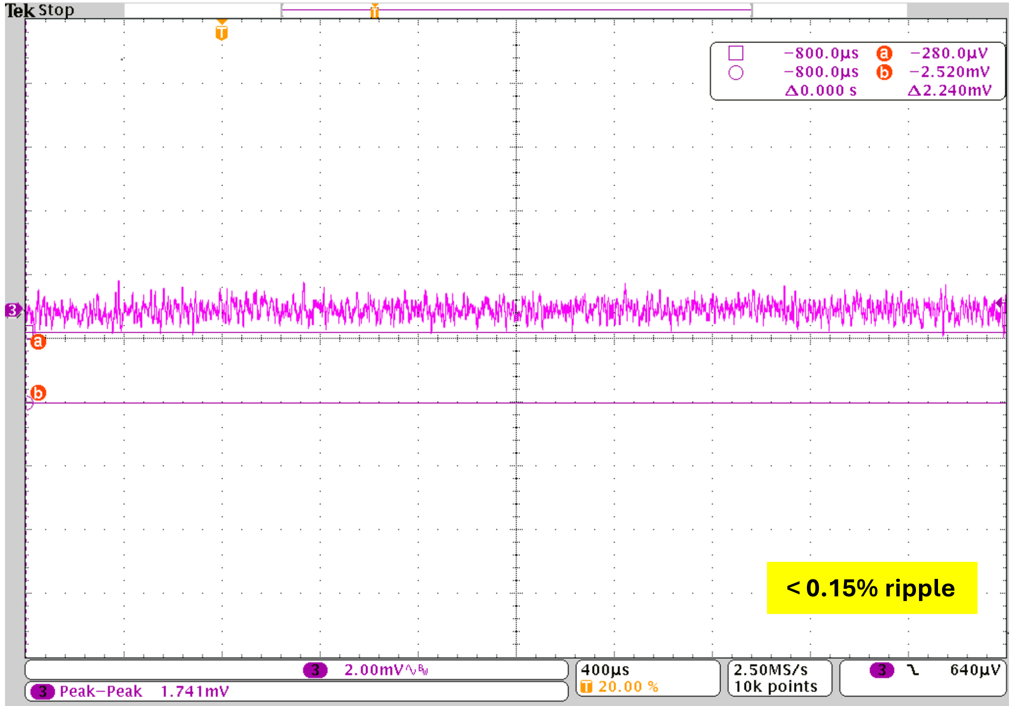
3d order low pass LC filter (readout board)

POL ripple measure @ pre-filter stage

LV PB



Noise/ Ripple measure pre-filter stage ~0.7% ≈ -52dB attenuation

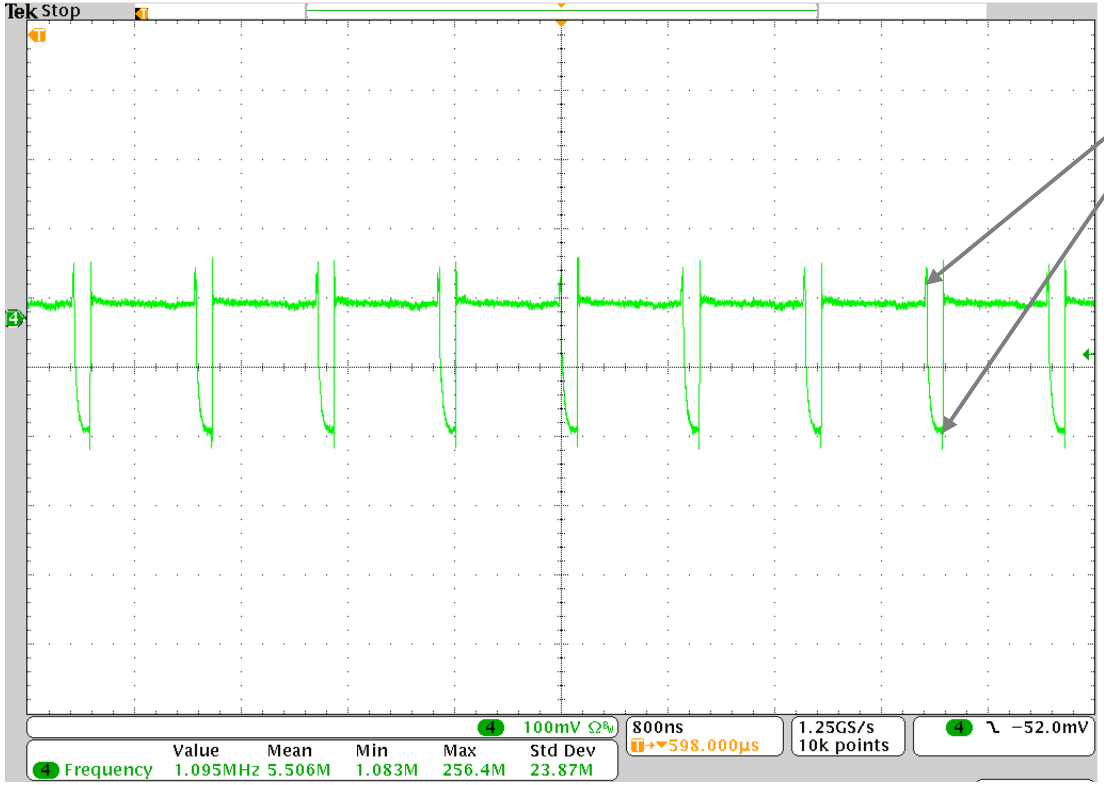


Noise/ Ripple measure post-filter stage ~0.15% ≈ -12.5dB

Brookhaven National Laboratory

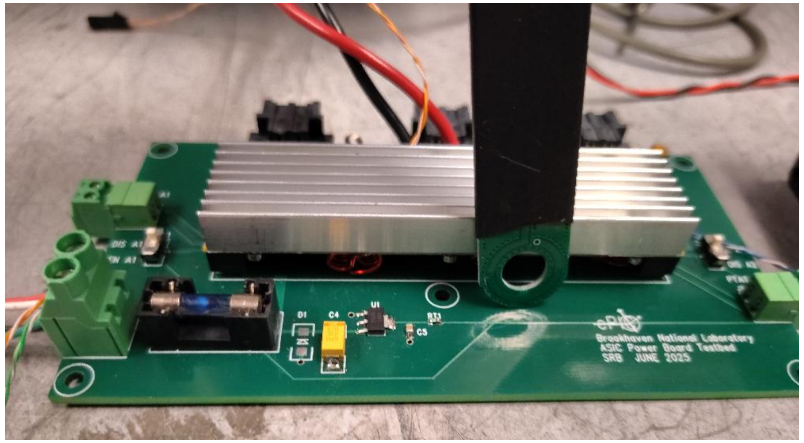
ePIC

Radiated EMI (relative measurements with H-Field Probe)…



Switching Inductor Nearfield EMI measure

- switching node ringing (minimize in the layout efficiency)
- loop parasitic + LC resonance
- PCB stackup => Switching node is placed 3-4 mils from ground return plane

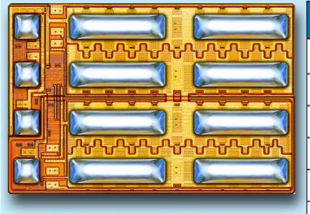


H-field EMI probe positioned to obtain strongest reading

Field strength exponentially decays as probe distance increases

bPLO48V & GaN Thermal Performance & Power Losses…

Results presented here are with 11mm x 20mm x10mm aluminum Heatsink…Board will be used with liquid cooling plate in fTOF & bTOF assembly



Package size: 2.59 x 3.85 mm

EPC2152 ePower™ Stage IC

Driver stage for bPOL48V with internal GaN swicth

Absolute Maximum Ratings				
SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{IN}	Input voltage		80	V
SW (continuous)	Output switching node (SW to GND), continuous		80	V
V_{DD}	Internal low side supply voltage		14	V
V_{BOOT} – SW	Internal high side supply voltage (V_{BOOT} to SW)		14	V
HS_{IN}, LS_{IN}	PWM logic inputs	-1	5.5	V
T_J	Junction temperature	-40	125	°C
T_{STG}	Storage temperature	-55	150	°C

Try to stay within 80% or 100°C
Note: device with bottom heatsink has a theoretical power output of ~40W!
We need ~ 15W / channel (44W / 3)

Conditions after 1hour: CH1: $10W_{OUT}$ **Ch2:** $10W_{OUT}$ **CH3:** $10W_{OUT}$

Ambient: 21°C

Thermal management: Total board power => 30W/ ~70.0%$_{EFF}$ = 43.0W$_{TOTAL}$

$$P_{loss} = P_{TOTAL} - PL_{OAD} = 43W - 30W \approx 13.0W_{LOSS}$$

bPOL48V PTAT$_{bPOL\#2}$ measure external case: 48°C

Note: Tj falling trip level 80°C (120° shutdown)
We can derive form this a SOA of ≈ 80°C

⇒ Tj = 60.3°C **(reported junction temperature from bPOL48V)**
⇒ 39.3°C rise over ambient
⇒ Calculated for 35°C$_{AMBIENT}$ => T_J is around 74.3°C

How efficient does our heatsink need to be to keep the board from going > 50°C ?

Environment

$$\theta_{sa} = \frac{50^{\circ}C - 35^{\circ}C}{13.0W} \qquad \theta_{sa} = \frac{15^{\circ}C}{13.0W} \approx 1.15^{\circ}C/W$$

Thermal resistance from HS to ambient

GaN device: measured external case: 60°C

NOTE: Tj is calculated for case package thermal resistance
Thermal Wafer Chip => Very low case to junction thermal resistance

⇒ Tj ≈ 63°C
⇒ 42°C rise over ambient
⇒ Calculated for 35°C$_{AMBIENT}$ => T_J is around 77°C

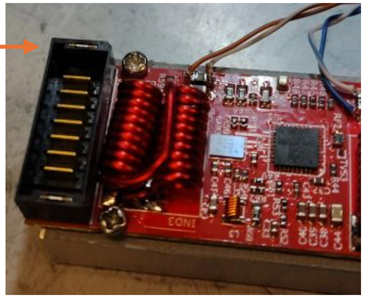
Cooling plate thermal performance still needs to be done!

DRAFT

UMPT/ UMPS Power Blade Mating Connectors

Contact Power Density => Required maximum current: 10A_{MAX}

Connector real-estate: (20mm x 8mm) 160mm^2



Required power / thermal density

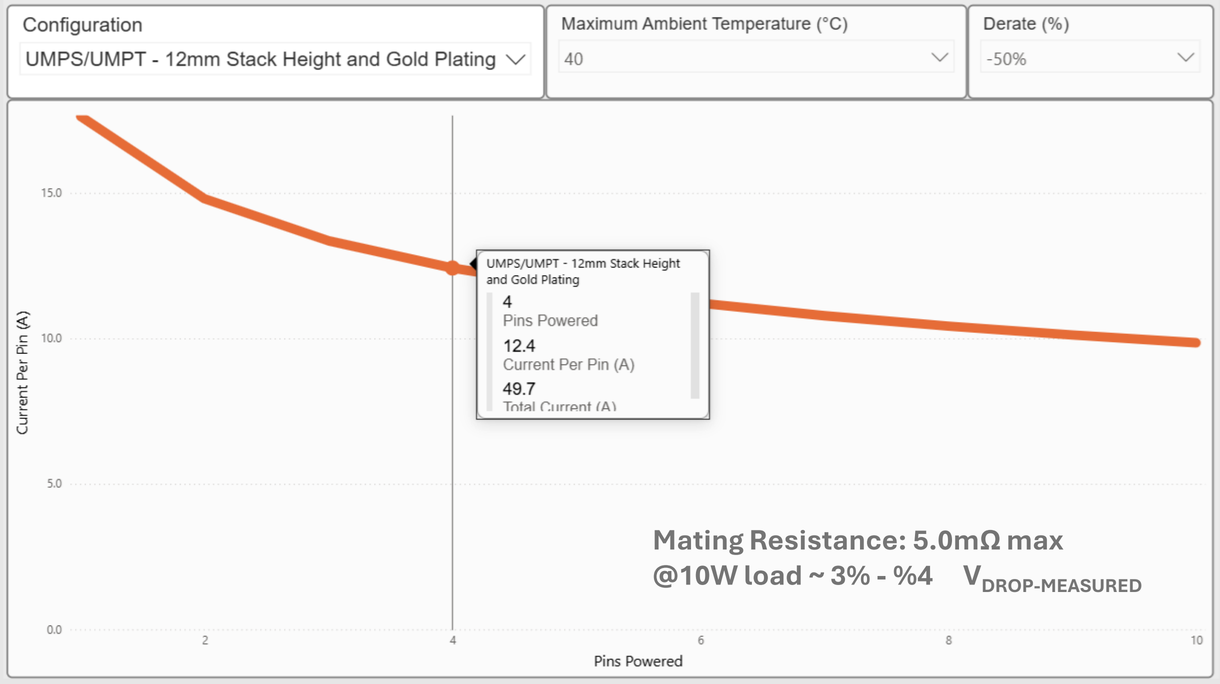
2x pairs each 10A => Total of 40A => 40A * 1.2V = 48W

48W/ 1.6cm^2 = 30.0W / cm^2

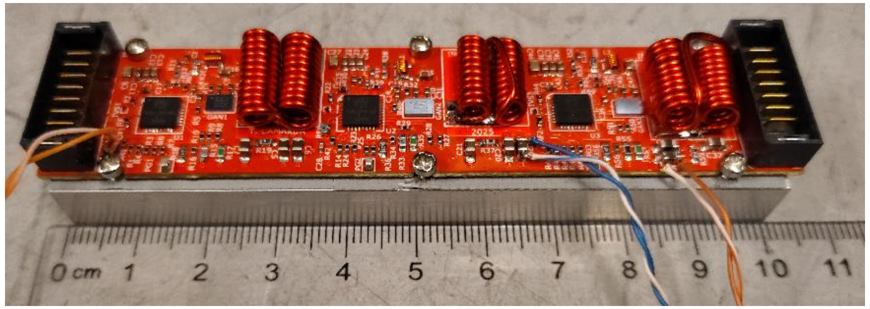
Manufacturers derating curve calculated power density => 49.6W /cm^2

EIA-364-31 ENVIORMENTAL TESTING FROM SAMTEC:

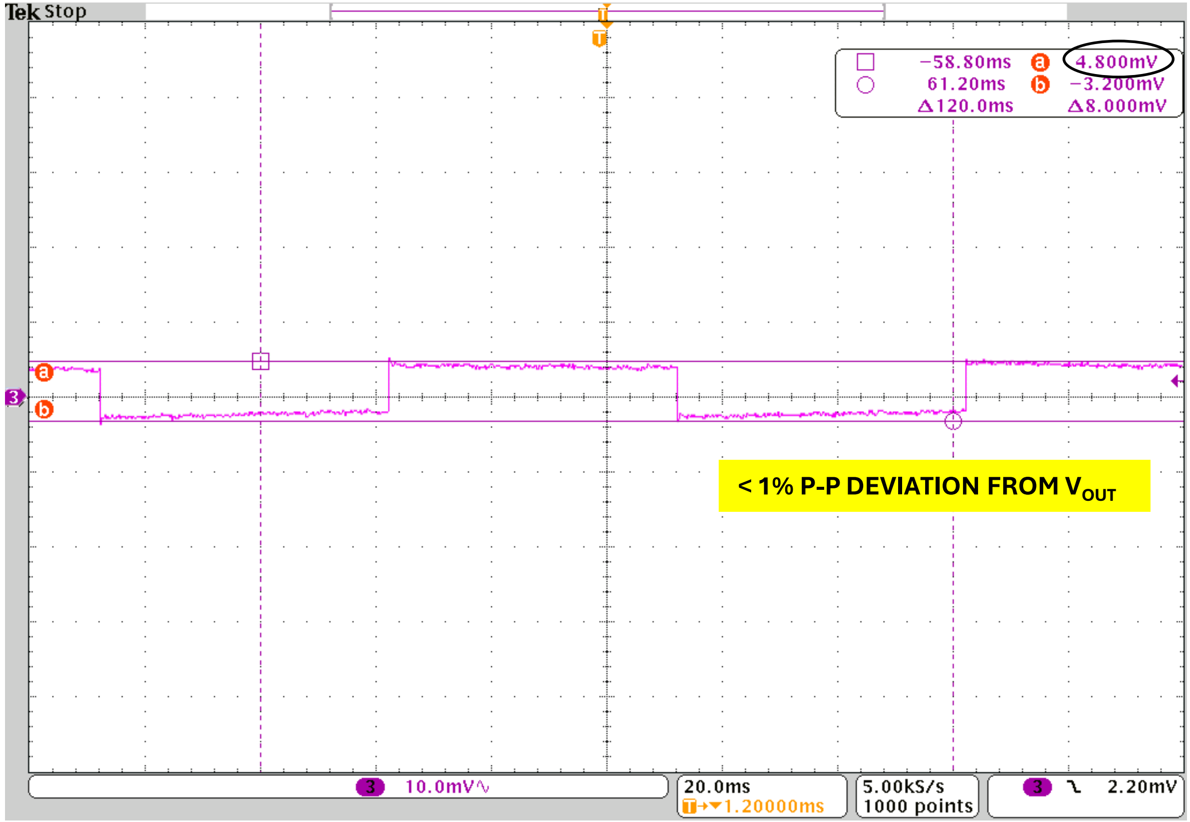
- **High humidity environment**
- **Temperature cycling: 25°C to 60°C**
- **Aging Contact Resistance over 10$_{YEARS}$ (LLCR) => Δ 0.001 Ohm**



If necessary…we could parallel contacts by eliminating the requirement to monitor PTAT and unify Enable 1 and 2



Transient load testing…

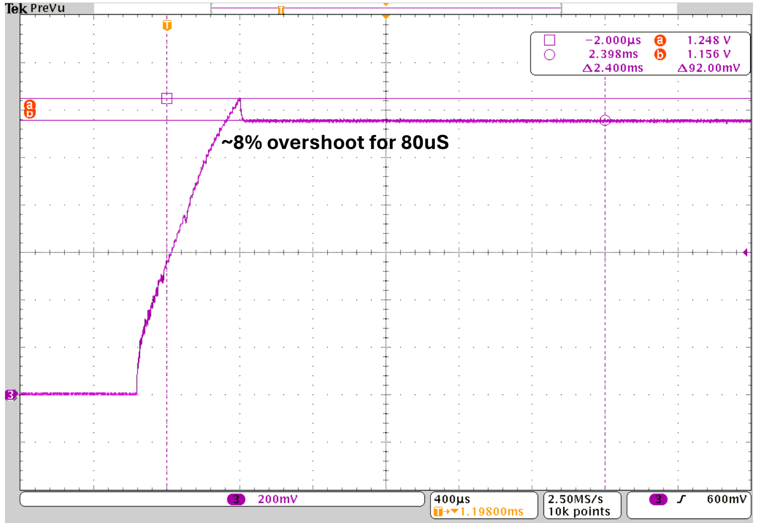


Output deviation for a ~40% load step with 1 A/µs slew rate.

Recovery band = V_{ABOVE} / V_{OUT} x 100 = 4.8mV/ 1.2V = 0.4%

3A transient load response 60% to 100% ΔLoad

For a +/- 1% recovery band acceptable tolerance is 1.2V x 0.01 = Δ12mV Measured: +4.8mV$_{ABOVE}$ -3.2$_{BELOW}$



- Power-up impulse response into an 8.3A load
- Simulate power-up from platform 14V power w/ buck enabled
- Feeder cable: ~60feet

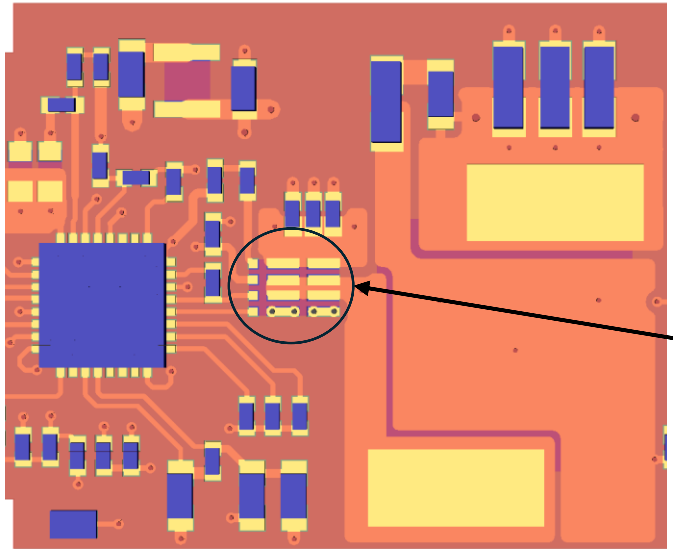
Recap...

Overall, our testing results look very good.

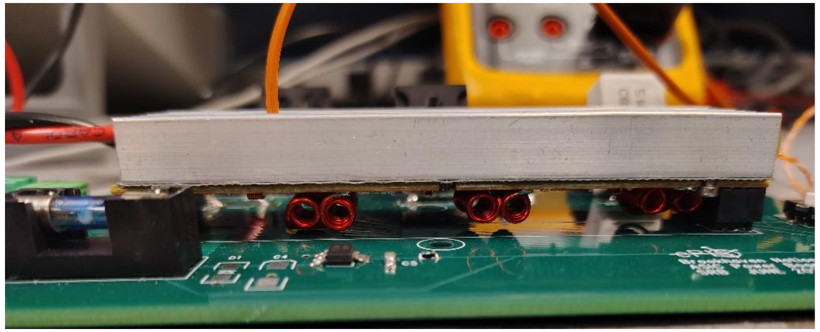
- **Board thermal transfer characteristics are carrying away the heat quite well. With 30W loading the small HS (100mmx10mm x 10mm) with a small fan, the board is operating ~40°C after 1 hour...**
- **bPOL48 buck converter internal running under 50°C (well within spec)**
- ***GaN FET temperature SAT***
- **Efficiency looks decent with >78.8% peak and 10W efficiency 68.9%**
- **Noise & Ripple look very good => 0.15% post filter, ripple could improve at ASIC board with more capacitance or 5th order filter to achieve <1mV ripple**
- **Near field EMI looks good also...**
- **60 foot feeder cable test: stable performance**
- **3A transient response: < 1%**
- **Repetitive power cycling: SAT**

Next board spin...

- **Mitigate switchnode parasitics**



Move switchnode to top layer



power board side view plugged into test load PCB

Contributions:

Gerard Visser......(Indiana U.) For his suggestion on the inductor winding

Acknowledgements:

The following people helped in securing funding and or getting us sample bPOL48V2 buck regulators necessary to complete this project

Prithwish Tribedy........(BNL)

Tonko Ljubicic............(Rice U.)

Norbert Novitzky........(ORNL)