More efficiency with bPOL48 DC/DC for ePIC

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Constraints:

- Use bPOL48 ASIC and GAN IC of some sort
  - Another strategy is evaluate radiation tolerance of various COTS silicon IC's, not discussed today
  - bPOL48 is only a controller – need GAN chip with integrated driver (e.g. EPC2152 that bPOL48 was designed to be paired with); there are not many options – and the options are not ideal
- Nonmagnetic inductor (I mean, no core) due to ePIC B field
  - Not required for LFHCAL, BHCAL, nHCAL? Iron powder will work, and more efficiently!
- My focus is on up to a 1 – 3 A load current, 1.0 – 3.3 V output
- Vin will be chosen to optimize some combination of efficiency and cable size/mass
  - Details will vary by subsystem, but in practice I think we would like 15 – 20 V input probably
  - Upper end of this likely constrained by Wiener MPOD specifications, *or we get a custom version*

Principal losses – some rather crudely estimated

the FET's are too big – but we have no choice here…

Loss type	general formula	Case A	Case B
bPOL48 power	V_{dd}*6mA	6mA*20V = 120 mW	6mA*5V = 30 mW
GAN power (gate drive, mostly)	V_{dd}*IddGAN; (20% proportional to f)	26mA*20V = 520 mW	21mA*5V = 105 mW
high FET I^2R	$\beta*I_L^2*R$	$\beta*(2\ A)^2*10m\Omega$ = 4 mW	$\beta*(2\ A)^2*9m\Omega$ = 3 mW
low FET I^2R	$(1-\beta)*I_L^2*R$	$(1-\beta)*(2\ A)^2*10m\Omega$ = 36 mW	$(1-\beta)*(2\ A)^2*10m\Omega$ = 33 mW
inductor I^2RDC	I_L^2*R	$(2\ A)^2*44m\Omega$ = 176 mW	$(2\ A)^2*60m\Omega$ = 240 mW
inductor I^2RAC	(Parseval's thm.)	400 mW	153 mW
charge losses	Q*f*VIN	~37nC*1.3MHz*20V = 960 mW	22nC*750kHz*20V = 330 mW

(~62 % efficiency calculated; consistent w/ Norbert's meas.)

(~79 % efficiency calculated; can we actually get that?)

Case A: bPOL48+EPC2152, 20 V in, 1.8 V 2 A out, 1.3 MHz, foCAL PCB toroid
Case B: bPOL48+EPC23104, 20 V in + *5 V auxiliary (ideal)*, 1.8 V 2 A out, 750 kHz, GV solenoids
duty factor β=1.8/20=0.09 (roughly!),
see backup slides here for inductor measurements

case A except w/ iron powder inductor:
8 mW DC loss, 20 mW AC loss

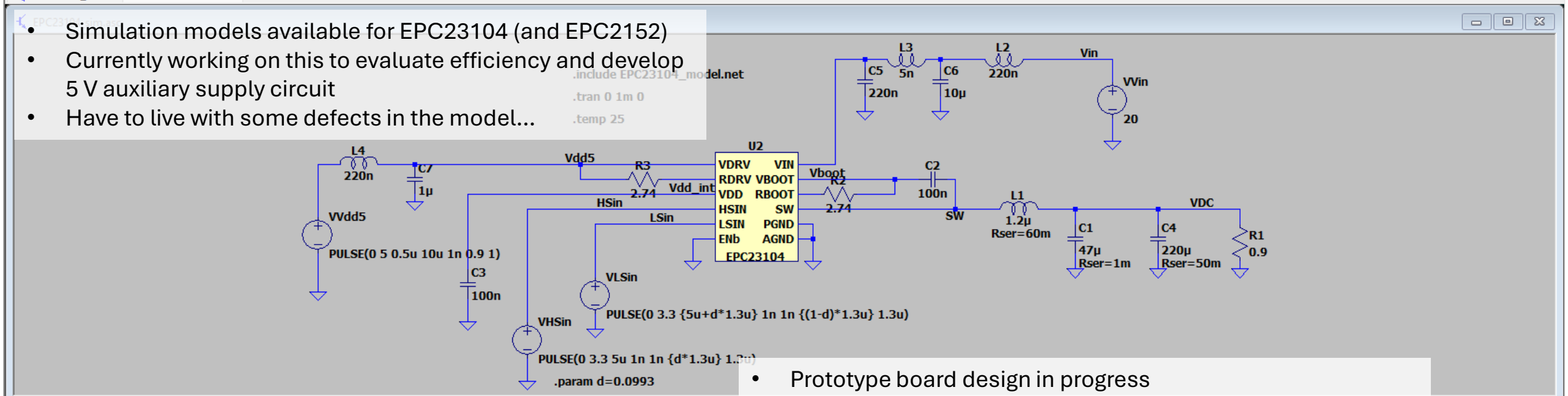
Three lines of attack

- Lower the frequency
  - But the inductor losses will go up, for same dimensions of it
- Use the EPC23104 which has substantially lower charge losses *and which enables the third way:*
- Power the converter circuits from 5 V auxiliary
  - Simplest way – a separate input to the board
  - Best way – steal this power from a DC/DC output somehow – even at 50% efficiency it helps
    - Only feasible for a 3 V or higher output, I think

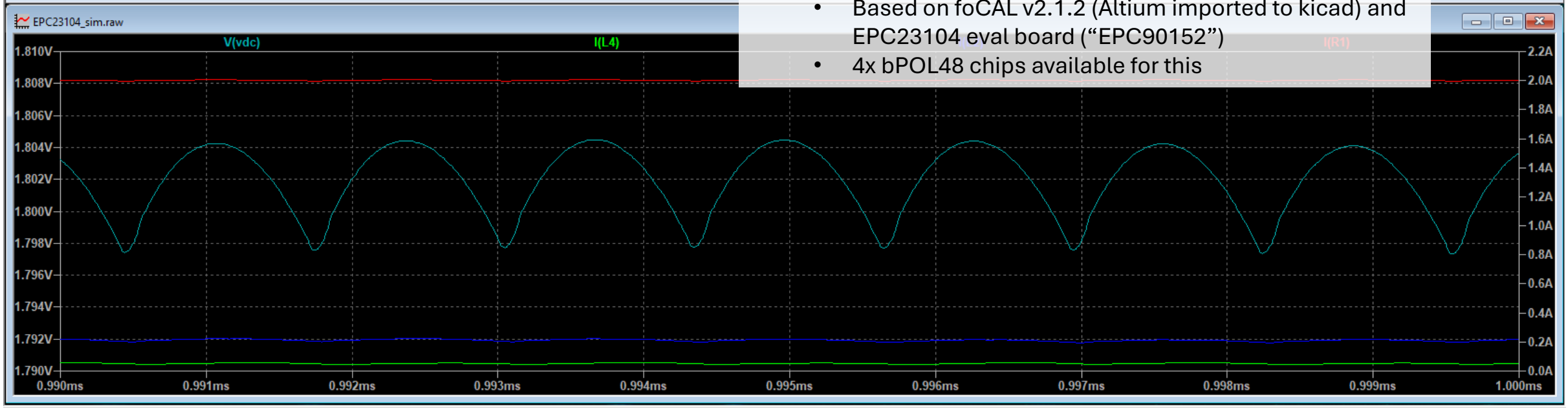
Or as a last resort

- Lower the input voltage
  - Bad idea though, since the whole point of using DC/DC was to *raise it as much as possible* and hence reduce the wire size and mass
- Rearrange system to gang more loads together on each DC/DC
  - More channels per DC/DC (more channels per FEB? More FEB per DC/DC?)
  - It sounds nice but in some cases it might conflict with system/mechanical constraints, and might introduce new problems with voltage drops in connections

- Simulation models available for EPC23104 (and EPC2152)
- Currently working on this to evaluate efficiency and develop 5 V auxiliary supply circuit
- Have to live with some defects in the model…



- Prototype board design in progress
  - Based on foCAL v2.1.2 (Altium imported to kicad) and EPC23104 eval board (“EPC90152”)
  - 4x bPOL48 chips available for this

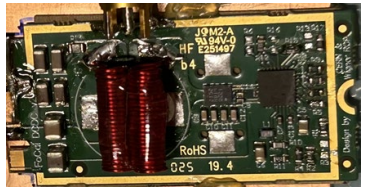


x = 0.99793ms y = 1.81058V, 2.264A

Development plans

- Protoype board w/ solenoid inductor, bPOL48 + EPC23104, 5V auxiliary, and attempted prototype of deriving the auxiliary from 3.3 V output. Test results in July.

- Need a set of specifications – **mainly mechanical and thermal** – for a generic ePIC DC/DC module
  - Like the foCAL v2.1.2 except



  - with some provision for <u>conduction cooling to the main board</u>
  - with an input filter!
  - and maybe an output filter
  - possibly a different connector

- “Final” design of this DC/DC either as a module, if there are other applications, or else simply on the bwd and fwd ECAL FEB’s. (On the FEB’s certainly makes cooling easier, in these cases… But the module, if it will be useful, is worth pursuing.

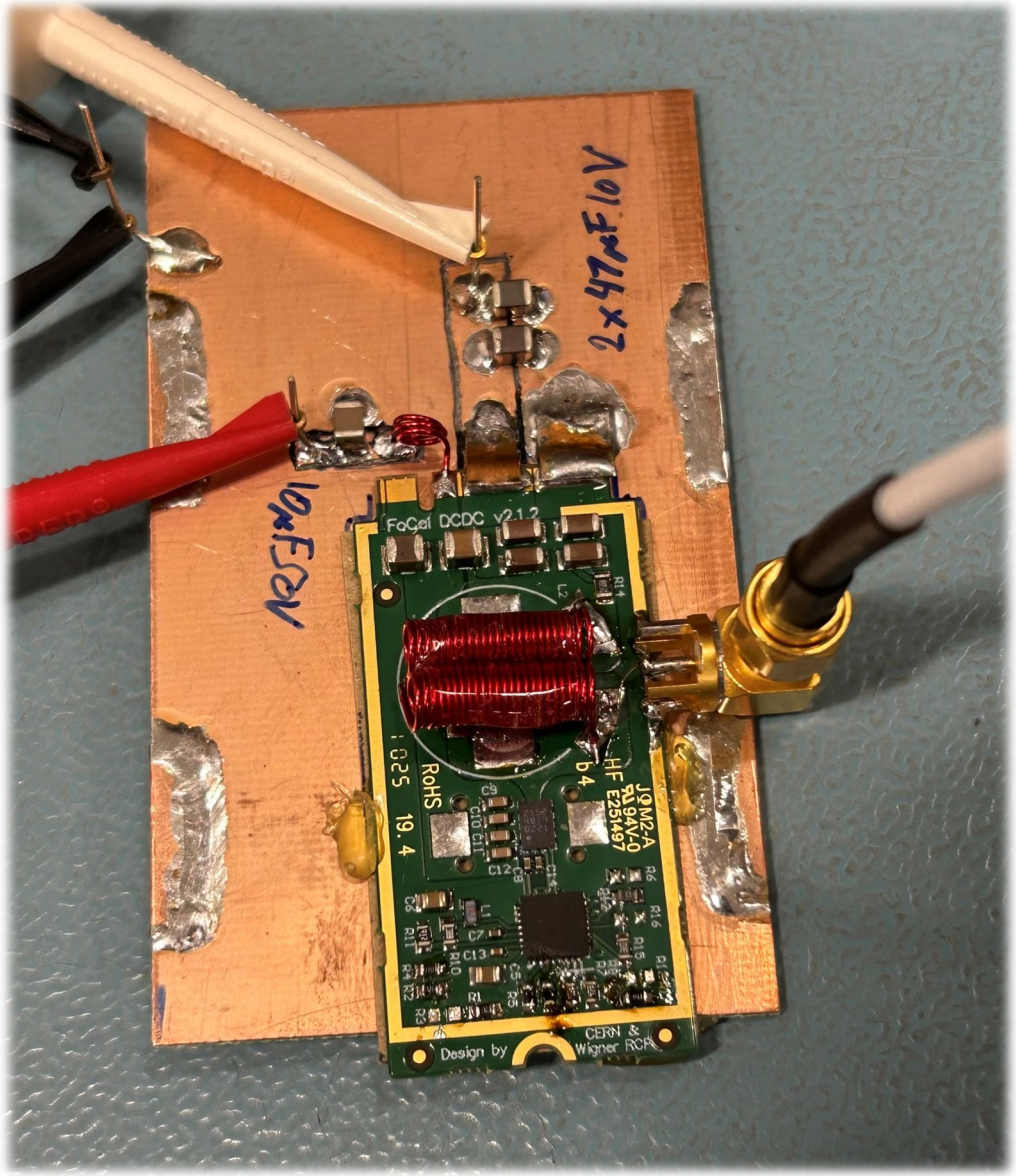
Help define the module specifications!

BACKUP SLIDES – OLD PRESENTATION ON bPOL48 TESTING, slightly refreshed

Investigations on bPOL48 / EPC2152 with FoCAL v2.1.2 power board (hacked)

- Efficiency
- Noise
- Transient response

my work is aimed at 1.8 V, 1 – 2 A loads (FEMC)



shown before output filter was added

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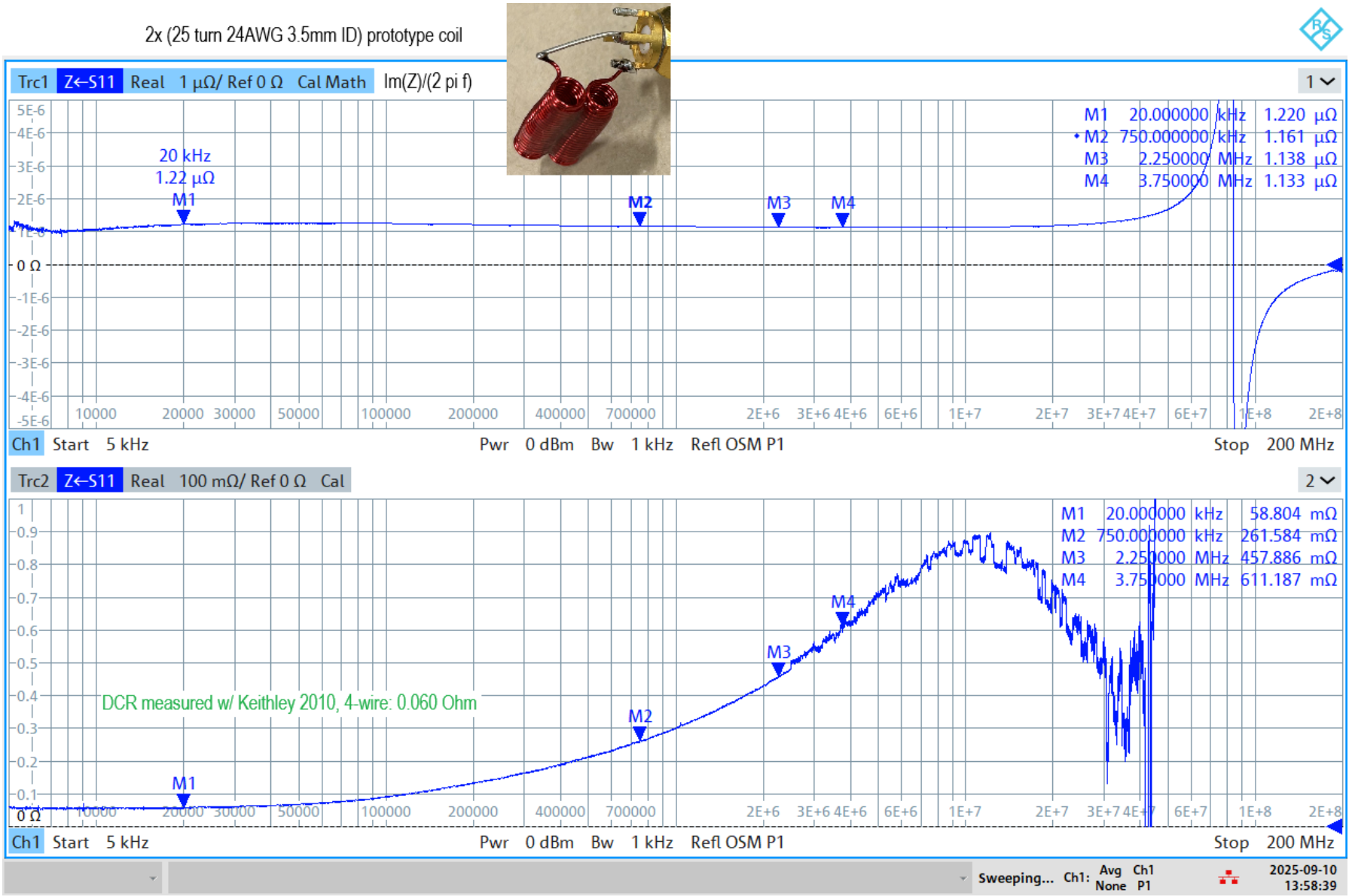
9/25/2025 ePIC Electronics & DAQ meeting

1st pass 1.2 µH inductor

(It's immediately evident from bPOL48 / EPC2152 datasheets that for a 1 – 2 Amp output, we want to operate at a much lower frequency than "standard" bPOL48 applications… say 750 kHz)



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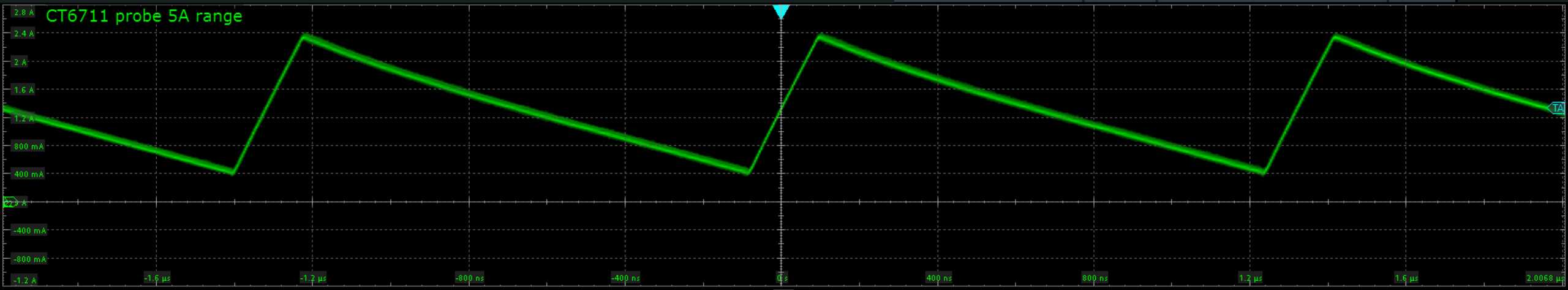
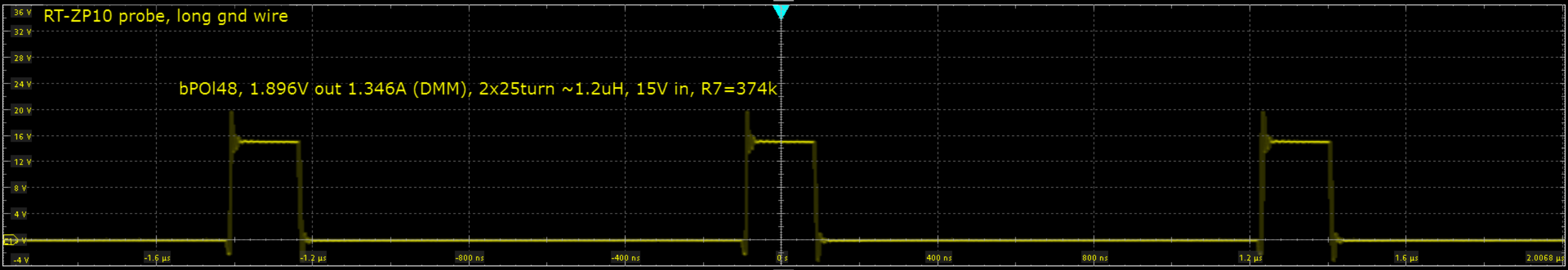
A look at some key waveforms (1.2 µH, 1.8 V ~1.35 A out)

Trigger: Edge 1.33 A Auto Stop | Horizontal: 400 ns/ 6.8 ns | Acquisition: 10 GSa/s Sample RT 40 kpts Hist 1.54 k | Info | 2025-09-10 15:51:29





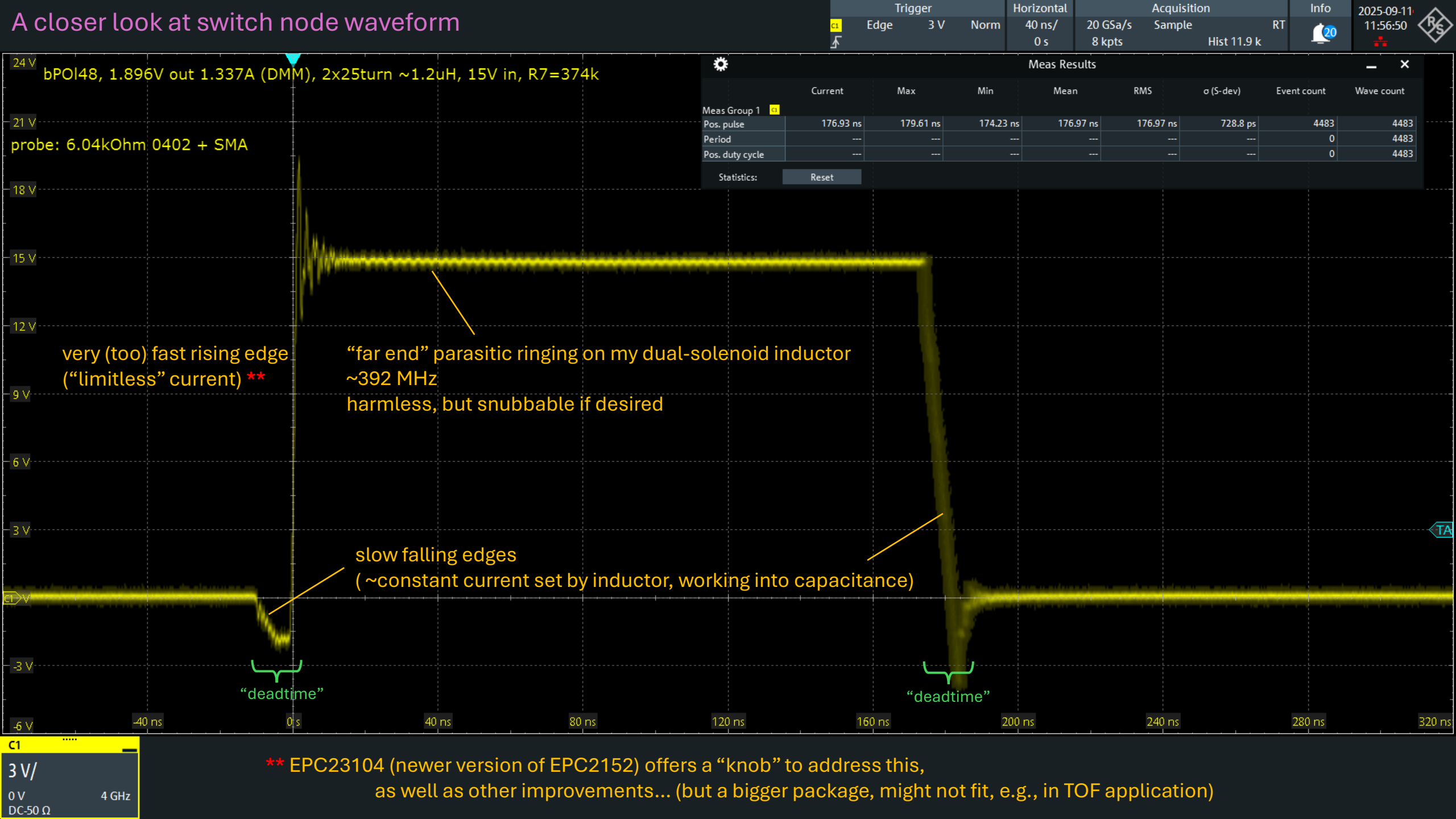
	Current	Max	Min	Mean	RMS	σ (S-dev)	Event count	Wave count
Meas Group 1								
Frequency	758.56 kHz	759.91 kHz	756.58 kHz	757.98 kHz	757.98 kHz	554.03 Hz	566	566
Pos. duty cycle	13.473 %	13.605 %	13.284 %	13.424 %	13.424 %	0.054 %	566	566
Meas Group 2								
Peak to peak	1.9605 A	2.0079 A	1.9447 A	1.9653 A	1.9653 A	10.72 mA	566	566
Cycle mean	1.3239 A	1.3723 A	1.2714 A	1.3277 A	1.3278 A	16.114 mA	566	566
Cycle RMS	1.4318 A	1.4771 A	1.3834 A	1.4358 A	1.4359 A	14.985 mA	566	566

Statistics: Reset

C1: 4 V/ 0 V 500 MHz DC-1 MΩ 10:1

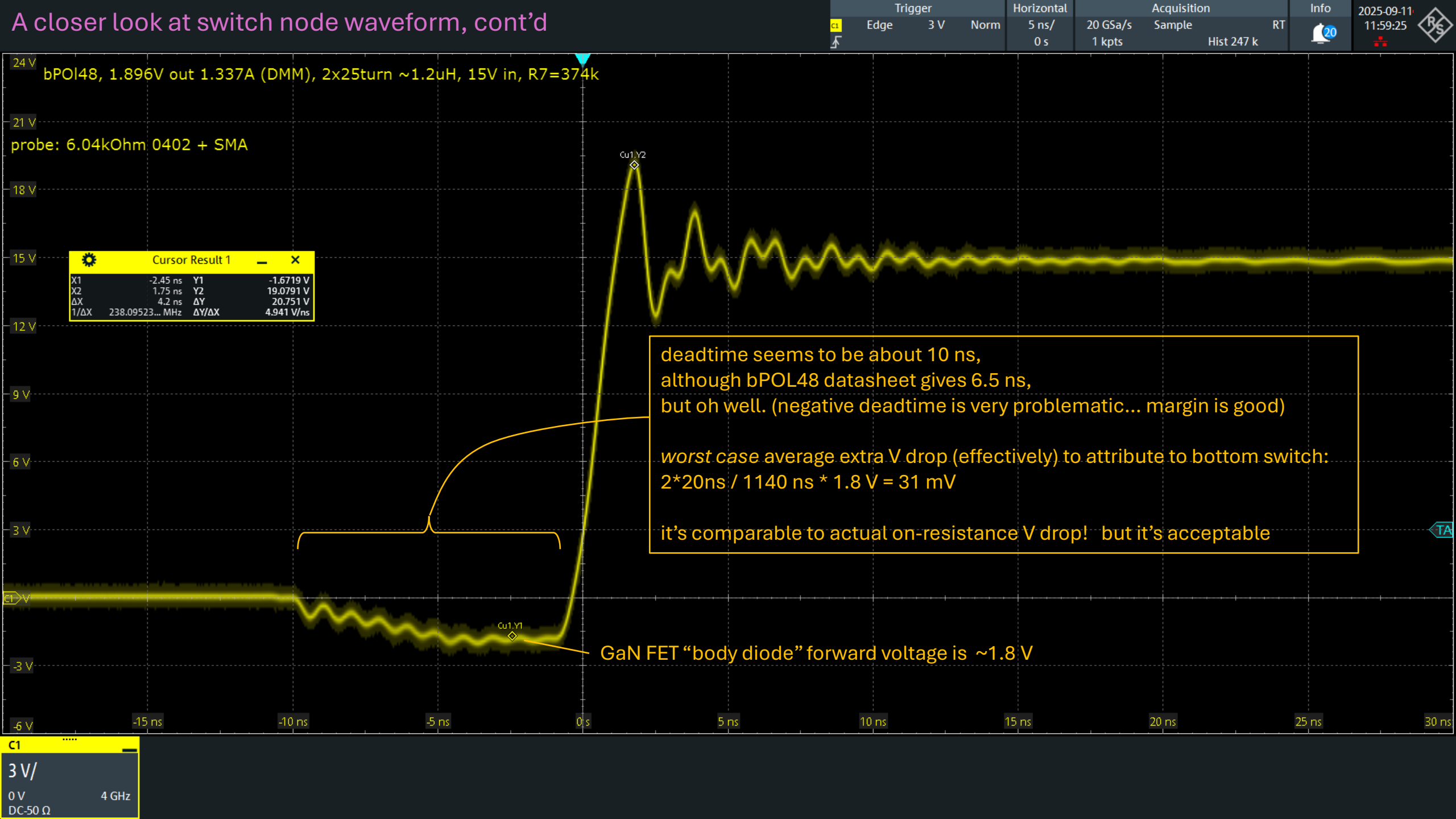
C2: 400 mA/ 0 A 500 MHz DC-1 MΩ inv

A closer look at switch node waveform

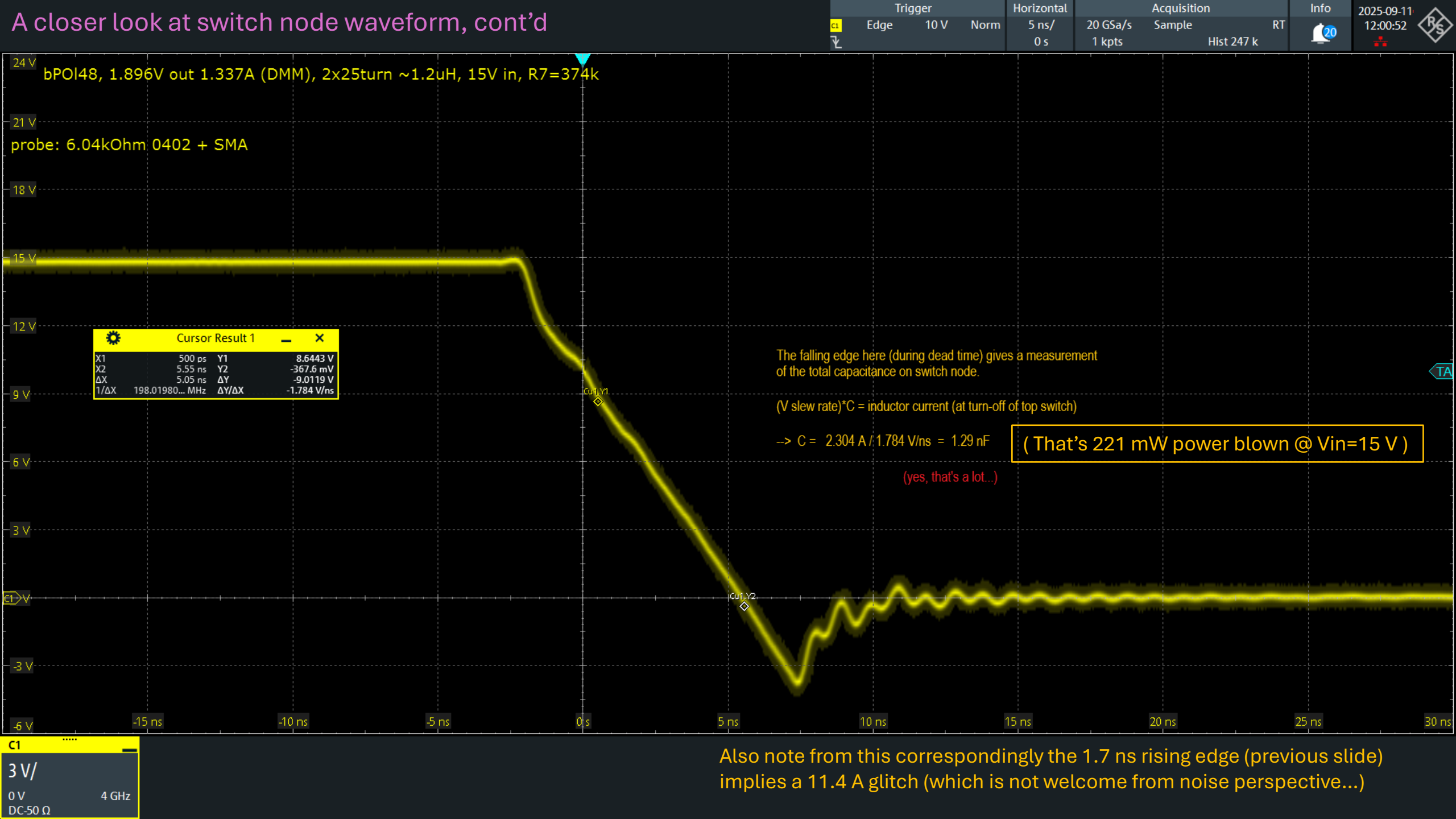


** EPC23104 (newer version of EPC2152) offers a “knob” to address this,
as well as other improvements… (but a bigger package, might not fit, e.g., in TOF application)

A closer look at switch node waveform, cont'd



A closer look at switch node waveform, cont'd



Also note from this correspondingly the 1.7 ns rising edge (previous slide) implies a 11.4 A glitch (which is not welcome from noise perspective...)

Some remarks on efficiency

- FoCalDCDC v2.1.2 layout generally good
  - widely spaced capacitors on input net might be ringing between them (I didn't try to meaure it)
  - switch net on PCB has too much parasitic capacitance to ground; entirely avoidable and this wastes power and increases EMI
  - but it is a nice module design with all I/O on one end, far from switching current paths, probably very good for reducing conducted EMI

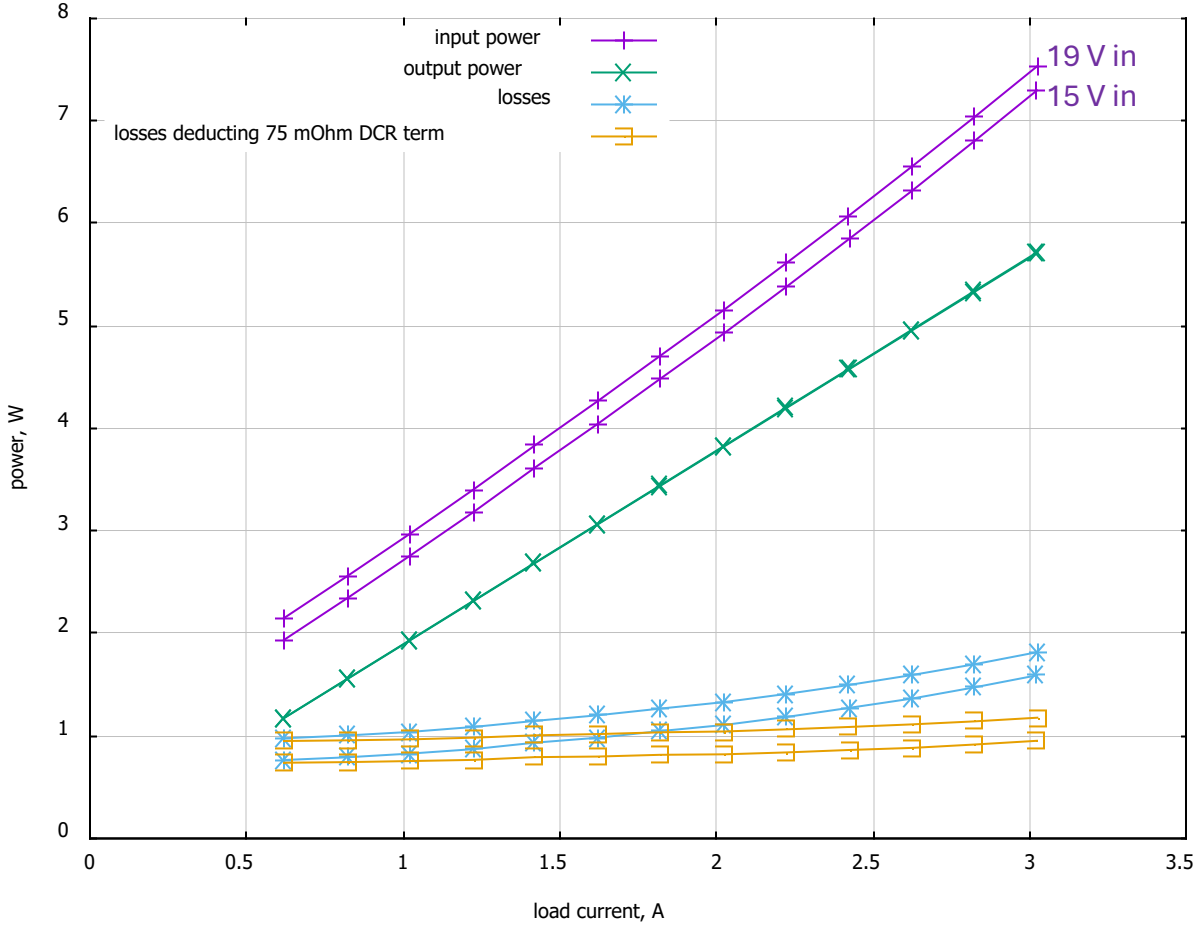
- For low load currents, bPOL48/EPC2152 efficiency suffers greatly from "background" losses (chip supply currents, gate charge, switch node charge, ripple current losses)
  - *The FET's are 4 – 5× too large! Operate at lowest reasonable frequency!* (DCR of the larger inductor is not a big deal at low current)
  - Consider EPC23104 (half the charge losses, lower I_{SUPPLY} too)
  - With EPC23104, only 5 V supply is needed (bPOL48 can work from 5 V input), so we could maybe power the converter from the output, after startup – significant power savings

- EPC23104 likely has adequate radiation tolerance
  - an all-GAN device (AFAIK) just like EPC2152
  - CERN DC/DC team is already working on testing it, we may hear more about this soon

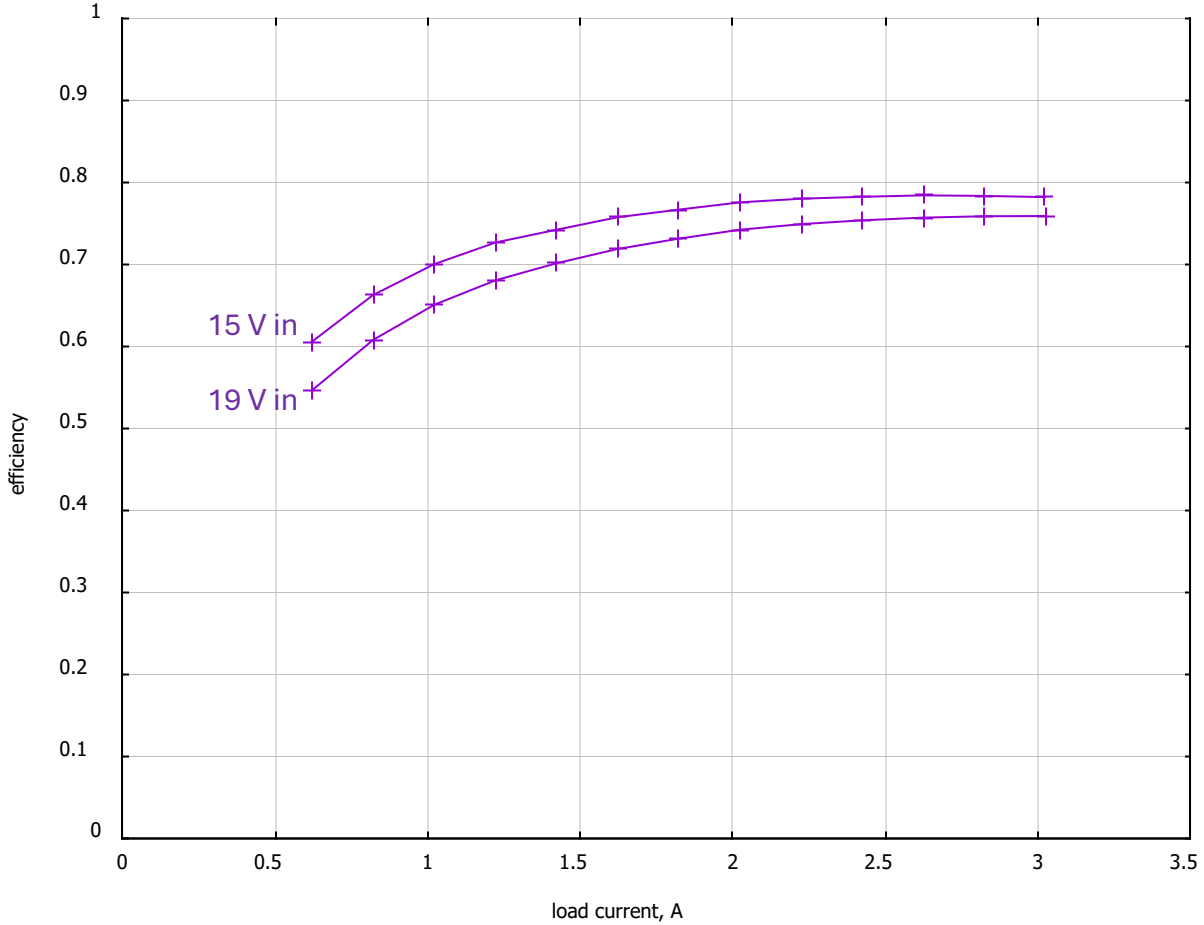
plots for the case of 15 V and 19 V input, 1.8 V output

(Note: voltage drop in input and output filter inductors is excluded here.)

power in, out, and lost



efficiency



75 mΩ DCR losses correspond to FET and inductor specifications.

Other losses are roughly independent of load current ***and are dominant*** here. (Not the way it should be.)

About **0.23 W [0.36 W @ 19 V]** due to switch capacitance, about **0.45 W [0.57 W]** chip supply power.

About **0.19 W [0.21 W]** due to inductor AC ripple I^2R losses.

Noise (EMI)

Despite the PCB layout with large parasitic capacitance on switch node, noise seen at FoCalDCDC v2.1.2 output is reasonably low, if an input filter is implemented.
I added a small output filter too (3 mV drop @ 1.5 A load, probably acceptable).

Switching ripple part of the output noise is good. (Spikes will be further reduced with a better layout, certainly.)

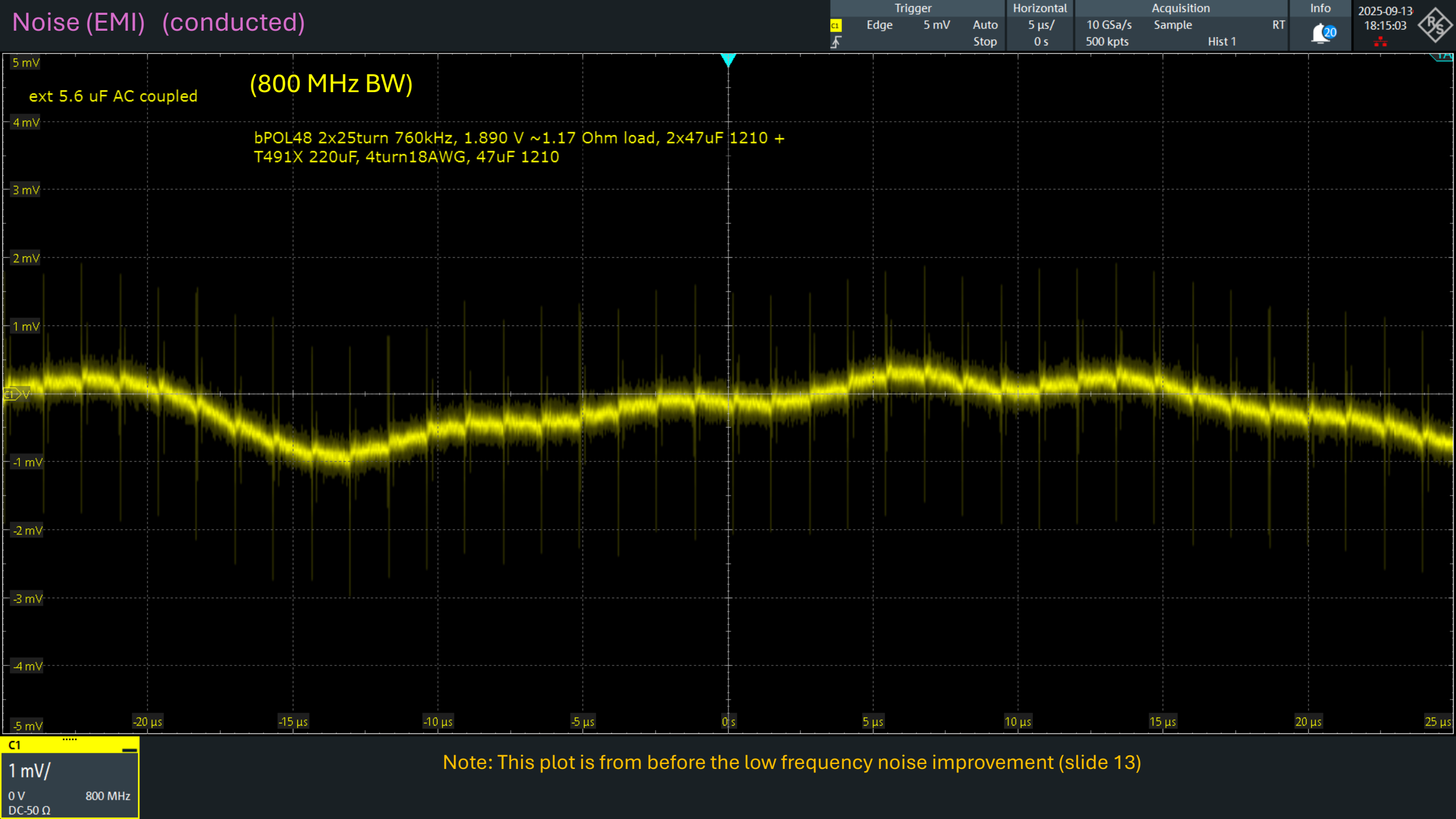
Low frequency part of output noise is not very good. May be tolerable. *Much better performance is seen with some COTS DC/DC chips*.
Sources of low frequency noise:

- Reference voltage into error amplifier – no control over this, fixed in bPOL48 design
- Resonance in buck "filter" – I think that's ruled out, noise peak did not move much upon adding a large tantalum capacitor
- Loop phase margin – yes some improvement possible (see below)
- Noise from large resistor values in feedback – that can't be helped, it is constrained by bPOL48 design

I have not yet looked at "radiated" noise, only conducted noise, which is probably the more significant (for FEMC application at least). Radiated noise measurement is rather subjective anyway.

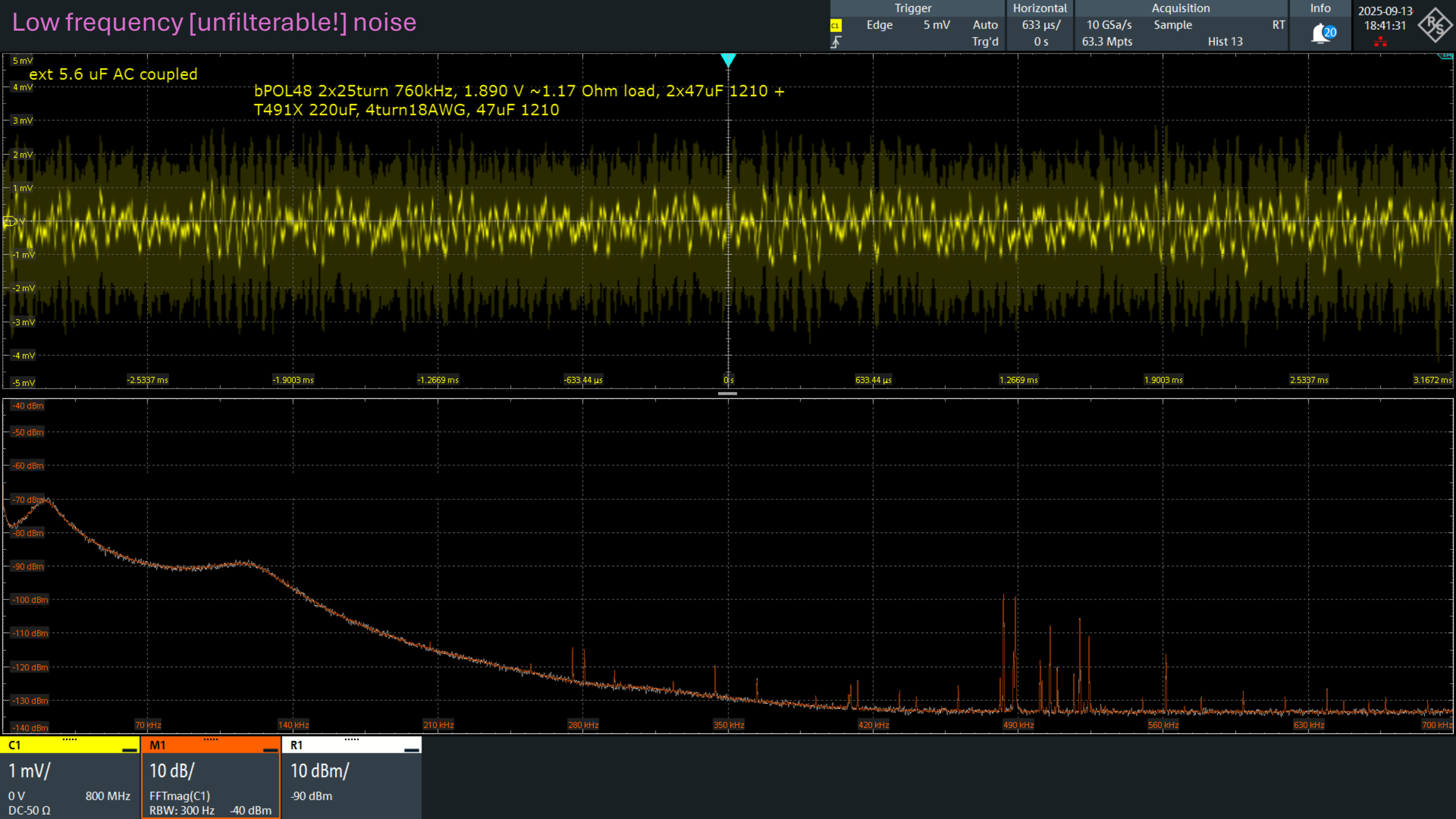
Noise (EMI) (conducted)

Noise (EMI) (conducted)

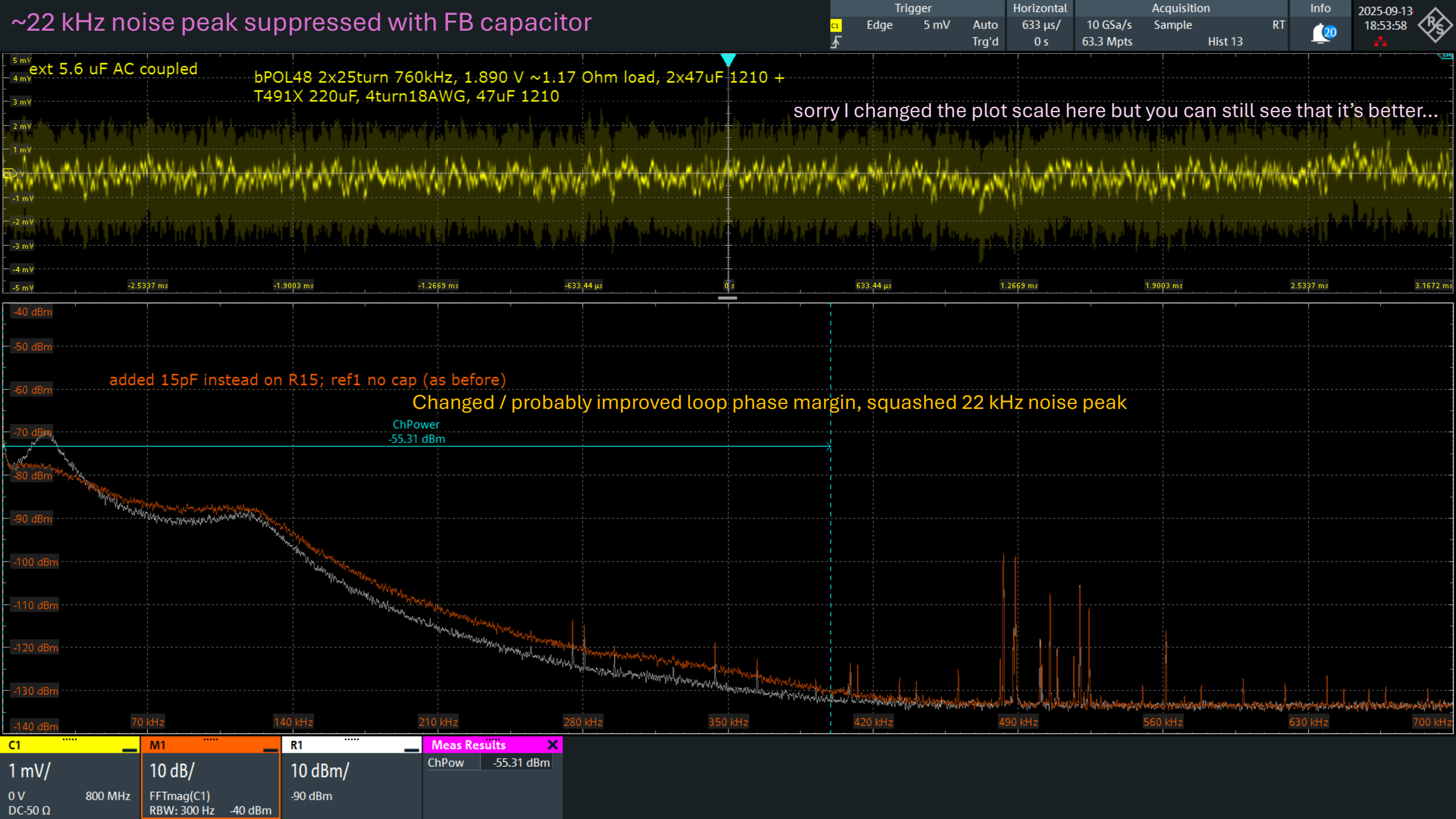


Note: This plot is from before the low frequency noise improvement (slide 13)

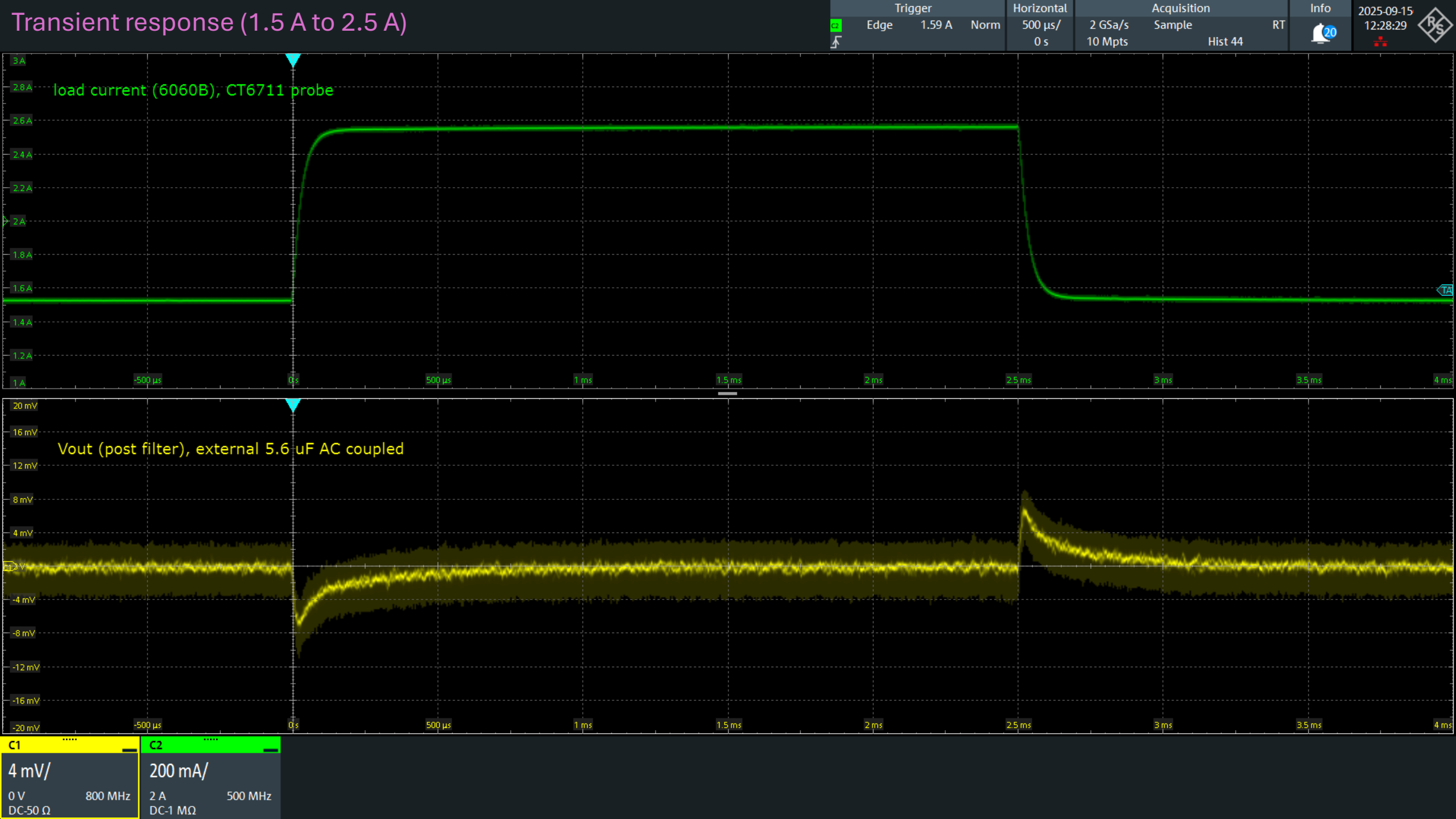
Low frequency [unfilterable!] noise



~22 kHz noise peak suppressed with FB capacitor



Transient response (1.5 A to 2.5 A)



Conclusions

bPOL48 works reasonably well for 15 – 18 V input, 1.8 V ~1.5 A output.

Maybe it can work a little better if EPC23104 can be used instead of EPC2152. Particularly if things can be powered from the output (5 V).

Some optimization work remains for the inductor design, I/O filters, and feedback.

If COTS DC/DC parts can be qualified for radiation, they might still be preferred*

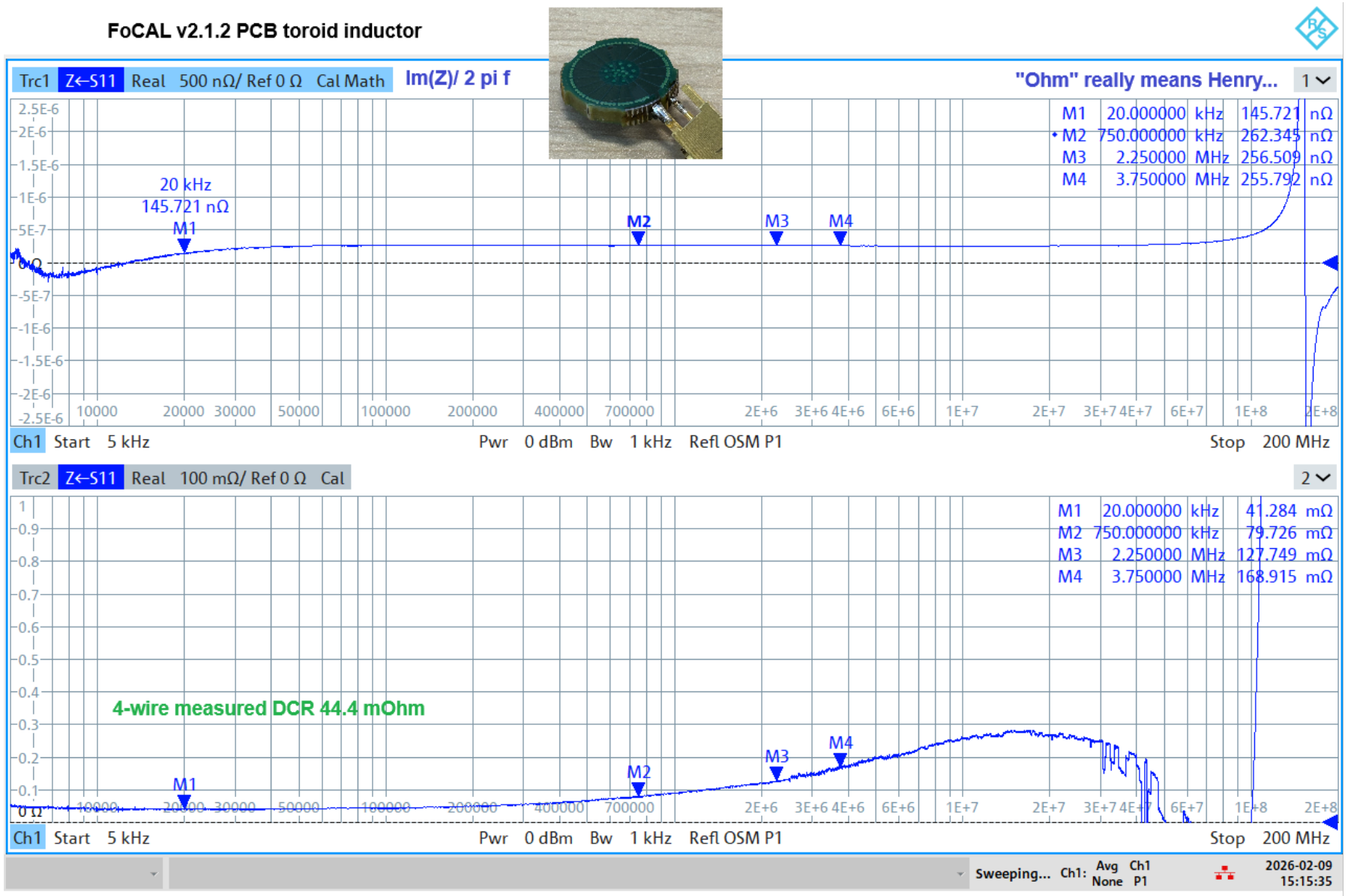
- Lower cost, wider availability
- Lower EMI (lower capacitances)
- Lower low frequency noise!
- Higher efficiency (lower capacitances)

But if they can't – bPOL48 looks pretty reasonable, and we could make it the baseline choice.

FEMC quantities: Likely 2 bPOL48 per FEB (1.8 V and 3.3 V or maybe 5 V, w/ LDO's). 594 FEB installed. Procurement quantity ~2*594*1.1(board spares)*1.15(parts excess) = **~1500 bPOL48's [+ EEEMC ~250 bPOL48's]**

* e.g. LTC3626

2/6/2026 supplement – measuring the PCB toroid inductor



2/6/2026 supplement – measuring the PCB toroid inductor – sanity check

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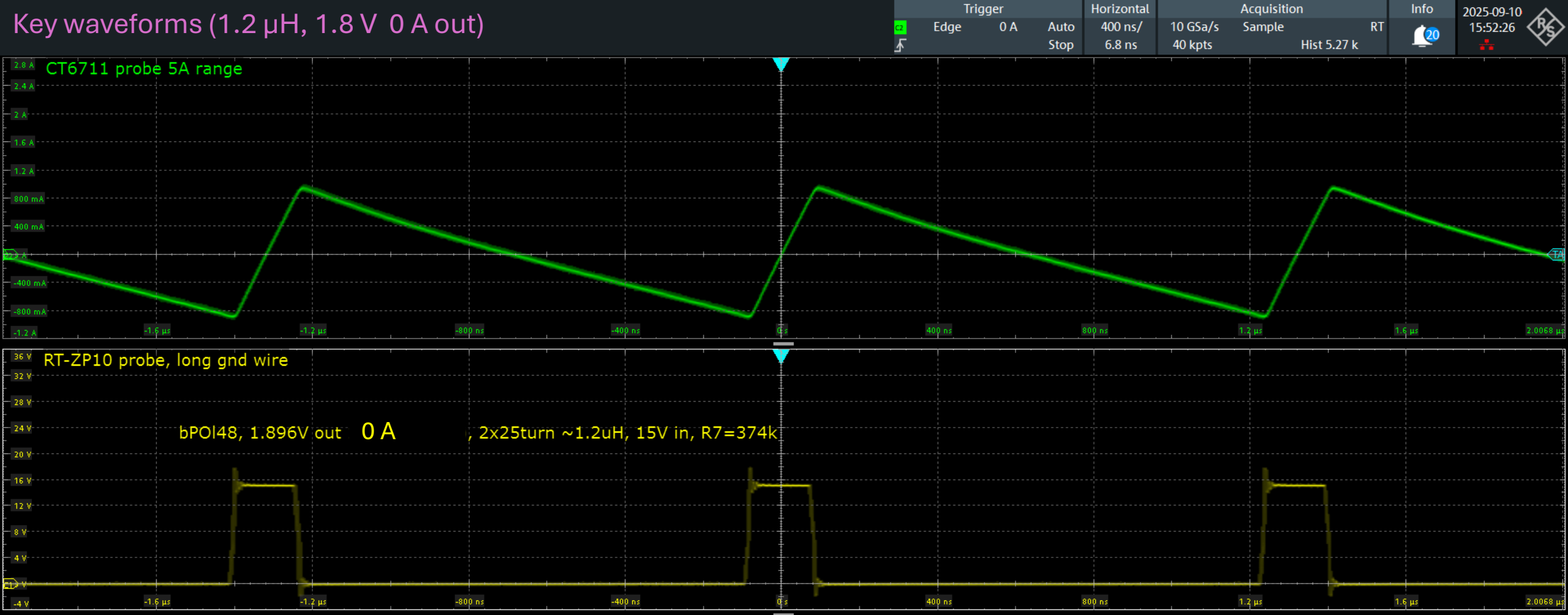
backup

Key waveforms (1.2 µH, 1.8 V 0 A out)



	Current	Max	Min	Mean	RMS	σ (S-dev)	Event count	Wave count
Meas Group 1								
Frequency	758.23 kHz	759.94 kHz	756.43 kHz	758.24 kHz	758.24 kHz	567.75 Hz	1578	1578
Pos. duty cycle	12.541 %	12.781 %	12.473 %	12.619 %	12.619 %	0.048 %	1578	1578
Meas Group 2								
Peak to peak	1.8498 A	1.8972 A	1.834 A	1.8606 A	1.8606 A	9.9996 mA	1578	1578
Cycle mean	-35.573 mA	31.35 mA	-62.993 mA	-17.474 mA	22.146 mA	13.61 mA	1578	1578
Cycle RMS	523.72 mA	525.87 mA	521.28 mA	523.18 mA	523.18 mA	630.83 µA	1578	1578

Statistics: Reset

C1 4 V/ 0 V 500 MHz DC-1 MΩ 10:1

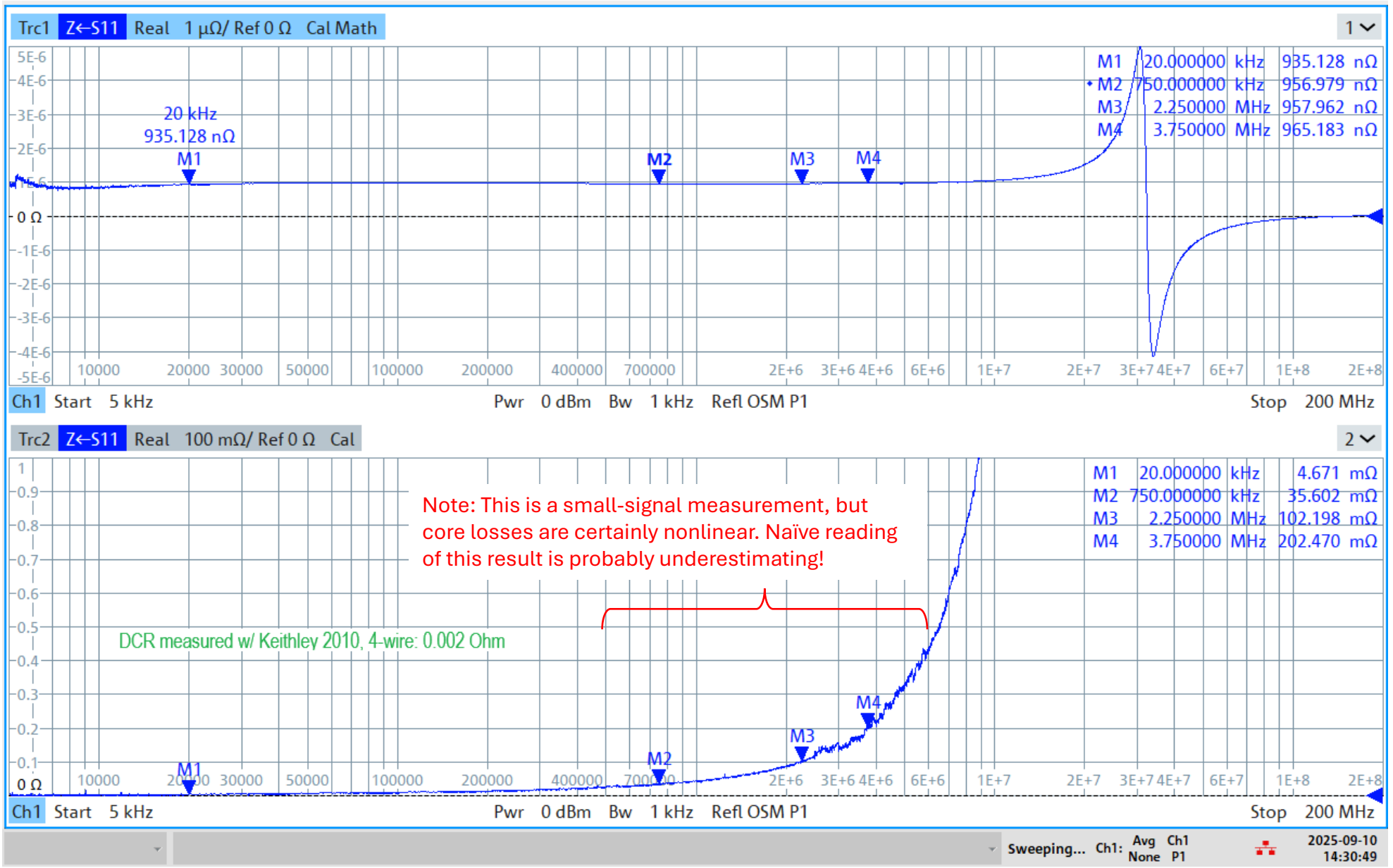
C2 400 mA/ 0 A 500 MHz DC-1 MΩ inv

Control waveforms and deadtime

Later I changed R8, R9 to 18.2 kΩ (was 47 kΩ).
Still plenty of deadtime.
Didn’t make any significant efficiency improvement though (at 1.8 V ~1.5 A).

FoCalDCDC stock 1 µH inductor (COTS, powder core, probably it is Kemet # MPX1D1264L1R0)

the (unknown P/N) powder core 1uH inductor that was on the board originally



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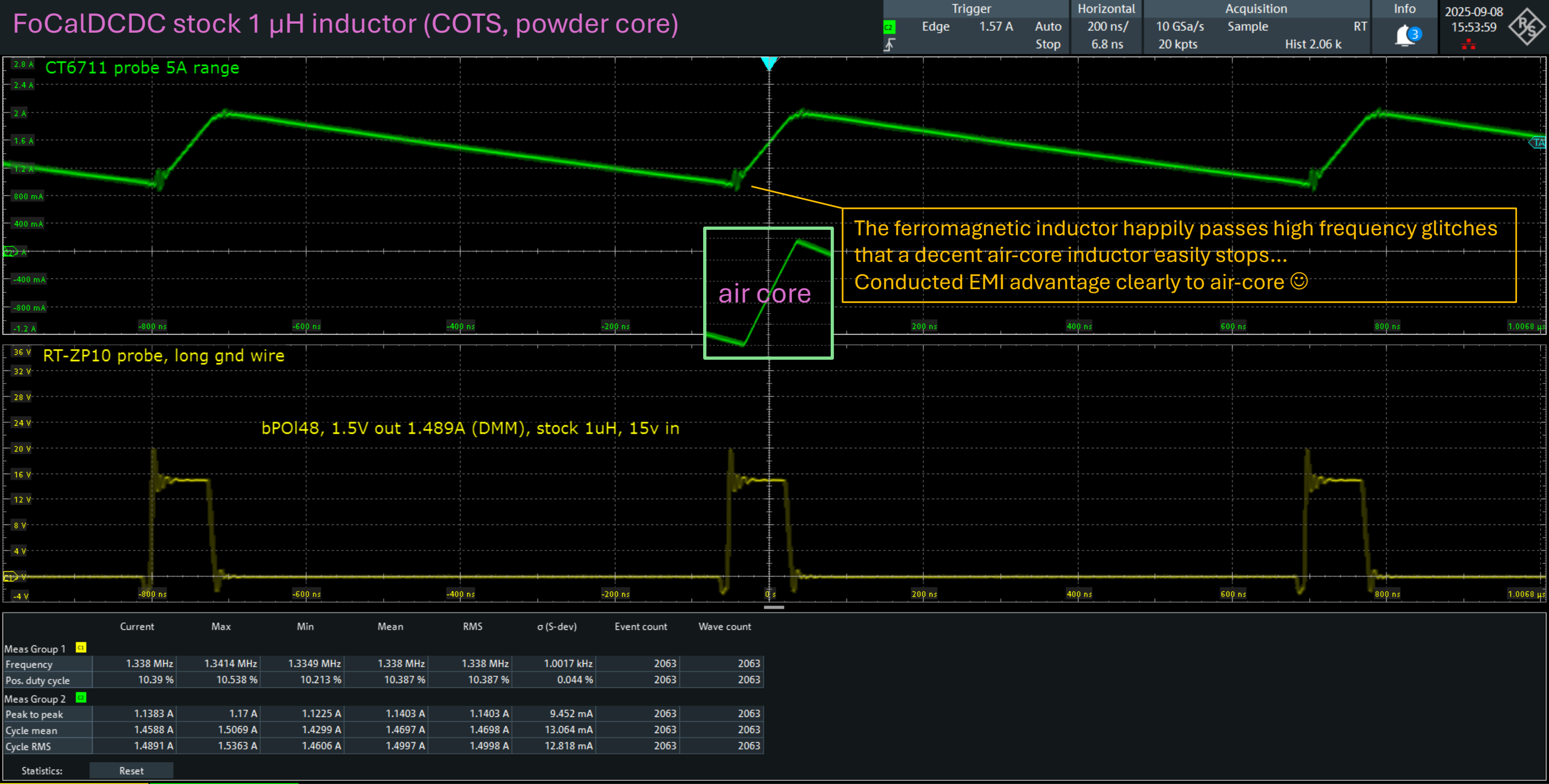
FoCalDCDC stock 1 µH inductor (COTS, powder core)



	Current	Max	Min	Mean	RMS	σ (S-dev)	Event count	Wave count
Meas Group 1								
Frequency	1.338 MHz	1.3414 MHz	1.3349 MHz	1.338 MHz	1.338 MHz	1.0017 kHz	2063	2063
Pos. duty cycle	10.39 %	10.538 %	10.213 %	10.387 %	10.387 %	0.044 %	2063	2063
Meas Group 2								
Peak to peak	1.1383 A	1.17 A	1.1225 A	1.1403 A	1.1403 A	9.452 mA	2063	2063
Cycle mean	1.4588 A	1.5069 A	1.4299 A	1.4697 A	1.4698 A	13.064 mA	2063	2063
Cycle RMS	1.4891 A	1.5363 A	1.4606 A	1.4997 A	1.4998 A	12.818 mA	2063	2063

Statistics: Reset

C1 4 V/ 0 V 500 MHz DC-1 MΩ 10:1

C2 400 mA/ 0 A 500 MHz DC-1 MΩ inv

FoCalDCDC, GV modifications

Default settings:
R1 and R3 not populated: the PGOOD signal is monitored by the DCB.
R2 and R4 not populated: the ENABLE signal is controlled by the DCB.

PGOOD = 1.18 V at Vo 1.50 V

Venable = 1.18 V for 18 V input.

EN_LINREG_XX have internal pullups. Mount pulldown to disable.

24k pulldown delays the enable of the regulator until Vin is around 14V (the internal pullup is 500k). This sets an effective UVLO at Vin=14V.

If the PGOOD signal is to be monitored, it must be pulled up on the DCB! In this case R1 and R2 is DNP!

A voltage above 800 mV applied to the Buck_En pin to be enabled and start operation.
An embedded 500 kΩ resistor pulls the voltage of the Buck_En pin to GND.

If R2, R4 resistors are not populated, the ENABLE pin must be controlled from the DCB!

Vout_Feed is the feedback of Vout to supply VDD in steady state (so LinPOL48V is only used for startup). For this to work, OutLin must be set to a lower value than Vout.

On my prototype board, Vin has 10 uF 50 V X5R 1210 and then feeds through an inductor to the Vin connection pad at edge of the FoCalDCDC board. Solenoid ~0.16" diameter, 7 turns 24 AWG.

VIN: min 13V ... max 48V
Conversion ratio (VIN/Vo): 2 ... 20
Possible output voltages: 1.5V; 2.75V; 5.0V;

VIN: 13V ... 30V

C1, C4 removed

These "removed" components do not exist in layout even. That confused me for a while...
Fine, no problem.

274k
475k
open
37.4k

R7 stock was 200k (30D code)
installed 383k for 800kHz target, got 737kHz
18.2k
then 374k, got 761kHz
leave it so
18.2k

Rf	fsw [MHz]
270k	1.03
200k	1.35
180k	1.48
160k	1.65
130k	1.99
100k	2.51
82k	2.98

R8,R9 18.2k as above, but it didn't make a significant difference.
Tu go slightly larger maybe 22.1k next time.

IC1
EN_LinReg5V
EN_LinReg12V
EN_Buck
PGOOD
RF
R_delayLS
R_delayHS
INV_ENABLE
DIS_EXT_DELAY
EN_PRED
PTAT
5V_12V_EPC
BGP_EA
Vdd_D
GND
EP
VIN48V
VDD5V
VDD12V
Vout
VIN_CTRL
OUT_LIN
FB_LIN
DiodeA
DiodeK
SW_Clamp
SW
PWM_HS
PWM_LS
Vi
Vout_S
#NAME?

IG2
VBOOT
VDD
HSin
LSin
VIN
SW
GND
EPC2152

HMK107C7224KAHTE

1.2 uH air-core coil

Additional 2 x 47uF capacitors must be placed on the DCB!

C17, C18 removed

On my prototype board, Vout connects to 2x 47uF 10V X5R 1210
|| 220uF 16V T491X,
then through inductor
~0.23" dia 3.5 turns 18AWG,
then one more 47uF 1210 is the output.

The T491X was a later addition, to check if output was ringing. Made little/no difference, it was not.
Probably good to have anyway though.

If Vo is below 3.3 V the voltage divider R12/R16 is not required.

The resistor between Vout_S and Vi must have a value of 1 MΩ.

Vi: Input voltage of the Error Amplifier. Vi is connected between the 2 resistors (R15 and R17) and the resulting voltage is compared to the internal reference voltage (about 580mV).

Output voltage settings table

Possible output voltages: 1.5V; 2.75V; 5.0V;

Target	R12	R16	R17	Vo
1.5V	0	DNP	619k	1.52V
2.75V	0	DNP	267k	2.75V
5.0V	3.3k	3.3k	301k	5.01V

for 1.8V output
zero
open
475k
open

15 pF cap on R15
(maybe 12 pF would be better)

Idea to try later: Since pin 12 provides higher frequency feedback, maybe pin 11 feedback can come all or just in part from load side of an output filter inductor, getting better regulation. Try.

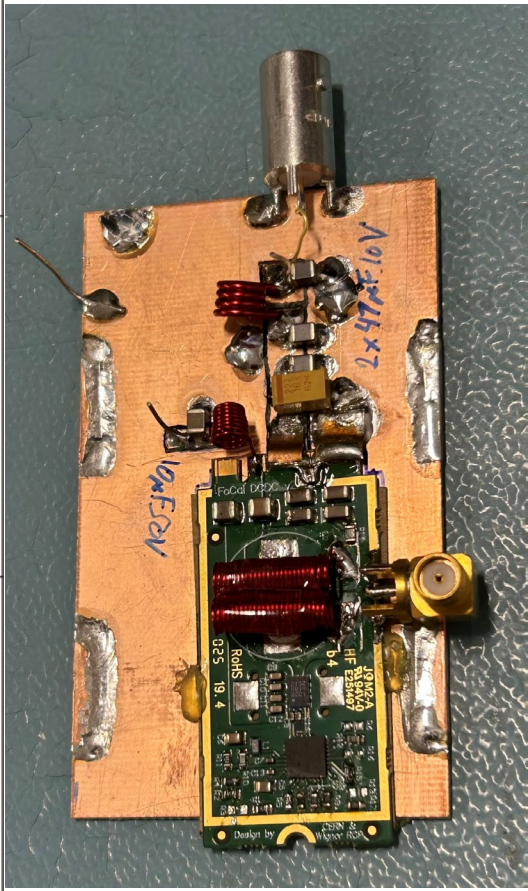
Signals and supplies monitoring

U1
ENABLE
PGOOD
VDD
PTAT
BGP_EA
Vdd_D
VIN
Vo
GND
MOUNTING-HOLE
M.2-B-KEY

Mechanical

FTG1
FTG2
FTG3
TB1

Test points



Wigner RCP Budapest, Hungary	Title: ProjectMainTitle FoCalDCDC v2.1		
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GAN chips compared

EPC2152 – ePower™ Stage IC

V_{IN}, 80 V

I_{Load}, 15 A V_{CC} = 12 V

Electrical Characteristics						
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply						
I_{DD_Q}	Off state total quiescent current	HS_{IN} /LS_{IN} = 0 V, V_{DD} = 12 V, SW floating		14	21	mA
I_{DD_1MHz}	Total operating current @1 MHz	PWM = 1 MHz, 50% On-Time, includes bootstrap current		25	37	
I_{DD_3MHz}	Total operating current @3 MHz	PWM = 3 MHz 50% On-Time, includes bootstrap current		28	40	
High Side Internal Power FET						
$R_{DS(on)\_HS}$	High side FET $R_{DS(on)}$	I_{LOAD} = +/-10 A, HS_{IN} = 5 V, LS_{IN} = 0 V		10	14.5	mΩ
$V_{HS\_DS\_Clamp}$	High side 3rd quadrant clamp	I_{LOAD} = - 10 A, HS_{IN} & LS_{IN} = 0 V		-2	-2.5	V
I_{LEAK_VIN-SW}	Leakage current (V_{IN} to SW)	HS_{IN} = 0 V, SW = 80 V, SW = 0 V		100	210	µA
C_{OSS_HSFET}	Output capacitance (V_{IN} to SW)	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 0 V		339		pF
Q_{OSS_HSFET}	Output charge (V_{IN} to SW)	HS_{IN} = 0 V, SW = 48 V, SW = 0 V		26		nC
Low Side Internal Power FET						
$R_{DS(on)\_LS}$	Low side FET $R_{DS(on)}$	I_{LOAD} = +/-10 A, LS_{IN} = 5 V, HS_{IN} = 0 V		10	14.5	mΩ
$V_{HS\_DS\_Clamp}$	Low side 3rd quadrant clamp	I_{LOAD} = - 10 A, HS_{IN} & LS_{IN} = 0 V		-2	-2.5	V
I_{LEAK_SW-GND}	Leakage current (SW to GND)	LS_{IN} = 0 V, SW = 80 V		150	310	µA
C_{WELL}	HV well capacitance (SW to GND)	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 48 V		57		pF
C_{OSS_LSFET}	Output capacitance (SW to GND)	LS_{IN} = 0 V, SW = 48 V		396		
Q_{OSS_LSFET}	Output charge (SW to GND)	LS_{IN} = 0 V, SW = 48 V		31		nC

EPC23104 – ePower™ Stage IC

V_{IN}, 100 V

I_{LOAD}, 15 A V_{CC} = 5 V

PRELIMINARY

Electrical Characteristics						
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply						
I_{DRV_Q}	Off State Total Quiescent Current	HS_{IN}/LS_{IN}/SD = 0 V, V_{DRV} = V_{DD} = 5 V, SW floating		10	*TBD*	mA
I_{DRV_100kHz}	Total Operating Current @100 kHz	PWM = 100 kHz, 50% On-Time, includes bootstrap current		14	*TBD*	
I_{DRV_1MHz}	Total Operating Current @1 MHz	PWM = 1 MHz, 50% On-Time, includes bootstrap current		20	*TBD*	
High Side Internal Power FET						
$R_{DS(on)\_HS}$	High Side FET $R_{DS(on)}$	I_{LOAD} = +/-10 A, HS_{IN} = 5 V, LS_{IN} = 0 V		8.7	11	mΩ
$V_{HS\_DS\_Clamp}$	High Side 3rd Quadrant Clamp	I_{LOAD} = - 10 A, HS_{IN} & LS_{IN} = 0 V		-1.5		V
I_{LEAK_VIN-SW}	Leakage Current (VIN to SW)	HSIN = 0 V, V_{IN} = 100 V, SW = 0 V			300	µA
C_{WELL}	HV-Well Capacitance (SW to PGND)	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 48 V		32		pF
C_{OSS_HSFET}	Output Capacitance (VIN to SW)	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 0 V		189		
Q_{OSS_HSFET}	Output Charge (VIN to SW)	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 0 V		15		nC
E_{QOSS_HSFET}	Output Capacitance Stored Energy	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 0 V		0.27		µJ
$E_{ON\_HS\_0}$	Turn-On Switching Energy (HS_FET)	HS Turn-On, SW = 0 V to 48 V, R_{BOOT} = 0 Ω, I_{LOAD} = 10 A		1.5		
$E_{ON\_HS\_1}$		HS Turn-On, SW = 0 V to 48 V, R_{BOOT} = 2.2 Ω, I_{LOAD} = 10 A		2.7		
E_{OFF_HS}	Turn-Off Switching Energy (HS_FET)	HS Turn-Off, SW = 48 V to 0 V, I_{LOAD} = 10 A		0.09		
Low Side Internal Power FET						
$R_{DS(on)\_LS}$	Low Side FET $R_{DS(on)}$	I_{LOAD} = +/-10 A, LS_{IN} = 5 V, HS_{IN} = 0 V		8.7	11	mΩ
$V_{LS\_DS\_Clamp}$	Low Side 3rd Quadrant Clamp	I_{LOAD} = - 10 A, HS_{IN} & LS_{IN} = 0 V		-1.5		V
$I_{LEAK\_SW-PGND}$	Leakage Current (SW to PGND)	LS_{IN} = 0 V, V_{IN} = 100 V, SW = 100 V			100	µA
C_{OSS_LSFET}	Output Capacitance (SW to PGND)	LS_{IN} = 0 V, SW = 48 V		189		pF
Q_{OSS_LSFET}	Output Charge (SW to PGND)	LS_{IN} = 0 V, SW = 48 V		15		nC
E_{QOSS_LSFET}	Output Capacitance Stored Energy	LS_{IN} = 0 V, SW = 48 V,		0.27		µJ
$E_{ON\_LS\_0}$	Turn-On Switching Energy (LS_FET)	LS Turn-On, SW = 48 V to 0 V, R_{BOOT} = 0 Ω, I_{LOAD} = 10A		1.5		
$E_{ON\_LS\_1}$		LS Turn-On, SW = 48 V to 0 V, R_{BOOT} = 2.2 Ω, I_{LOAD} = 10A		2.7		
E_{OFF_LS}	Turn-Off Switching Energy (LS_FET)	LS Turn-Off, SW = 0 V to 48 V, I_{LOAD} = 10 A		0.09		