



Ω MEGA



EICROC update

23 jun 2026

Organization for **M**icro-**E**lectronics desi**G**n and **A**pplications

2 more EICROC1 testboards sent to BNL together with 60 ASICs

EICROC0A/0B/1/1A metal fix gds files sent to TSMC

60 chips of each expected in ~2-3 months

EICROC2 RTL in good progress at Clermont

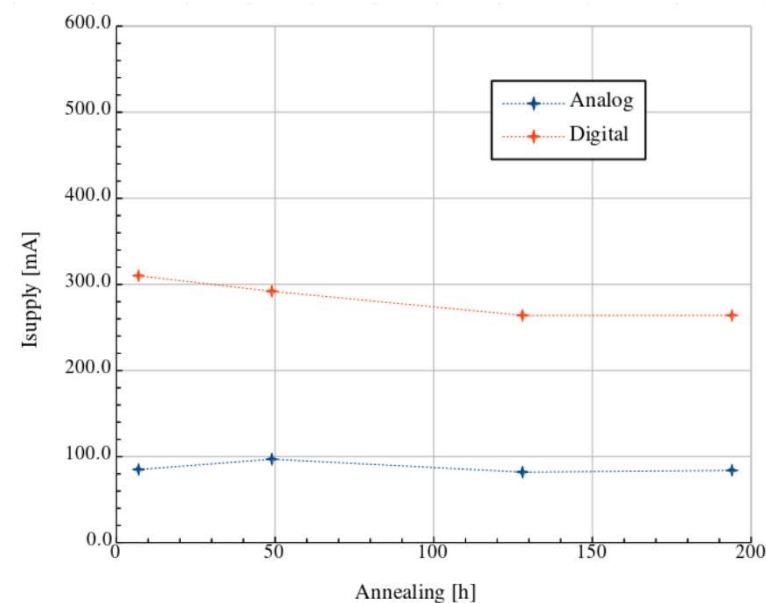
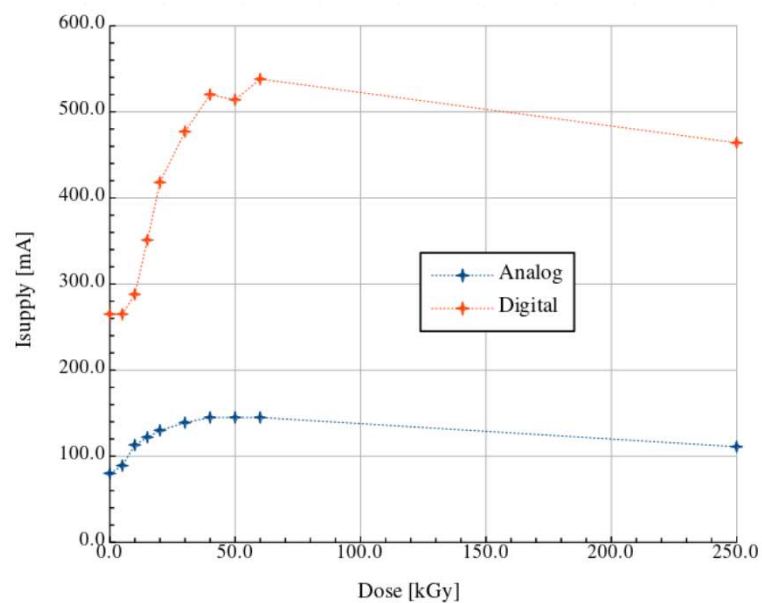
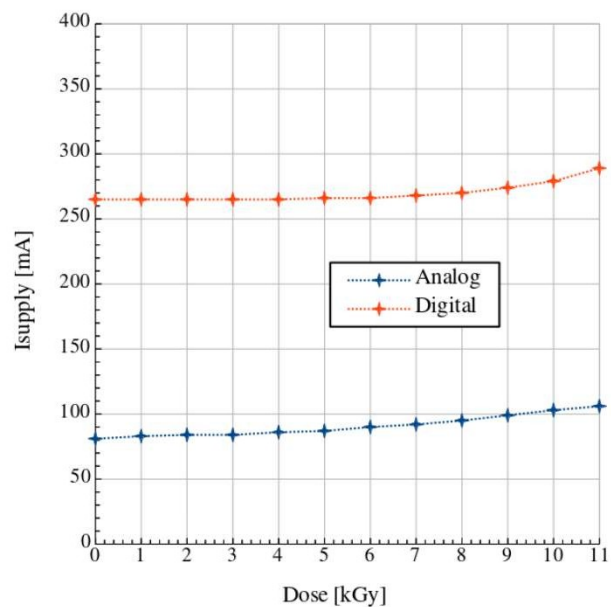
But... just informed that TSMC is abruptly discontinuing 130nm fab...

Fall back solutions under study

Expected radiation levels will be an important input (« 1 Mrad bump »)

TSMC130	TSMC65	UMC110	XFAB130	VIS130
5M 1T 1U RDL C4	5M 2T 1U RDL C4	5M 1T 1U no C4?		As TSMC130
Radhard 200 Mrad	Radhard 200 Mrad	Bump @ 5 Mrad	N/A	Which fab ?
ER : 300 k\$	ER : 750 k\$	ER : 300 k\$?		
EIC	EIC, LHCb	EIC, LHCb, ALICE		
AGH, Lisbon, SLAC	FNAL, BNL, CERN	Torino		
Discontinued	Perenity ?	Low volume	6-9 months fab	Available when ?
	ADC			
DNW, HiR, CMIM	DNW, HiR, CMIM			

- Measured by INFN Torino

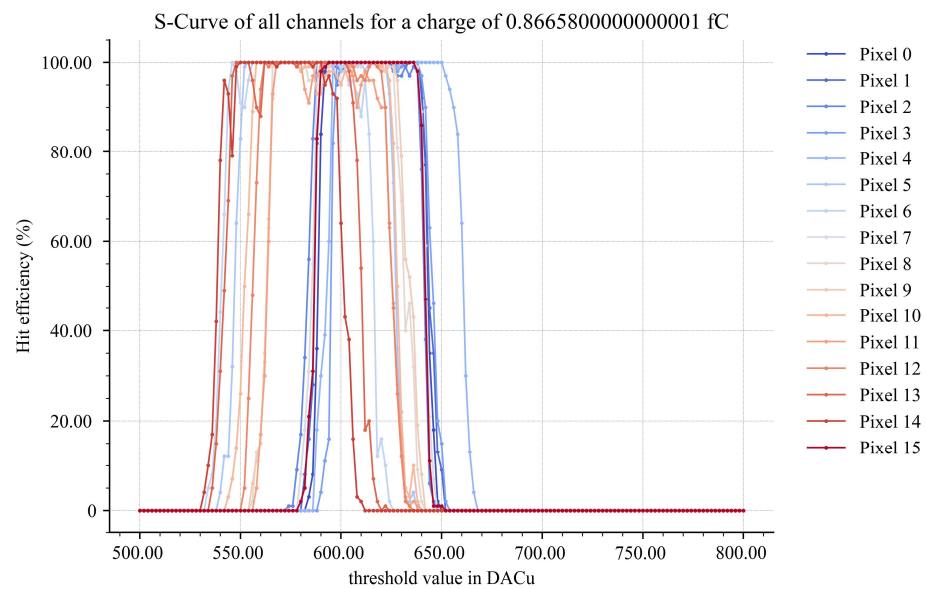


Question(s) asked :

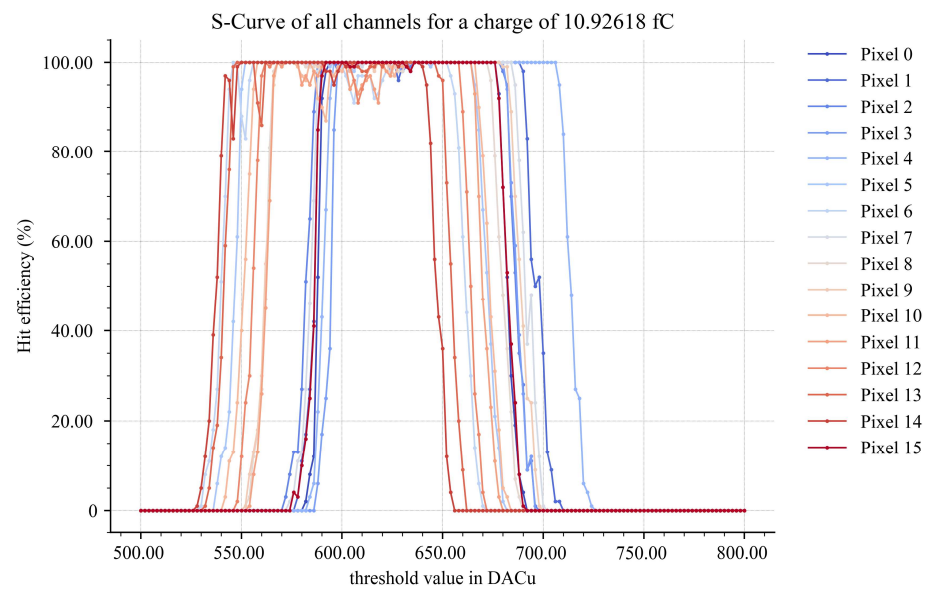
- What is the performance of the card with AC-LGAD?
- **Reminder : slow control bug precludes individual pixel tuning**

Test setup :

- PCB2 : ASIC with wire-bonded AC-LGAD sensor
- Custom debug config : measurements on the 07/04 had no pixel config re-writing after every EoC write, that was fixed on 08/04
- No correction can be done per channel at the moment

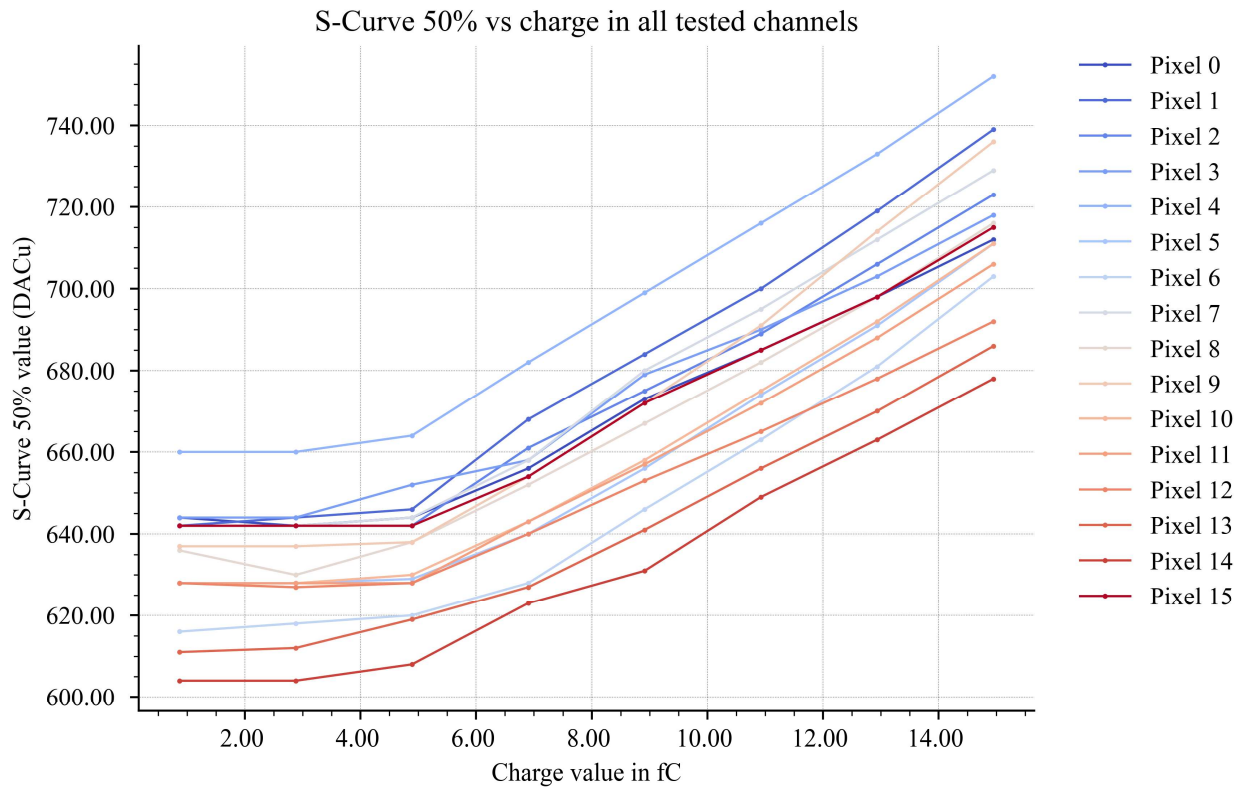


S-Curve with 0 DACu



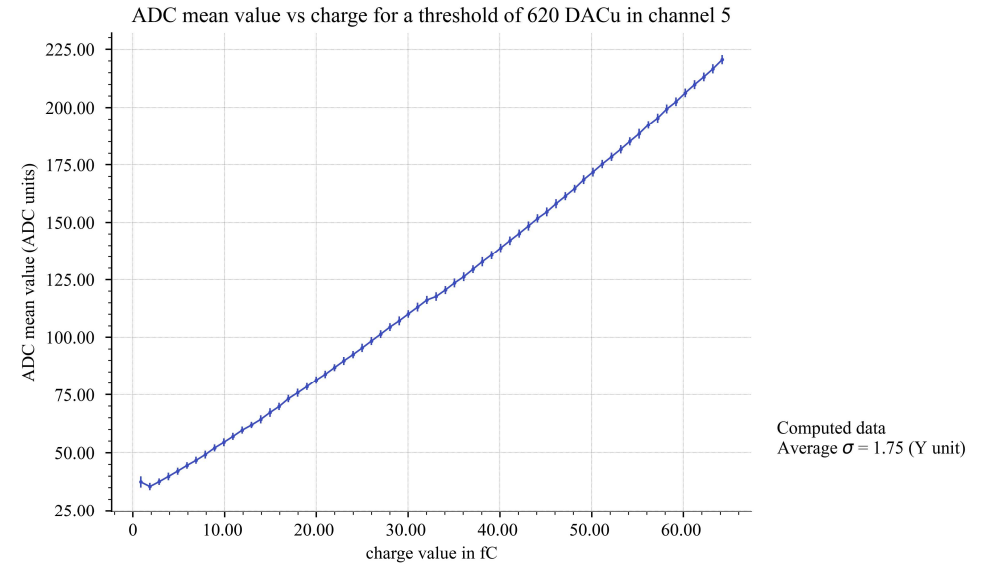
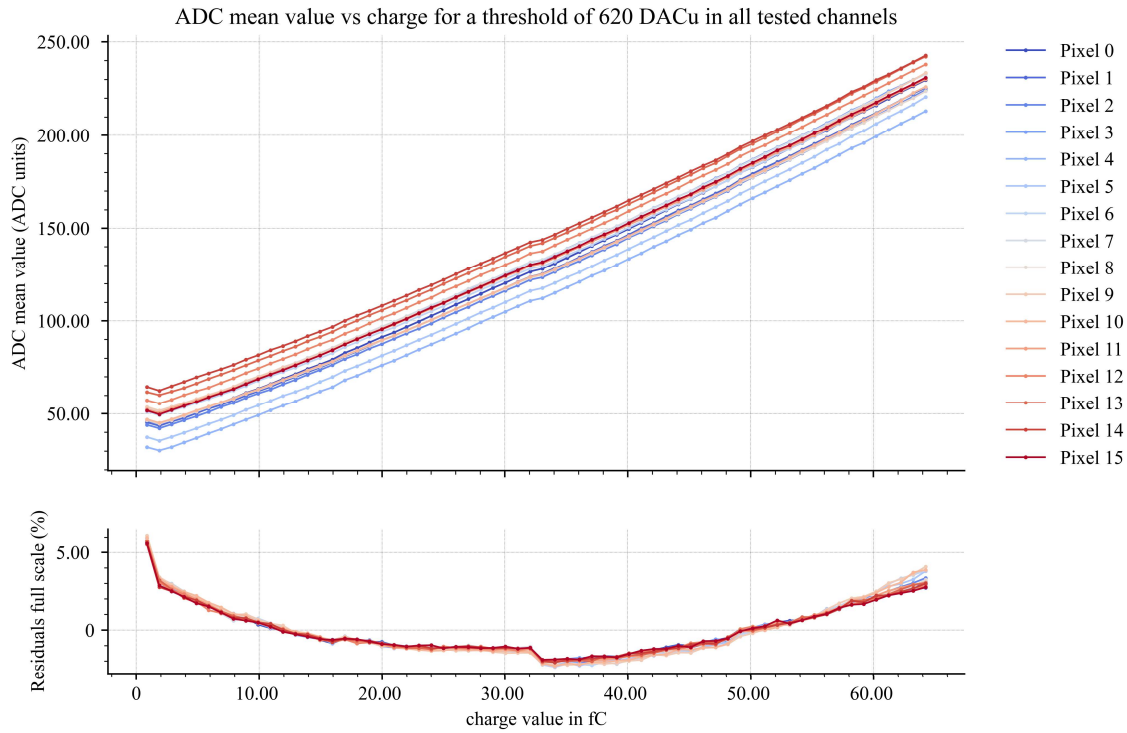
S-Curve with 10 DACu

PCB2 – 22/06/2026 : S-Curve 50% vs charge



Lowest charge detected with discriminator around 5-6 fC. Results are consistent between simultaneous and separate injections.

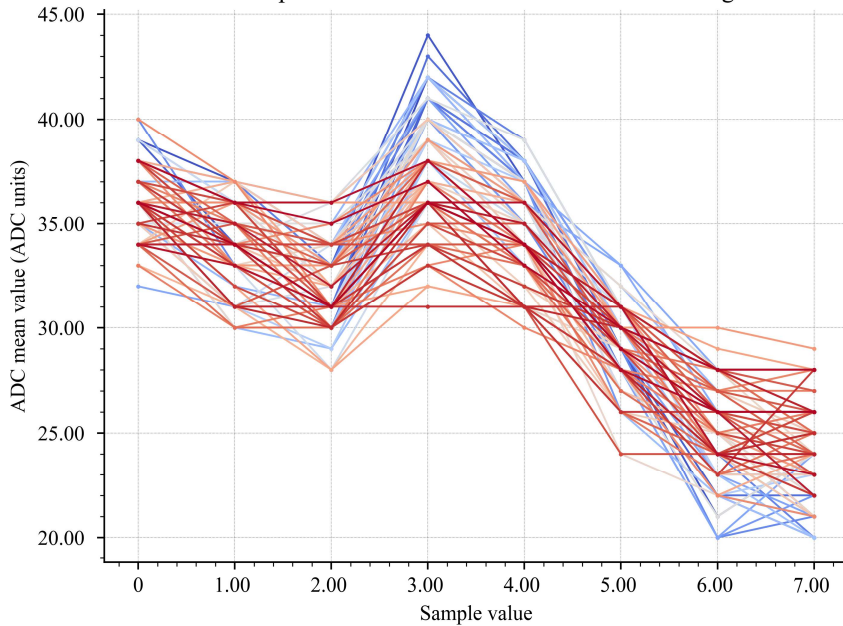
PCB2 – 22/06/2026 : ADC linearity



Zoom on channel 5, RMS of 1.8 ADCu

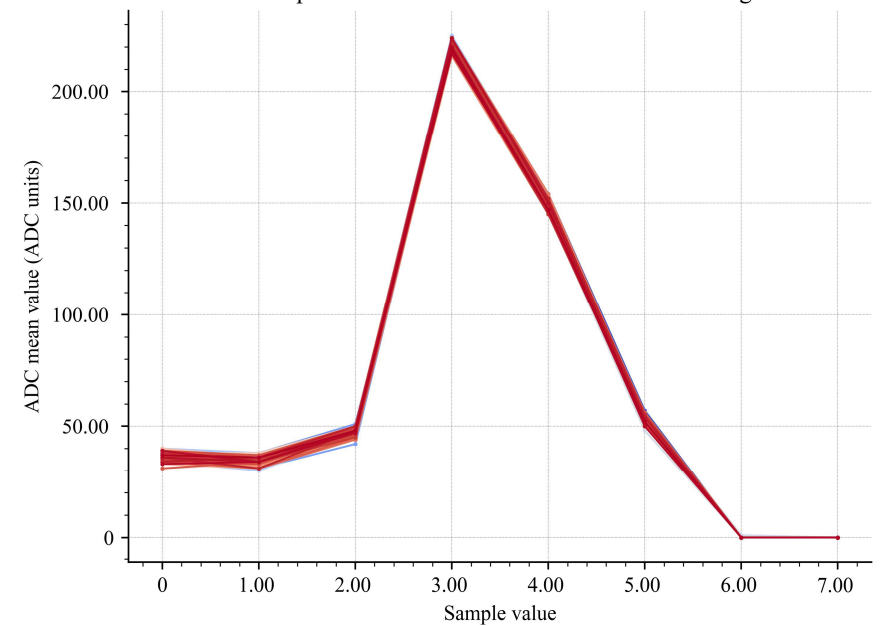
Non-linearity is similar to ASIC alone +
 $c_D = 11$; difference to linear regression
 between +/- 2.5%

ADC mean value vs event samples for a threshold of 620 DACu and a charge of 0.87 fC in channel 5



Signal reconstruction at lowest charge
Same signal as ASIC alone

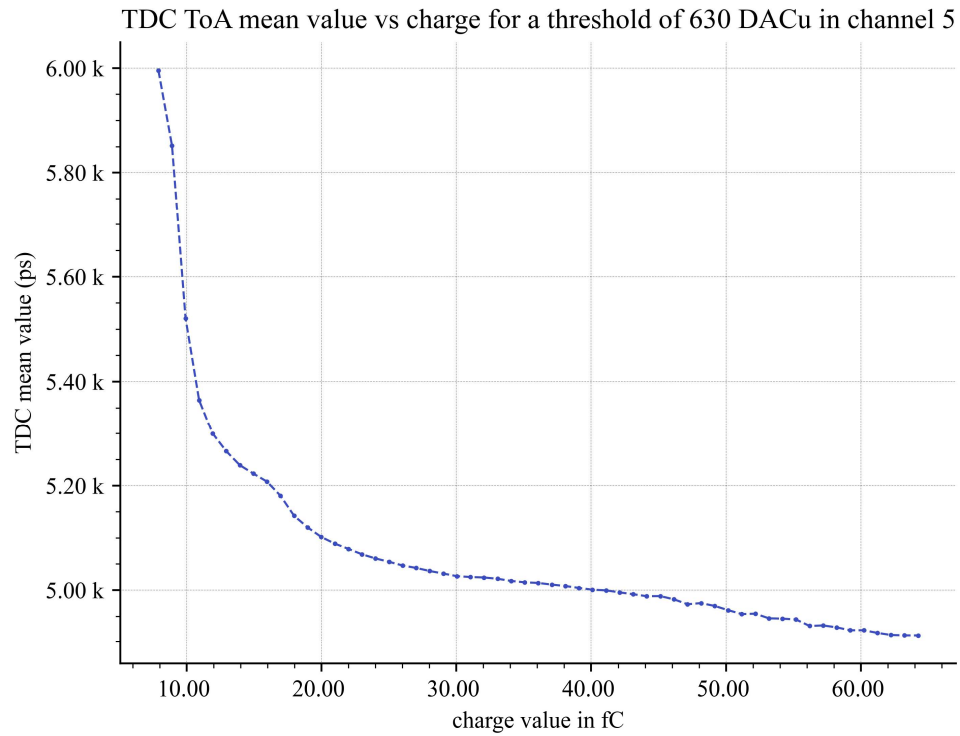
ADC mean value vs event samples for a threshold of 620 DACu and a charge of 64.24 fC in channel 5



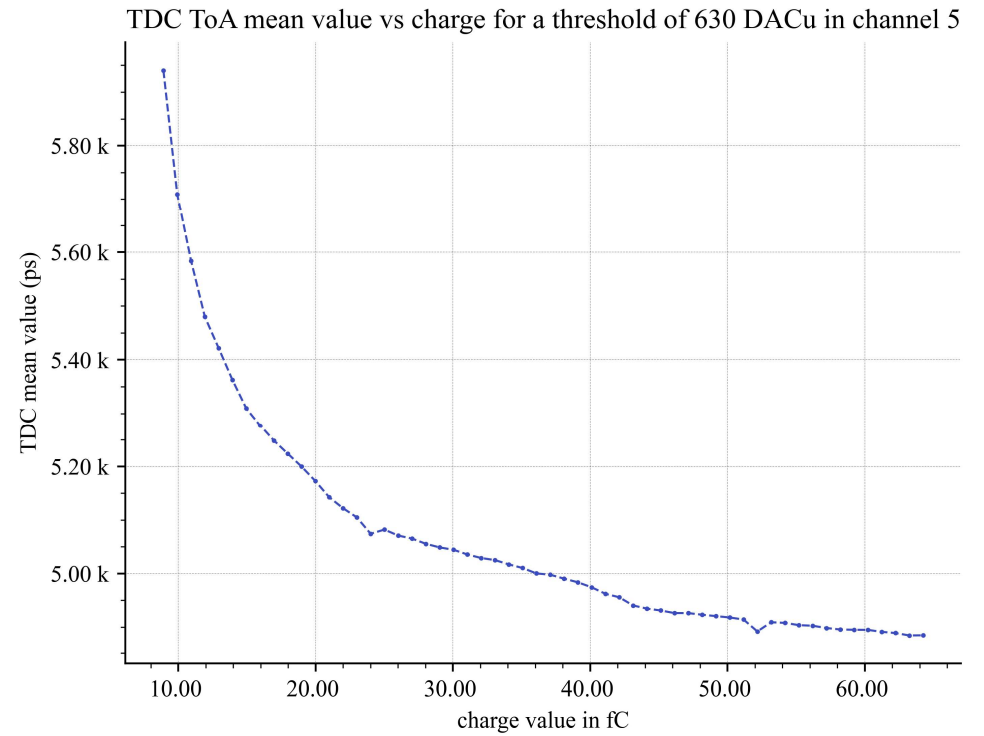
Signal reconstruction at highest charge
Same signal as ASIC alone

Tests done with **no threshold writing** to avoid
ADC signal errors (probably a software issue)

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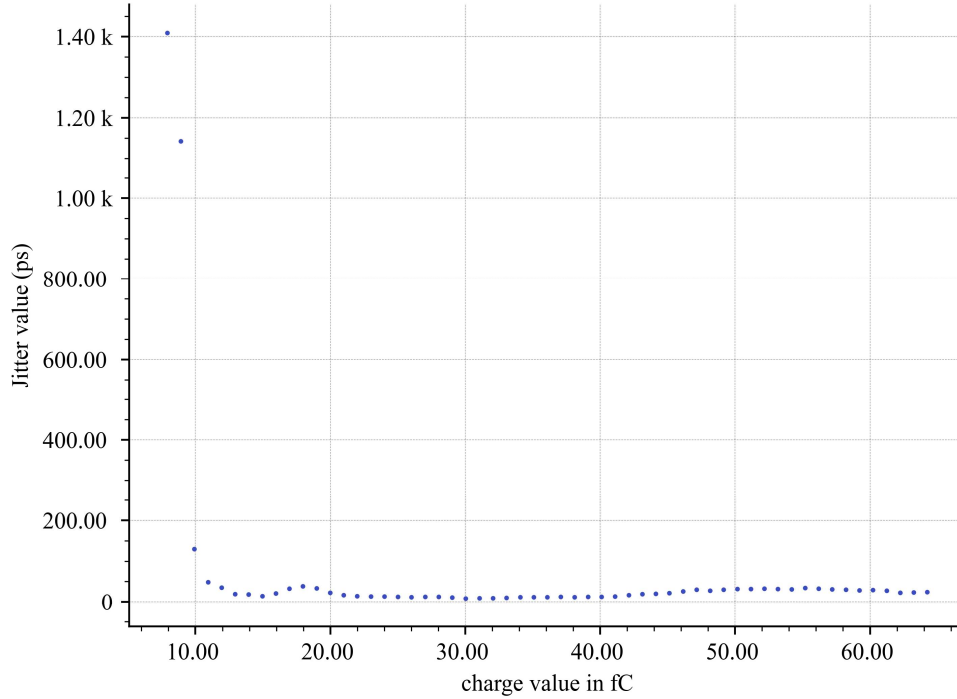


Injection only in channel 5



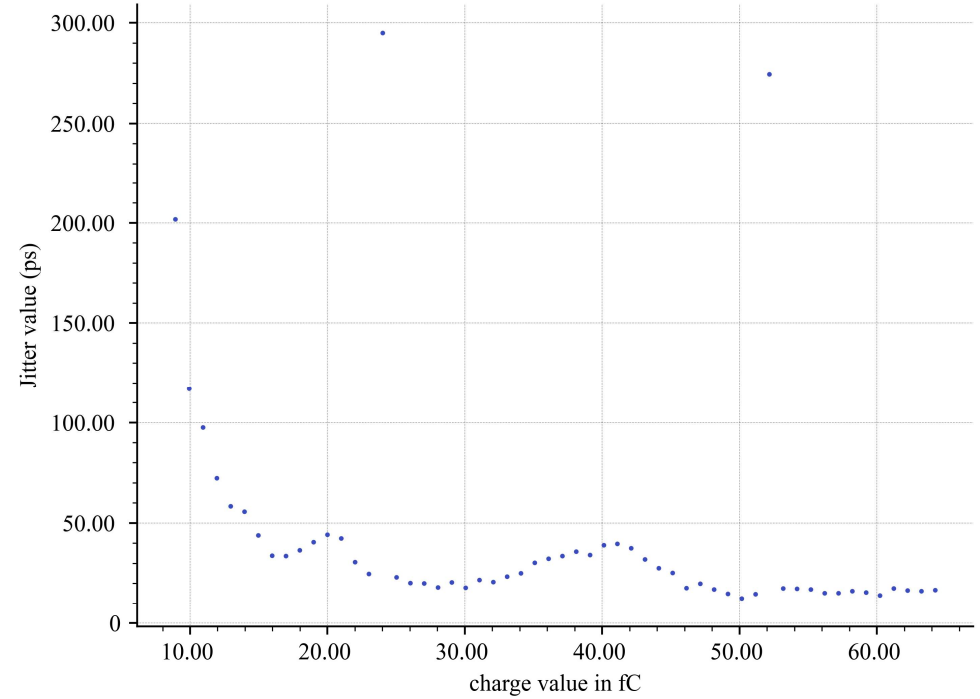
Injection only in channel 5 with all other discriminators disabled
Range is 1 charge value smaller than plot on the left

TDC jitter vs charge for a threshold of 630 DACu in channel 5



Injection only in channel 5

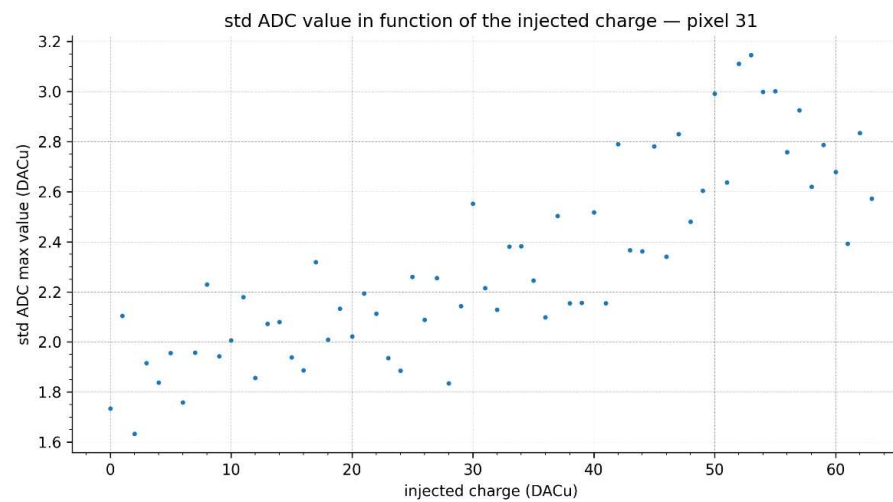
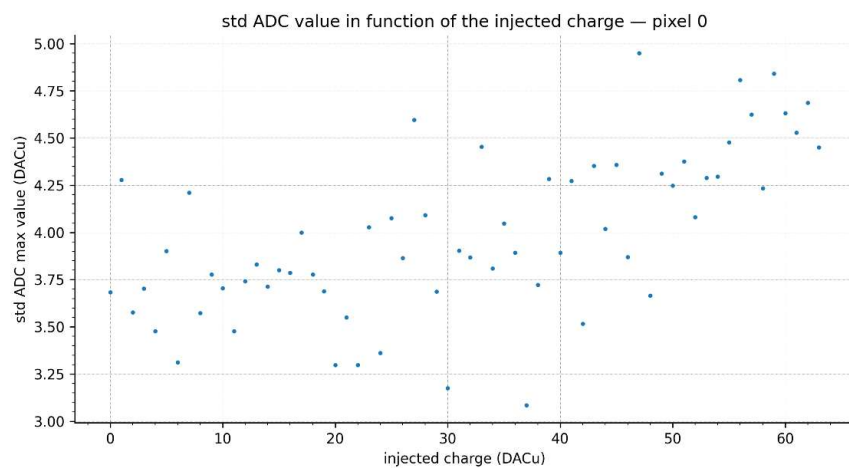
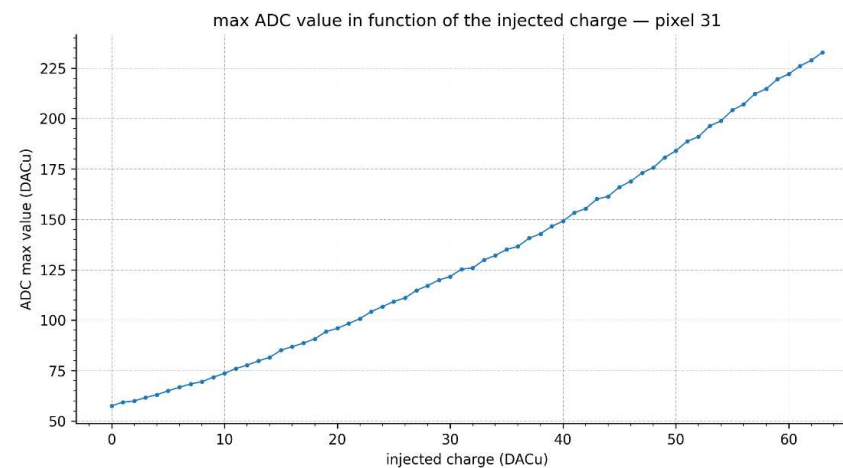
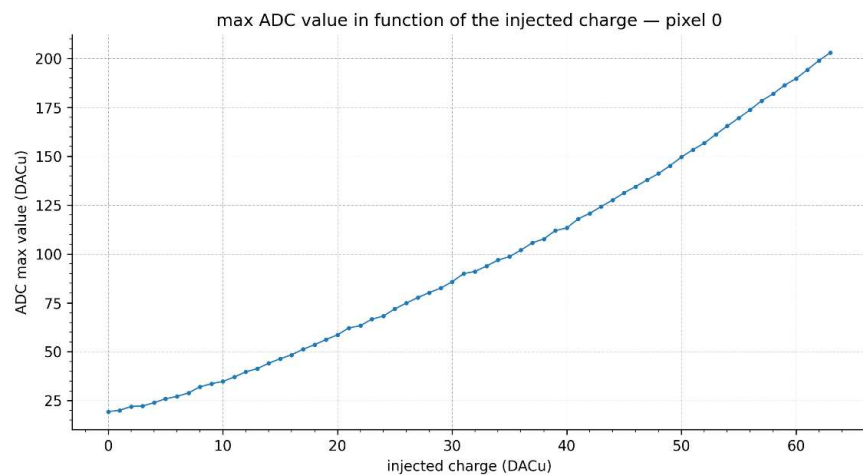
TDC jitter vs charge for a threshold of 630 DACu in channel 5



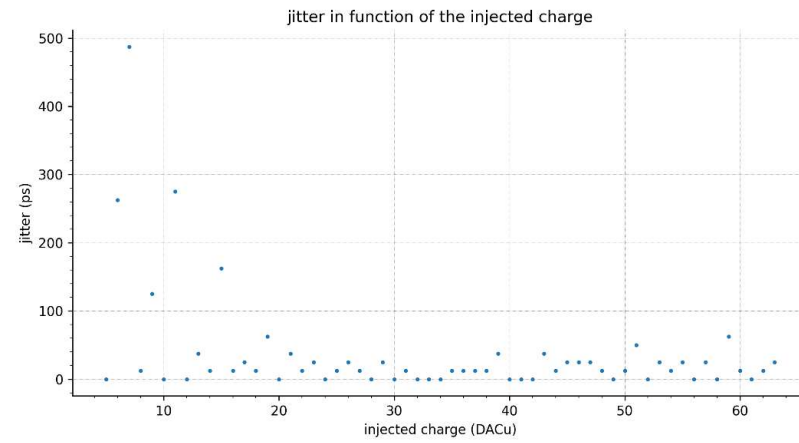
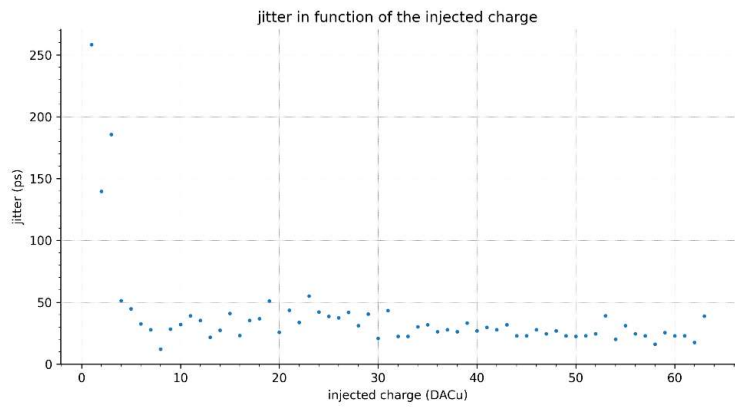
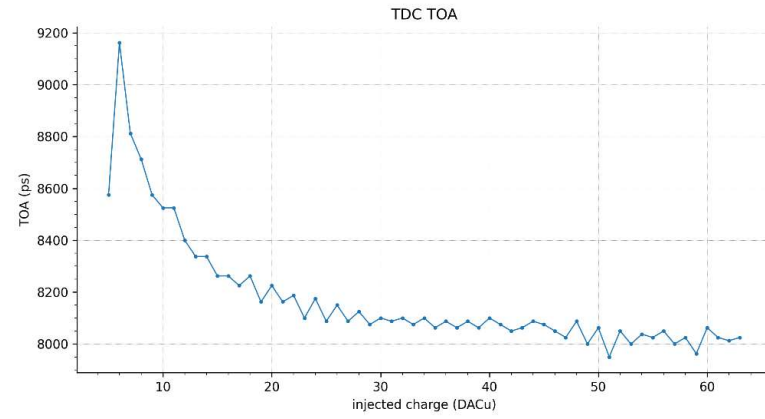
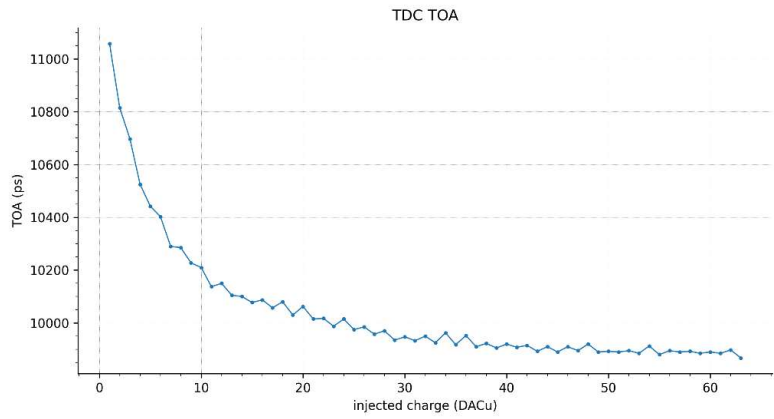
Injection only in channel 5 with all other discriminators disabled

Proper TDC calibration is needed...

EICROC1 linéarity ADC pixel 0 vs 31 [Kinann]

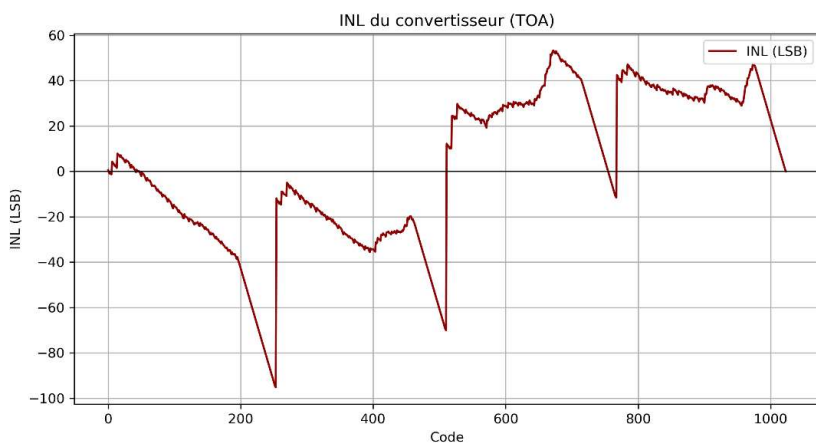
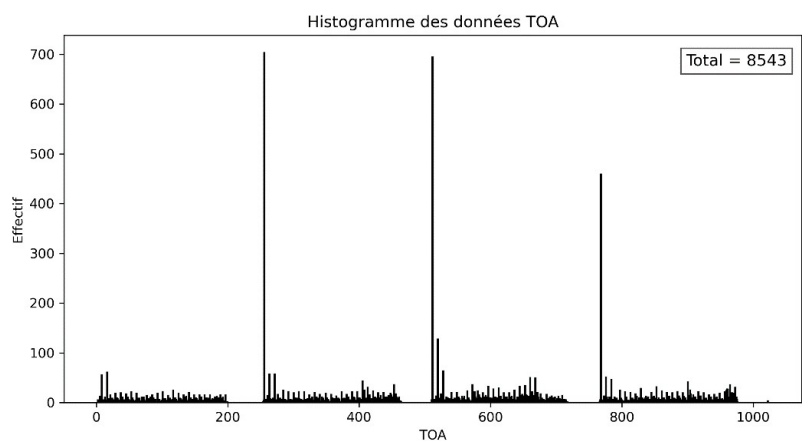


EICROC1 TDC TOA and jitter pixel 0 vs 31

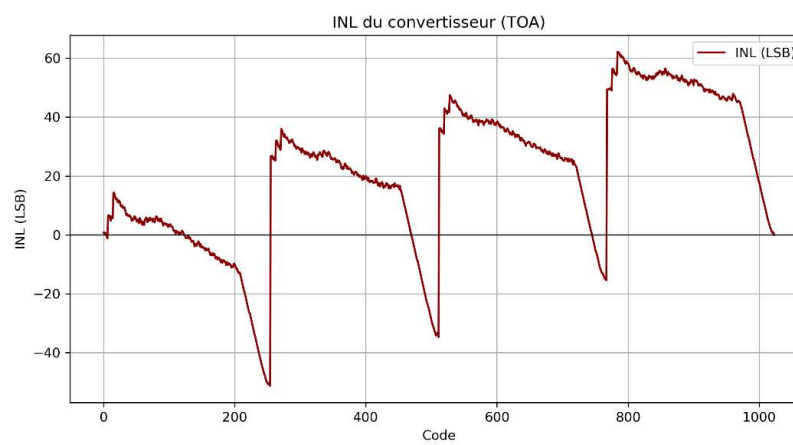
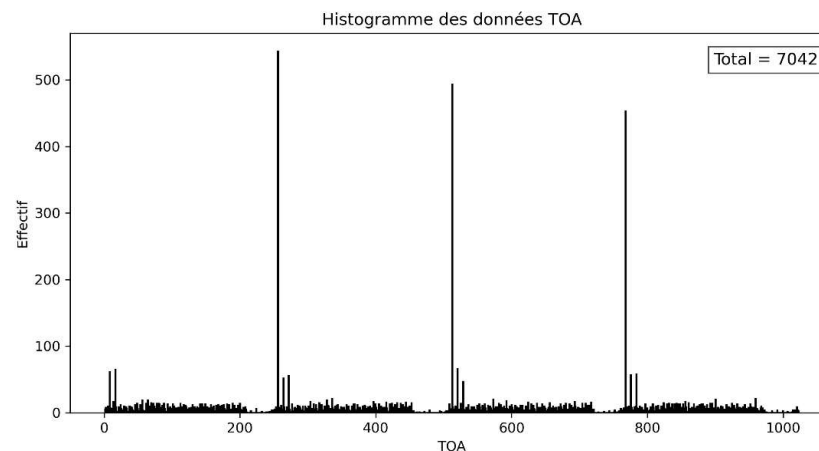


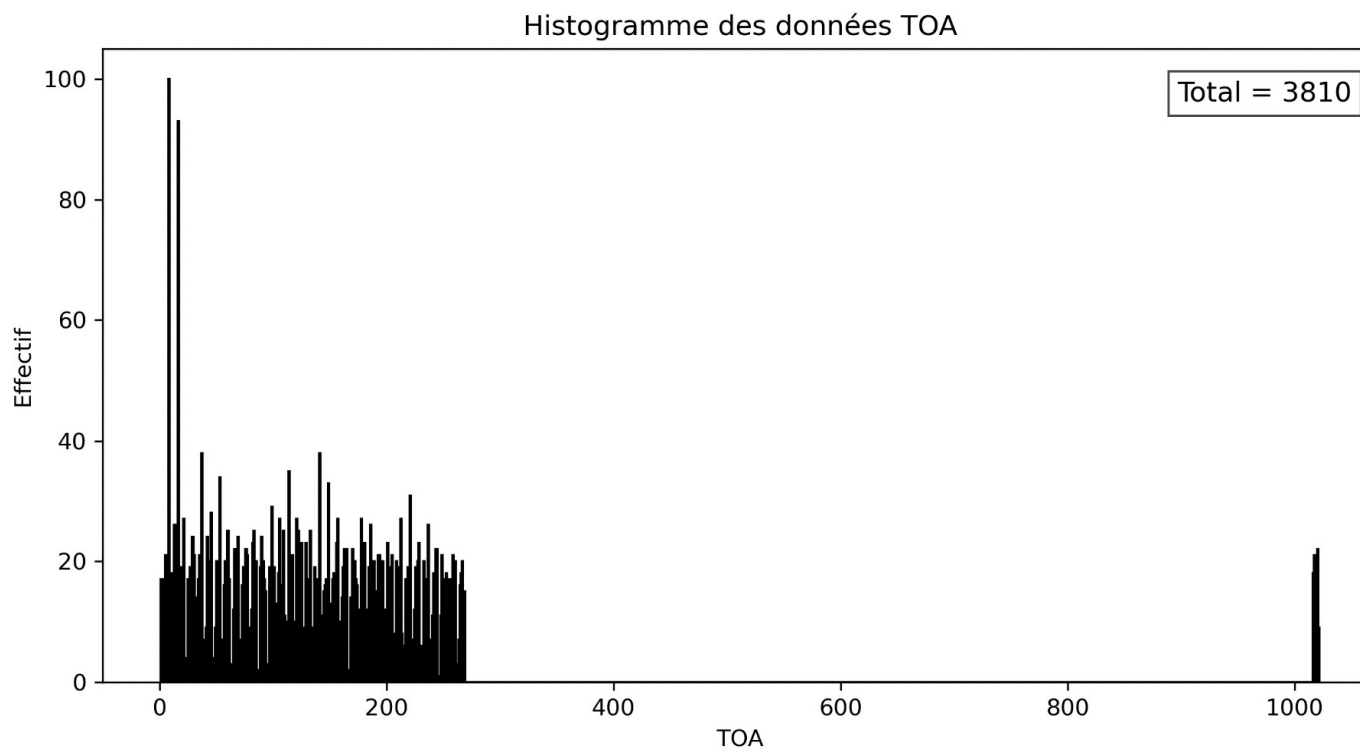
Distribution TOA pixel 0

Config « par défaut » :



Trimming dans le pixel : DAC_CAL_CTDC





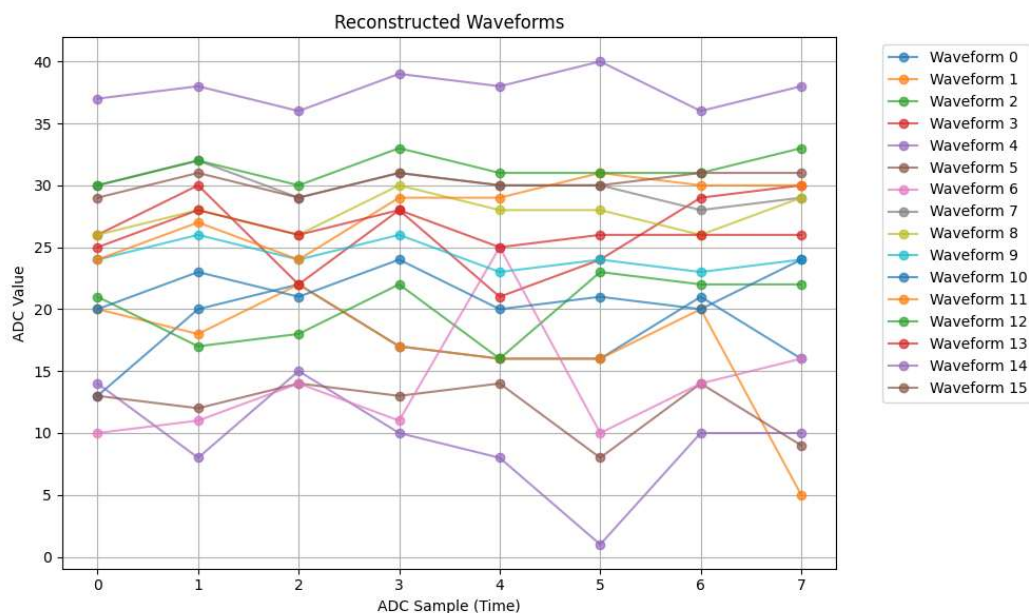
RST_COUNTER = 1

- Continue test bench measurements on EICROC1 ASIC alone
 - Understanding TDC misconfiguration
- Start laser tests with EICROC0A and sensor at IJCLAB
- Study TSMC130 replacement
- Proceed with EICROC2 digital design at Clermont (relatively techno independant)

BACKUP

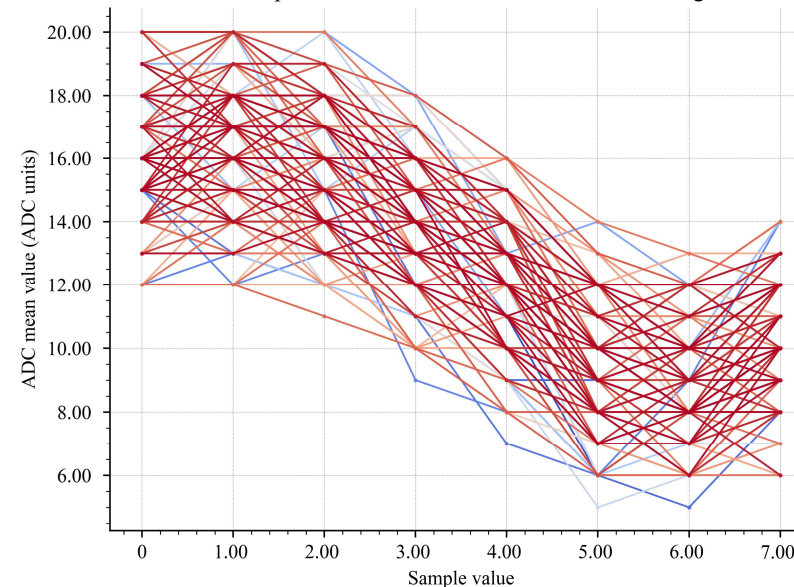
ADC signals

External inj.



Internal Inj.

ADC mean value vs event samples for a threshold of 400 DACu and a charge of 0.87 fC in channel 0



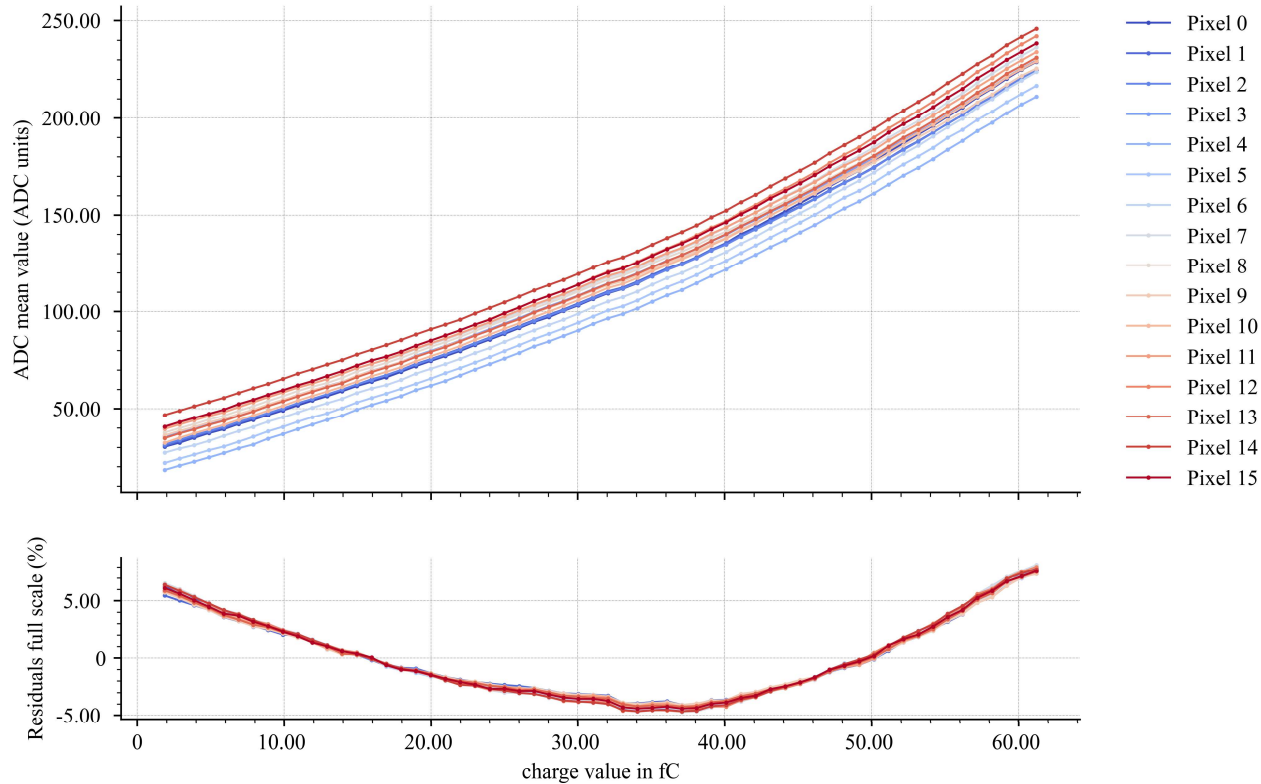
Test with external injection used no command pulse, **no c_{test} was wired to the front ends.**

Internal injection was obtained with FPGA cmdpulse, **no c_{test} was wired to the front ends** and 0 DACu as input charge.

Only 1 event could be captured with the external injection, but the waveform doesn't show the linear decreasing behavior seen in the plot with the internal injection. We might be seeing some internal cmdpulse interference in the signal?

ADC linearity (all channels injected sim.)

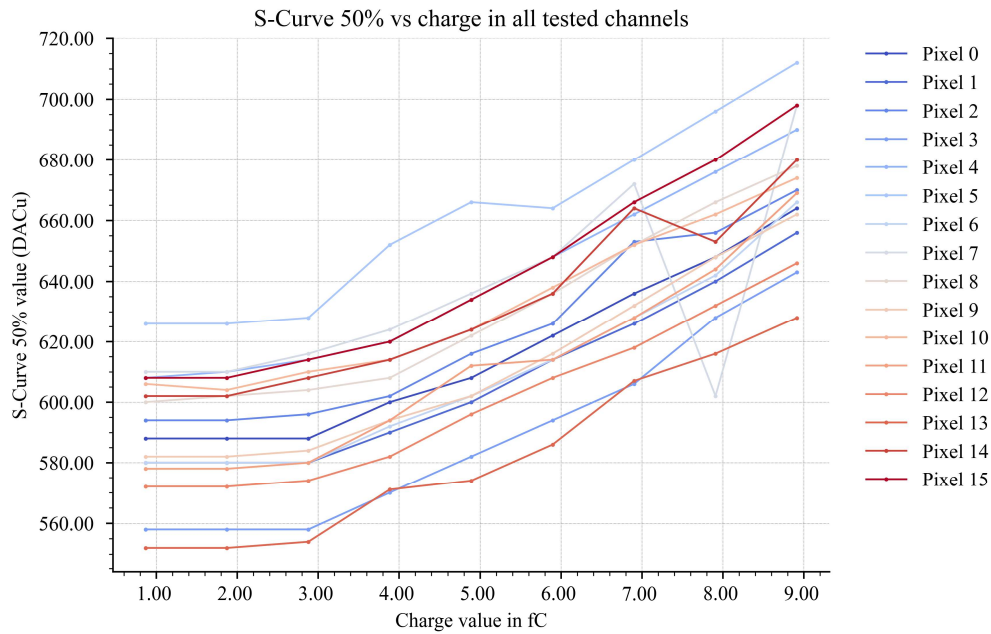
ADC mean value vs charge for a threshold of 650 DACu in all tested channels



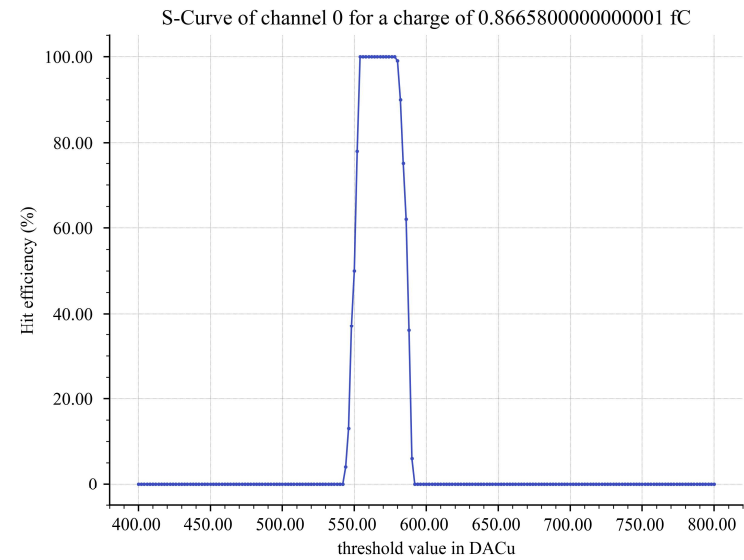
ADC linearity is very similar between channels. The range also seems to be quite similar between all channels. We can see two different “parts” to the linearity, with 2 different slopes.

Slope 1 (from 0 to 32 fC) is around 2.6 ADCu / fC
 Slope 2 (from 32 to 38 fC) is around 3.2 ADCu / fC
 Slope 3 (from 38 to 62 fC) is around 4.4 ADCu / fC

S-Curve 50% vs charge



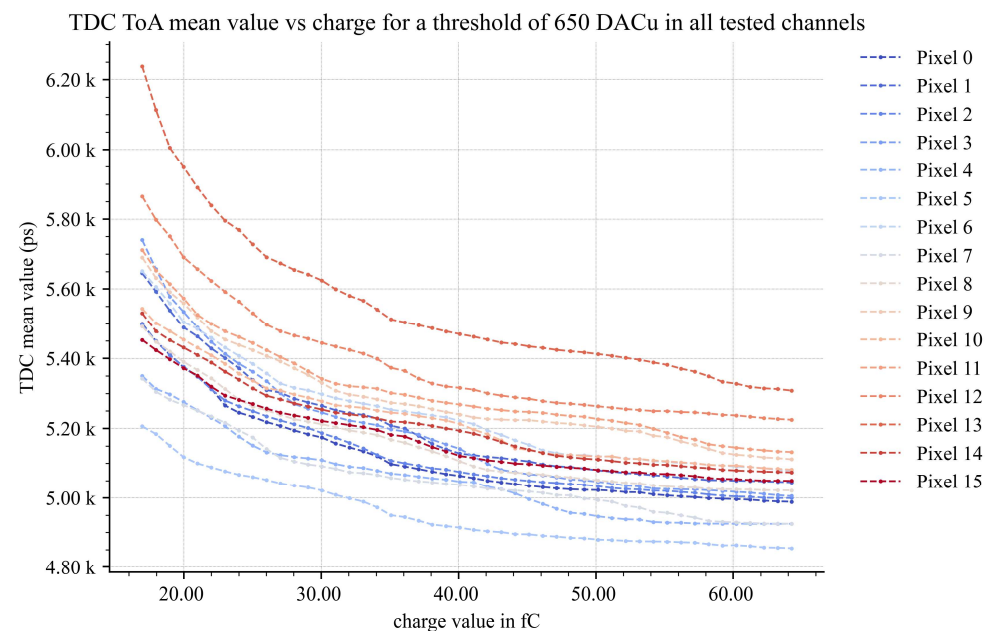
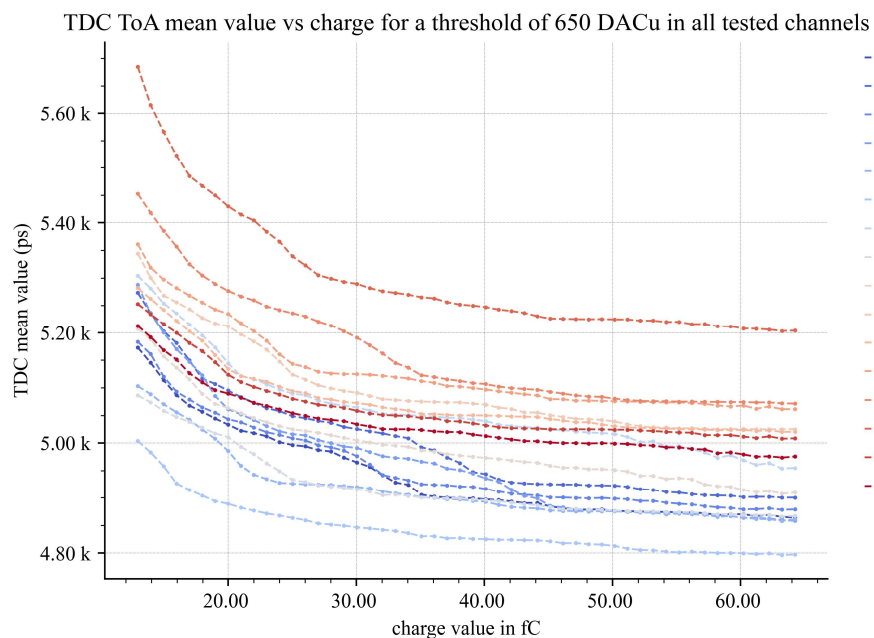
Minimum charge detected is around 4 fC.
 The noise envelope at 1 fC is around 40 DACu (20 mV), as seen on plot (see plot under).
 Slope from 4 fC to 9 fC is around 12.2 DACu / fC, or 6.1 mV / fC



TDC ToA for $c_D = 00$ and $c_D = 11$

$c_D = 00$

$c_D = 11$



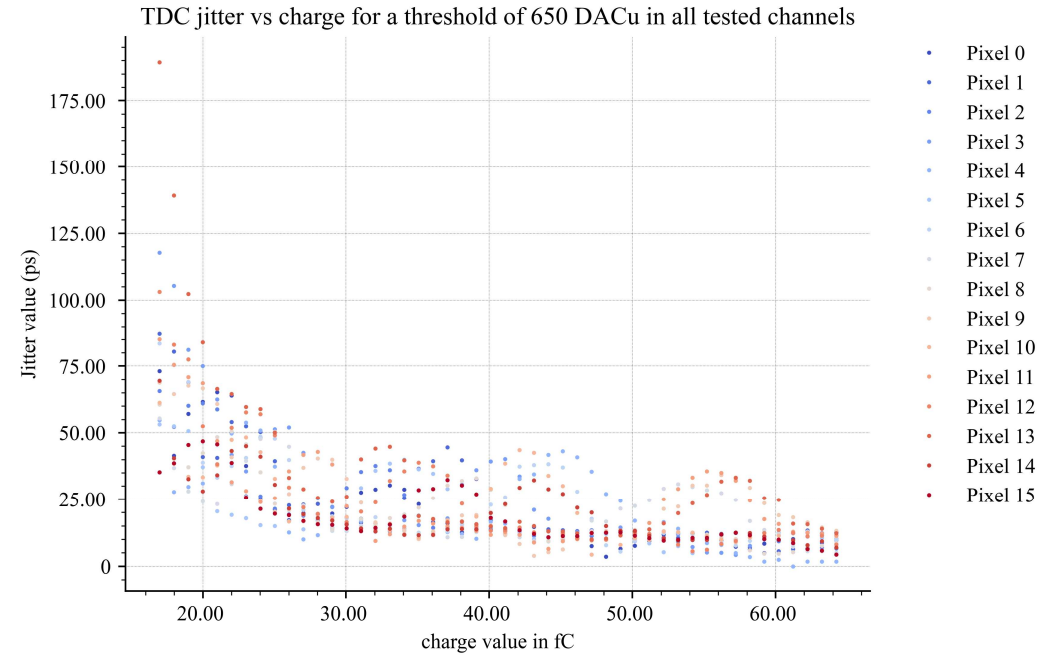
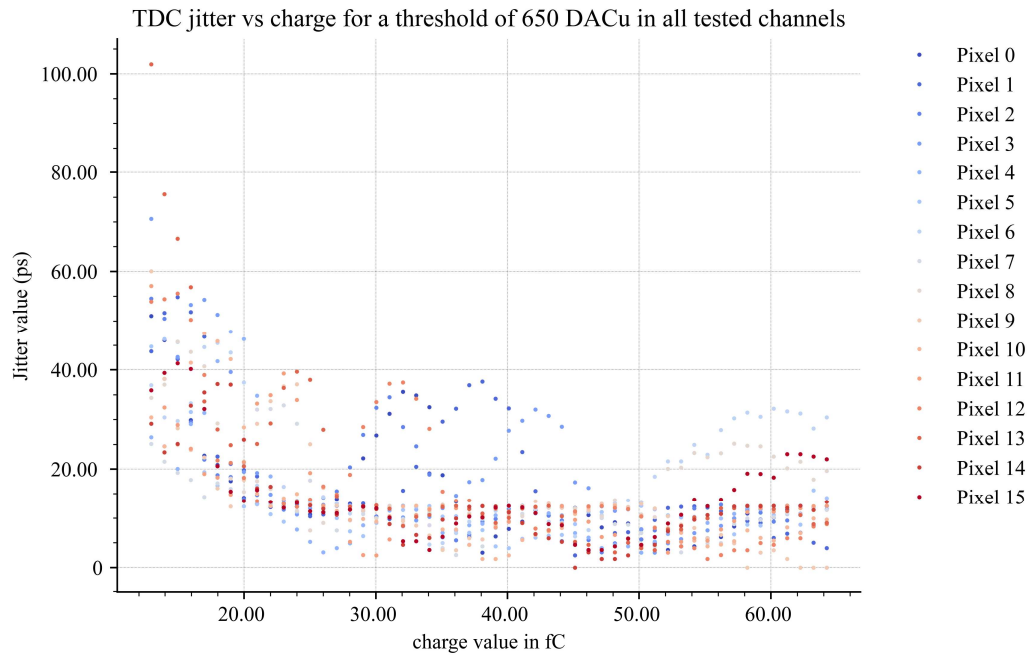
There is a visible effect of c_D on ToA results, with the ToA being higher when the capacitance is enabled. The range is different on the plots because of the additional capacitance which restricted the “usable” charge range in the results to a smaller interval.

In our restricted range, we find a ToA range around 500ps for $c_D = 00$ and 850ps for $c_D = 11$.

TDC jitter for $c_D = 00$ and $c_D = 11$

$c_D = 00$

$c_D = 11$



Jitter plots exhibit a very good jitter floor, which indicates better performance with regards to EICROC0. The “bumps” seen in the TDC values could be from an incorrect TDC configuration.