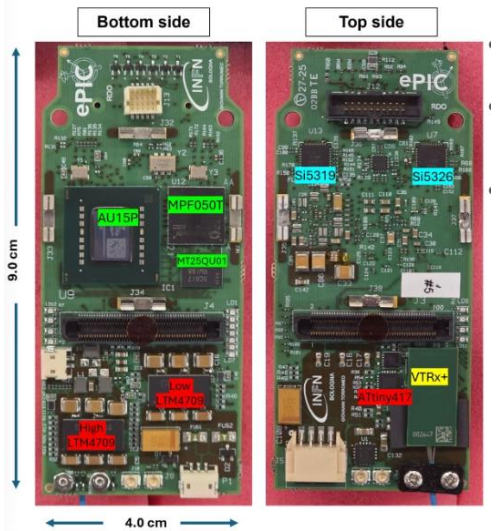


Status of dRICH RDO

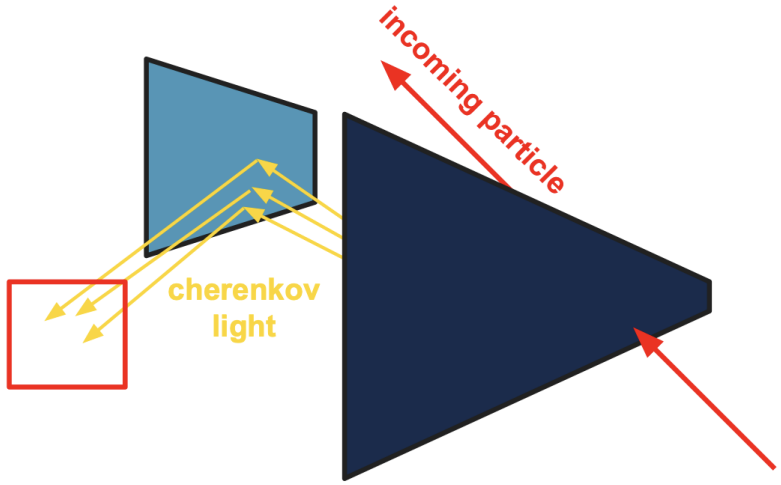
INFN RDO Bologna team
P. Antonioli, D. Falchieri, S. Geminiani, M. Panza, L. Rignanese,G. Torromeo

Electronics & DAQ WG meeting
2 July 2026

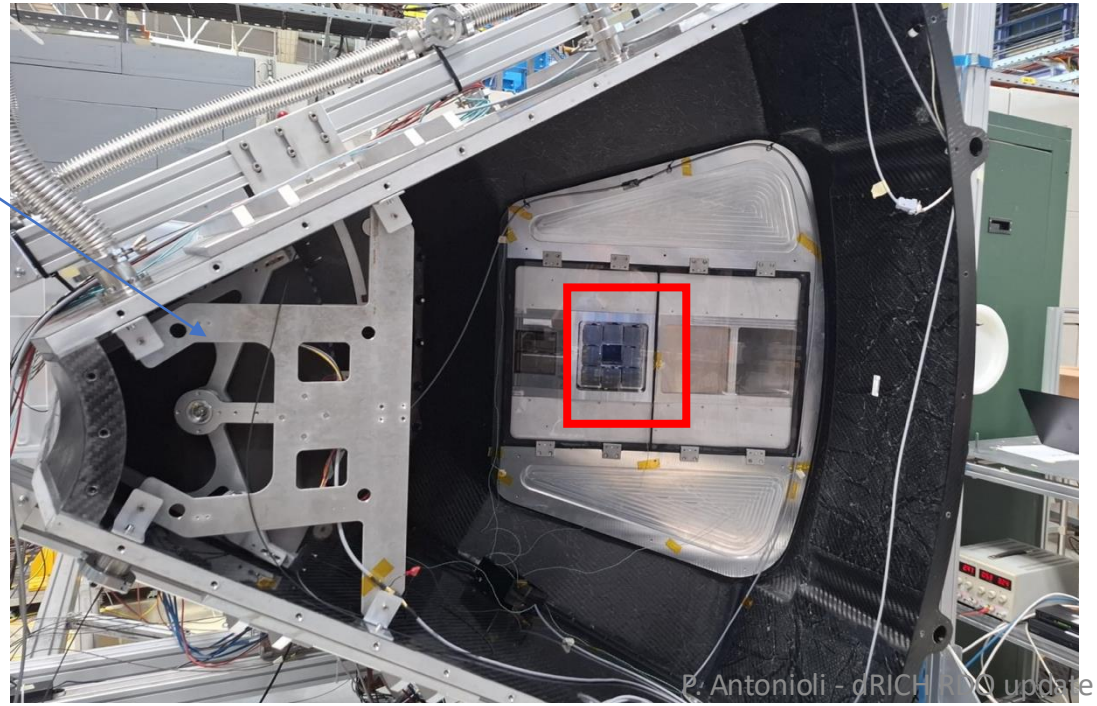
Since last update

- use of RDO at last dRICH test beam
- progresses on testing/developing protocol for RDO-DAM data transmission + focus on recovered clock

From CERN-PS dRICH test beam



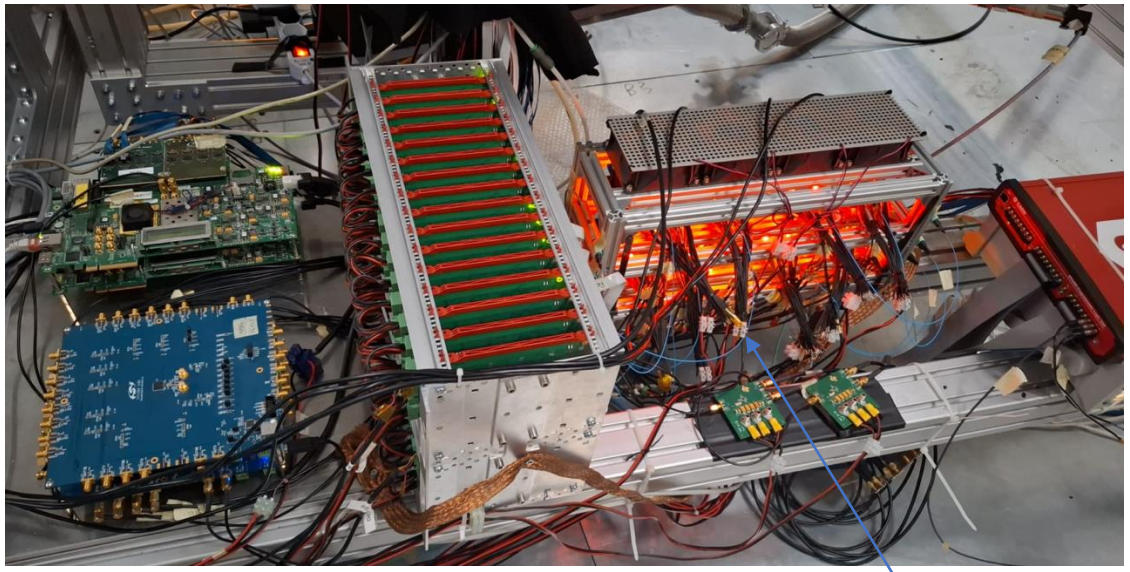
MIRROR



From CERN-PS dRICH test beam

(emphasis here on RDO only)

8 PDU (8 ALCOR32 each) read by 8 RDO

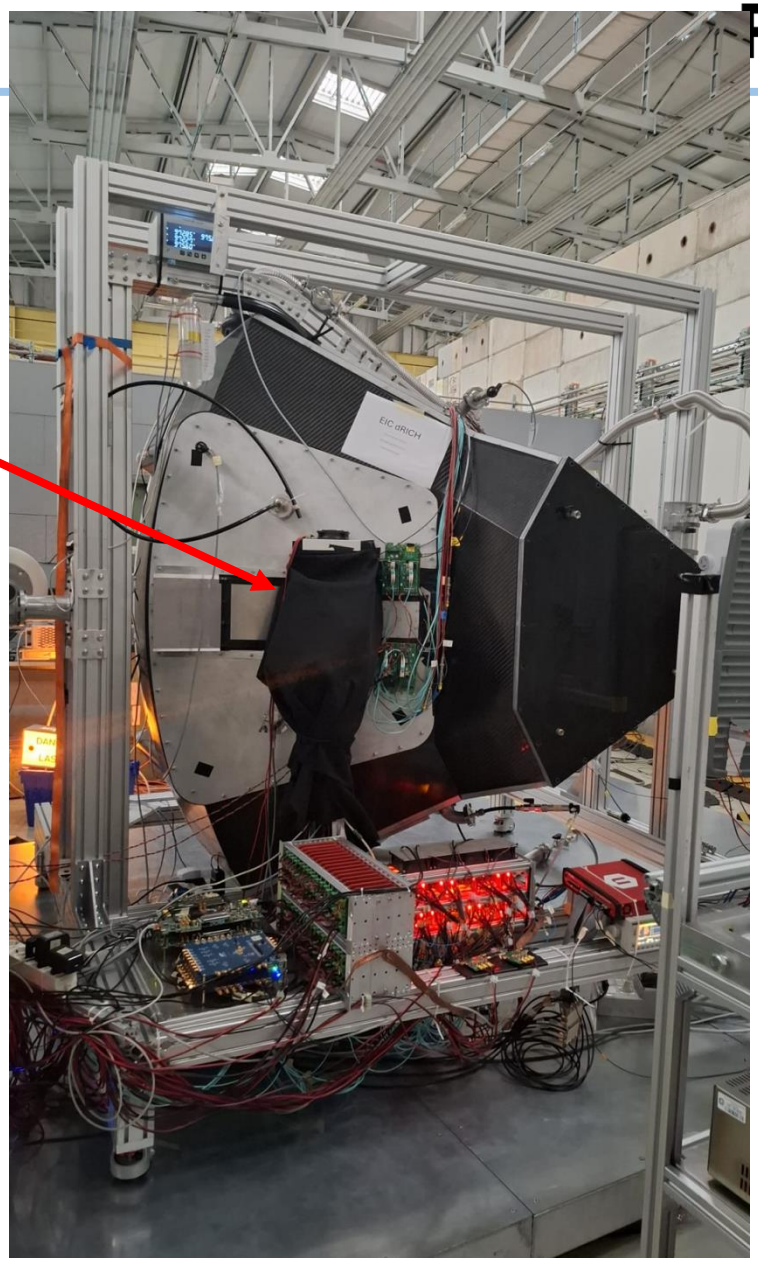


CLOCK

LV POWER

RDO “CRATE”

8 PDU



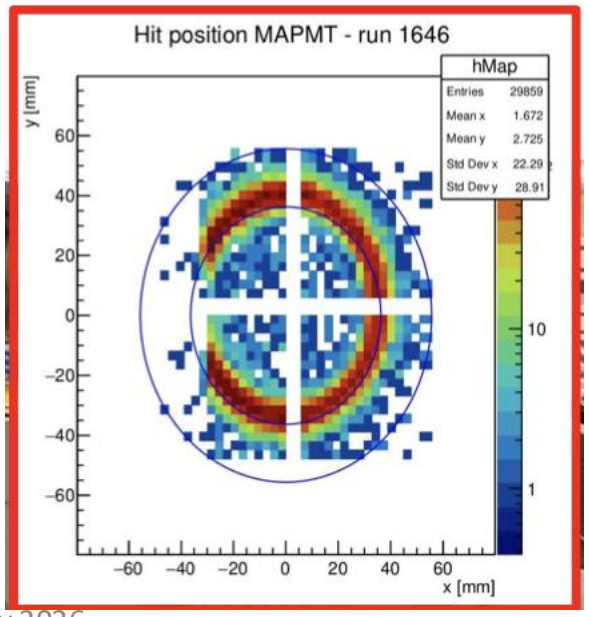
From CERN-PS dRICH test beam

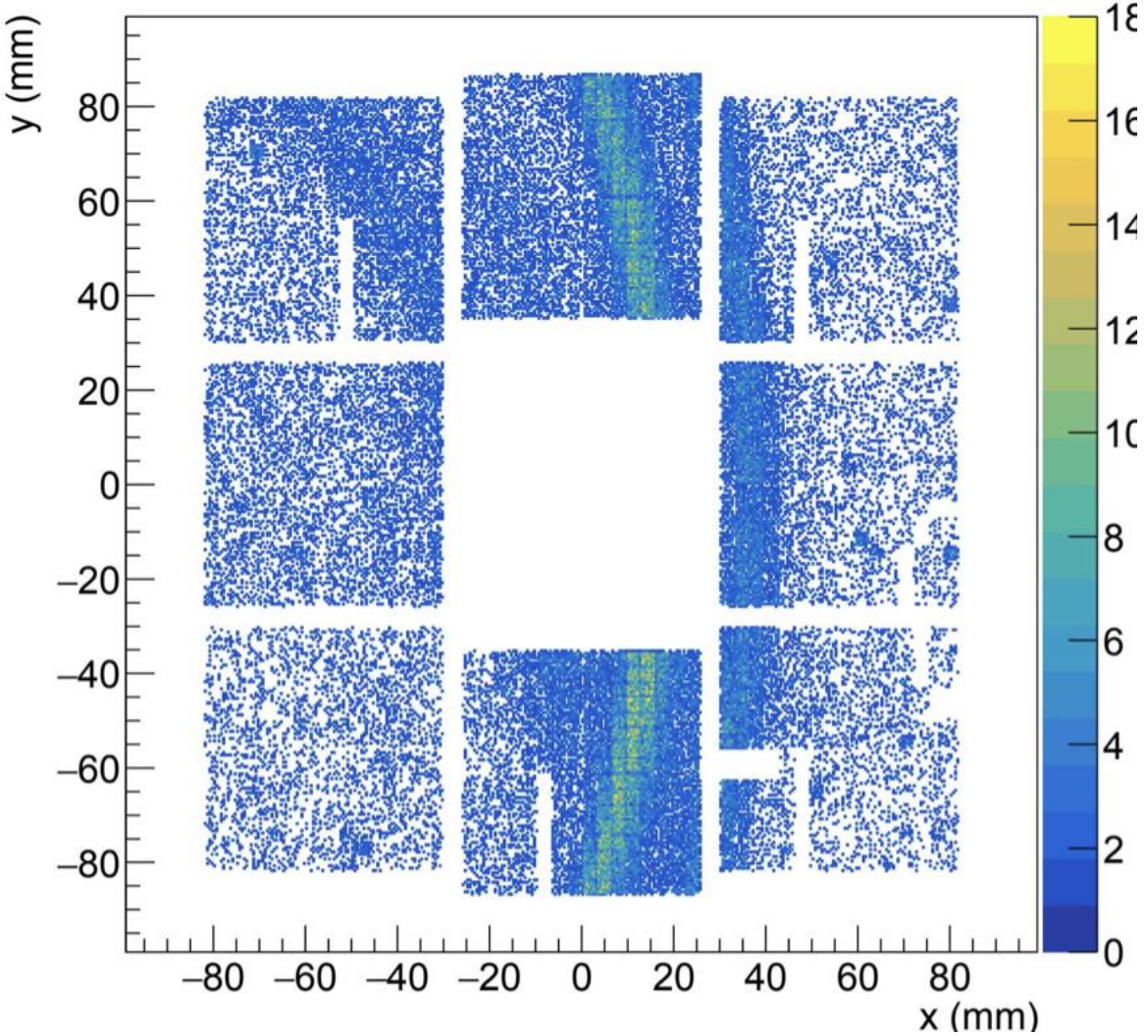
(emphasis on RDO only)

8 PDU (8 ALCOR32 each) read by 8 RDO

readout proved very stable (still on IPBUS)
tested many configurations

(gas ring measured by MAPMT)
(main goal was on new full scale prototype + gas system (C2F6) not on electronics nevertheless… **we are happy with DAQ via RDO**)





Toward RDO-DAM protocol

M. Panza (master student)

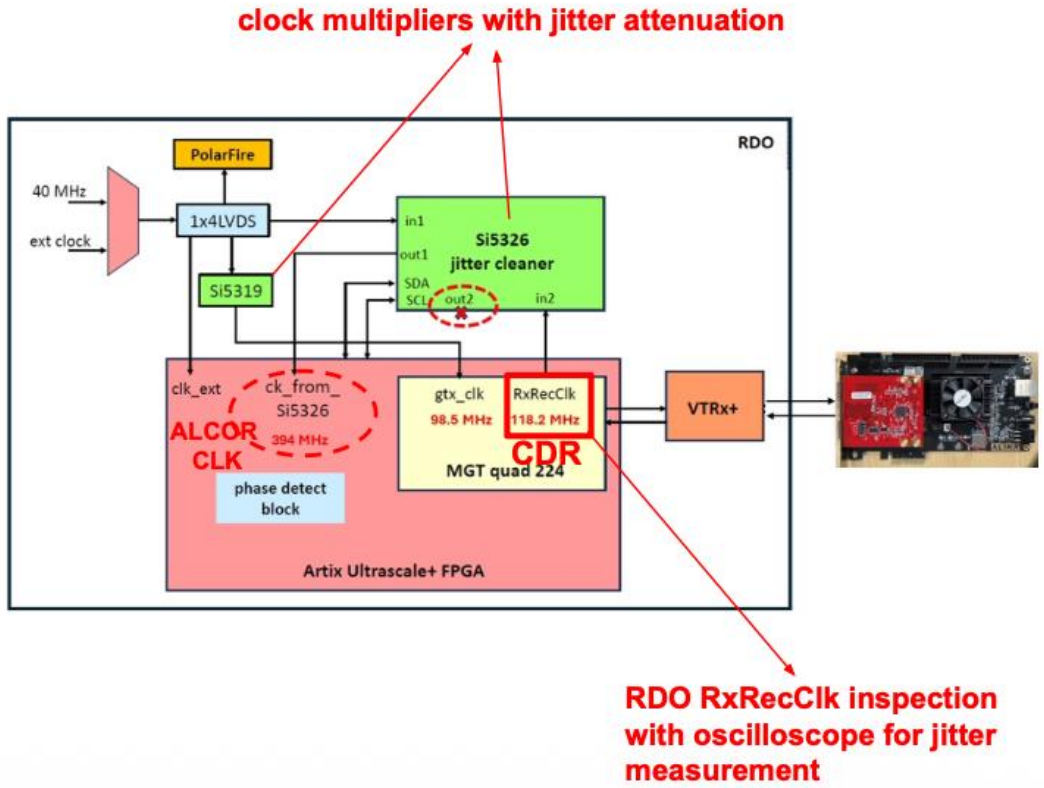
First link implementation with 8b/10b encoding

- **Transceiver Wizard** Vivado IP Core used for link implementation
  - **Settings**
    - **8b/10b** encoding
    - MGT reference clock: 98.5 MHz
    - **Uplink** Line Rates : **1.576 Gb/s**, **9.456 Gb/s**
    - **Downlink** Line Rates : **1.576 Gb/s**, **4.728 Gb/s**
    - User/**Internal Data Width**: 32b / **40b**

- RDO **Clock and Data Recovery (CDR) mechanism** → **from** 0-to-1 and 1-to-0 **transitions** in data received by the DAM, **RDO CDR** circuitry **recovers TX clock** signal up to a **constant** phase shift
  - **RDO recovered clock** frequencies:

    39.4 MHz

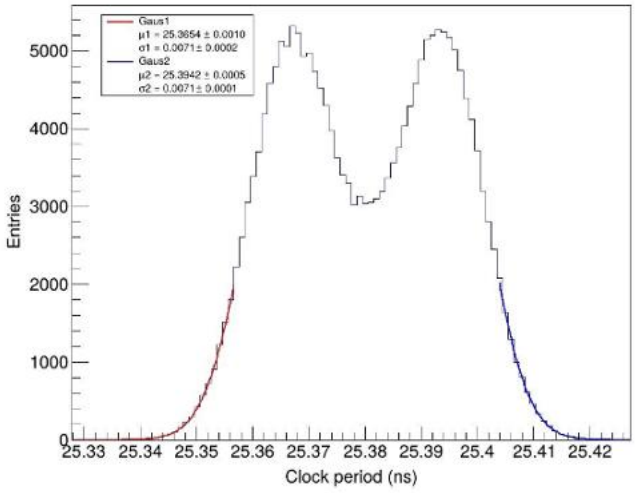
    118.2 MHz = 3 x 39.4 MHz



Preliminary recovered clock jitter analysis

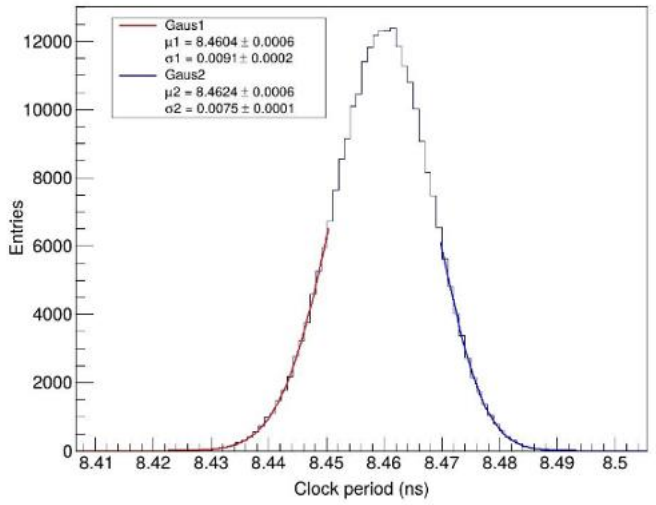
- RDO recovered clock **period measurements** performed with **oscilloscope** at 40 GS/s for jitter evaluation
- **Double Gaussian** fit function

RDO rec_clk jitter measurements

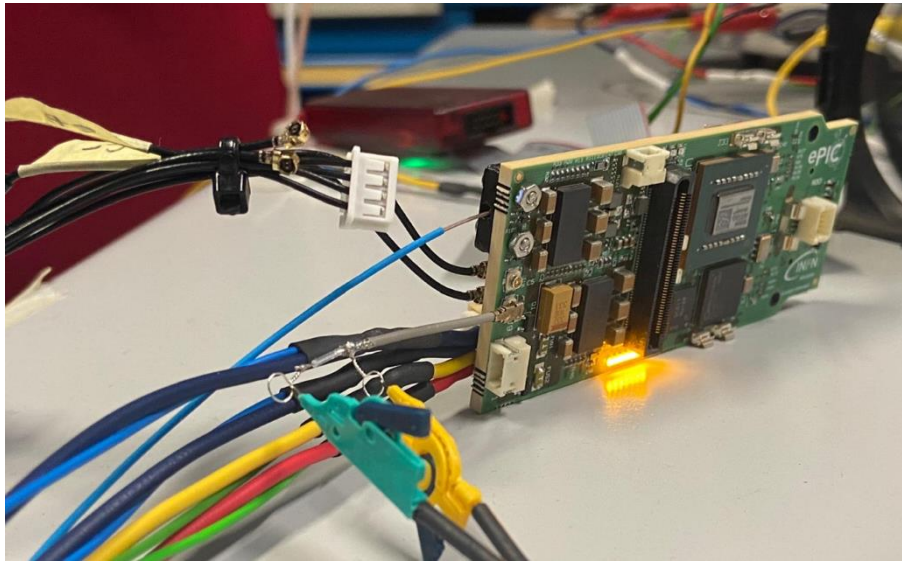


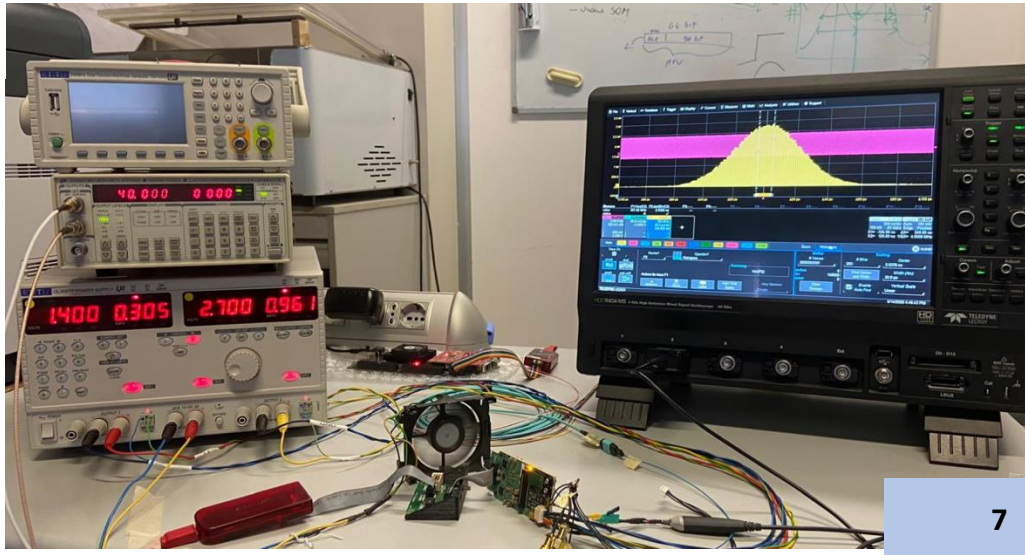
- **39.4 MHz** rec_clk **results**:
  - Deterministic Jitter: 28.8 ± 2.0 ps
  - Random Jitter: 7.1 ± 0.2 ps
  - **Total Jitter: 35.9 ± 1.9 ps**

RDO rec_clk jitter measurements



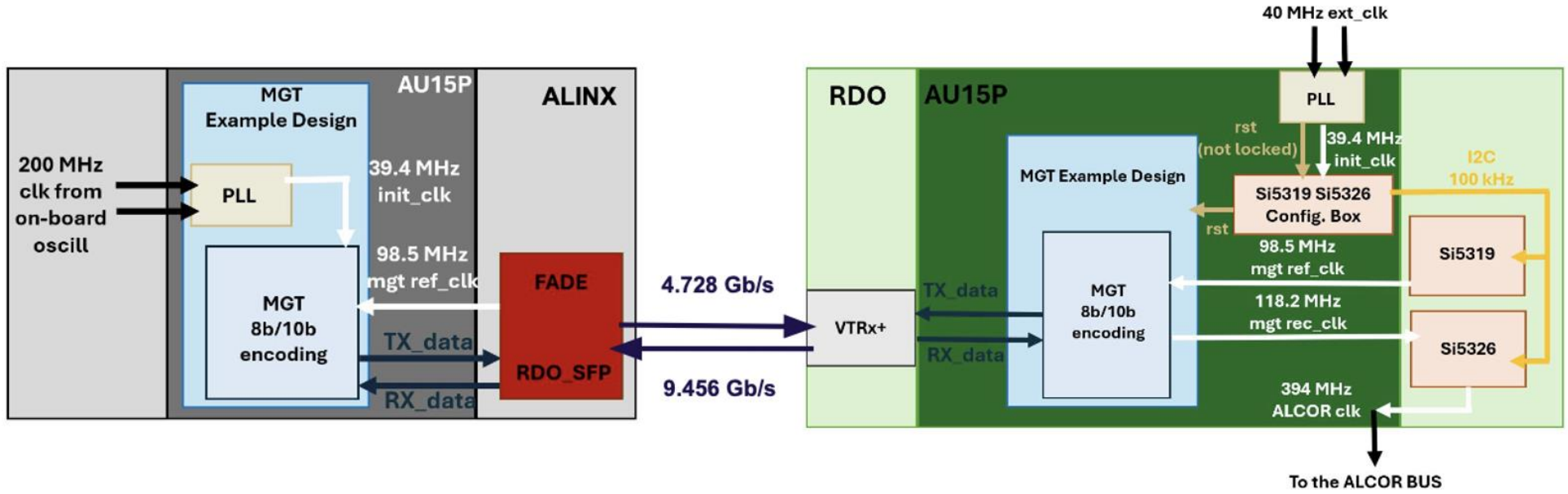
- **118.2 MHz** rec_clk **results**:
  - Deterministic Jitter: 2.0 ± 1.7 ps
  - Random Jitter: 8.3 ± 0.2 ps
  - **Total Jitter: 10.3 ± 1.5 ps**





It works. Several checks on-going plus potential refinements (using HPTDI IP core developed at CERN for AMD US)

Mini-DAQ development



- **Si5326** chip activated by **extending** Si5319 configuration **FSM** and **394 MHz clock inspected** via oscilloscope
- Current focus: **replace** MGT Example Designs implementing 8b/10b encoding scheme in existing firmware architecture with Vivado **Aurora 64b/66b IP Cores**

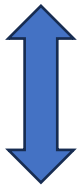
Plan:
- implement Aurora 64b/66b → test (rec. clock + comm.)
- implement lpGBT-FPGA → test (rec. clock + comm.)

compare performance under radiation

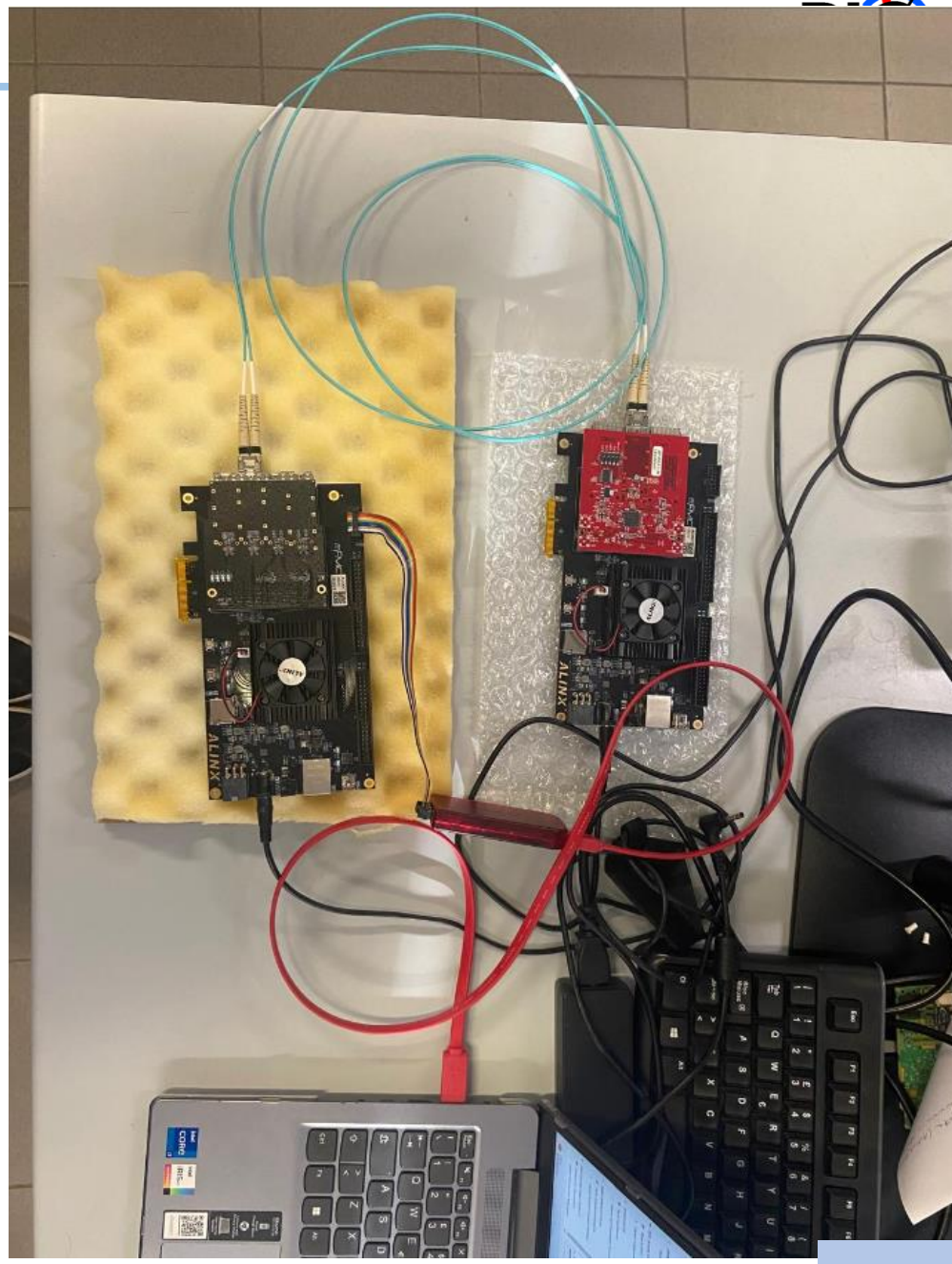
RDO R&D without RDO

we have just 8 RDOs, all deployed at CERN SPS and PS test beams
RDO not available (in Bologna) from 14 May to 1 July!!

(ALINX AXAU15 + FADE) — DAM prototyping



(ALINX AXAU15 + ALINX FH1223) — RDO prototyping



Outlook

- implement and test Aurora 64b/66b and lpGBT
- replace IPBUS interface
- iteration under radiation tests with blind scrubbing
- full exposure of RDO under radiation
- → RDO v1.1 (fix several minor mistakes found through various debugging, preparing for ALCOR64 → PDU with RDO inside)

[more comprehensive presentation on dRICH DAQ backend+frontend @Glasgow in 2 weeks including status about answers related to impact of background on throughput]