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Status report of the eRD109 project on SALSA chip development

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EPIC DAQ/electronics WG meeting

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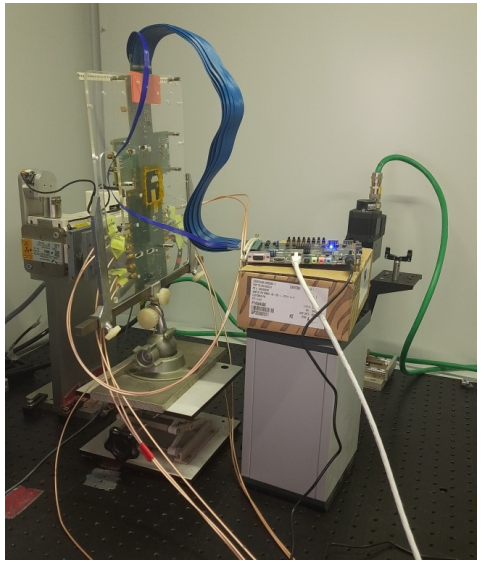
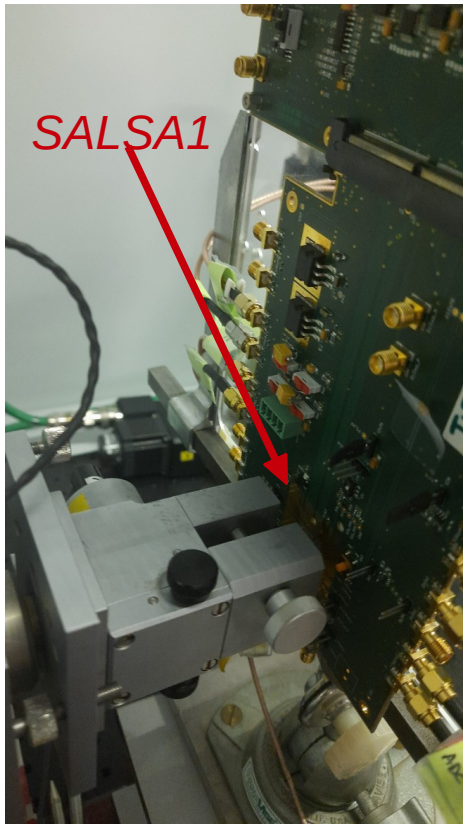
STATUS OF THE PROTOTYPES

SALSA1 prototype

- Radiation tests: done this Monday-Tuesday at X-ray generator in SOLEIL facility near Saclay
- Adapted SALSA1 test-bench: unified test scripts, measurement of all probes
- Radiation levels not well known yet, around 300 krad/h, no result yet
- No date yet for TID tests on PRISMEv1





CURRENT STATUS: SALSA2

SALSA2 development status

- Front-end:
  - Whole schematic and layout done
  - But changes ongoing due to no more access to lead-free bumps for TSMC 65nm MPW (cf next slide)
- DSP
  - Updates done: data processing chain, pipeline flushing during reset
  - Updates ongoing on few modules: pattern generation, statistics
  - Discussions on triplication for rad hardness, TMRG tool, selection of signals to triplicate
  - Tests ongoing with FPGA, integration of DSP in main UVM workspace ongoing
  - Verification starting, some bugs already found
- I/O core
  - Updates done on clock manager for improved efficiency, simplification of sampling clock resync mechanism
- Control core
  - Updates on slow-control registers, on fast command decoding, and on general counters
  - Asynchronous SC bit decoding done, integration foreseen soon
  - Packet generation for synchro and monitoring data in progress
  - Next step: tests of control core + DSP (all processing chain) with UVM

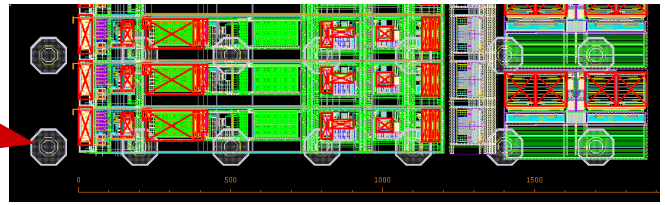
Timeline

- Chip submission foreseen November 2026, but consequences of bump issue to be evaluated
- Tests from Spring 2027
- Distribution to users expected from Summer 2027

BUMPS IN TSMC 65NM MPW PROJECTS

Issue with bumps

- TSMC no longer produces lead-free bumps for 65nm MPWs, but engineering runs are still ok
- Only copper pillars (pitch < 210nm) are proposed for MPWs
- Present SALSA2 designs with bumps at 300µm pitch



Possible solutions

- Keep MPW with bumps
  - we have to buy additional complete wafers, and manage all bump processes ourselves
  - → long, additional costs, involving extra companies
- Engineering run with bumps
  - Too expensive (~650k€) → need to find partners to share reticle
  - Possible but would introduce delays
  - Future of lead-free bumps ?
- Go to copper pillars
  - Pitch < 210µm → need to adapt layout (for instance, go to 150µm)
  - Need time to validate integration in BGA package (package company involved in discussions)
  - Compatible with bonding finish

Present situation

- Bumps vs copper pillars solutions still under study
- Idea to add pads on periphery of chip design → first tests with bonded connections, gives more time to complete BGA packaging
- Decision to be taken soon

PROJECT MILESTONES AND NEXT STEPS

eRD109 FY24 project milestones

- SALSA2 specifications → July 2024
- SALSA2 submission → November 2026
- Beginning of SALSA2 tests → Spring 2027

eRD109 FY25 project milestones

- SALSA3 design specifications → aiming Q4 2026 (after SALSA2 submission)
- SALSA3 submission → Spring 2028
- Performance evaluation → 2nd semester 2028

Very next steps

- SALSA1 tests → Results of TID tests
- PRISMEv1 chip → TID tests after Summer ?
- SALSA2 development → in progress