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SVT Data Rates

J. Schambach

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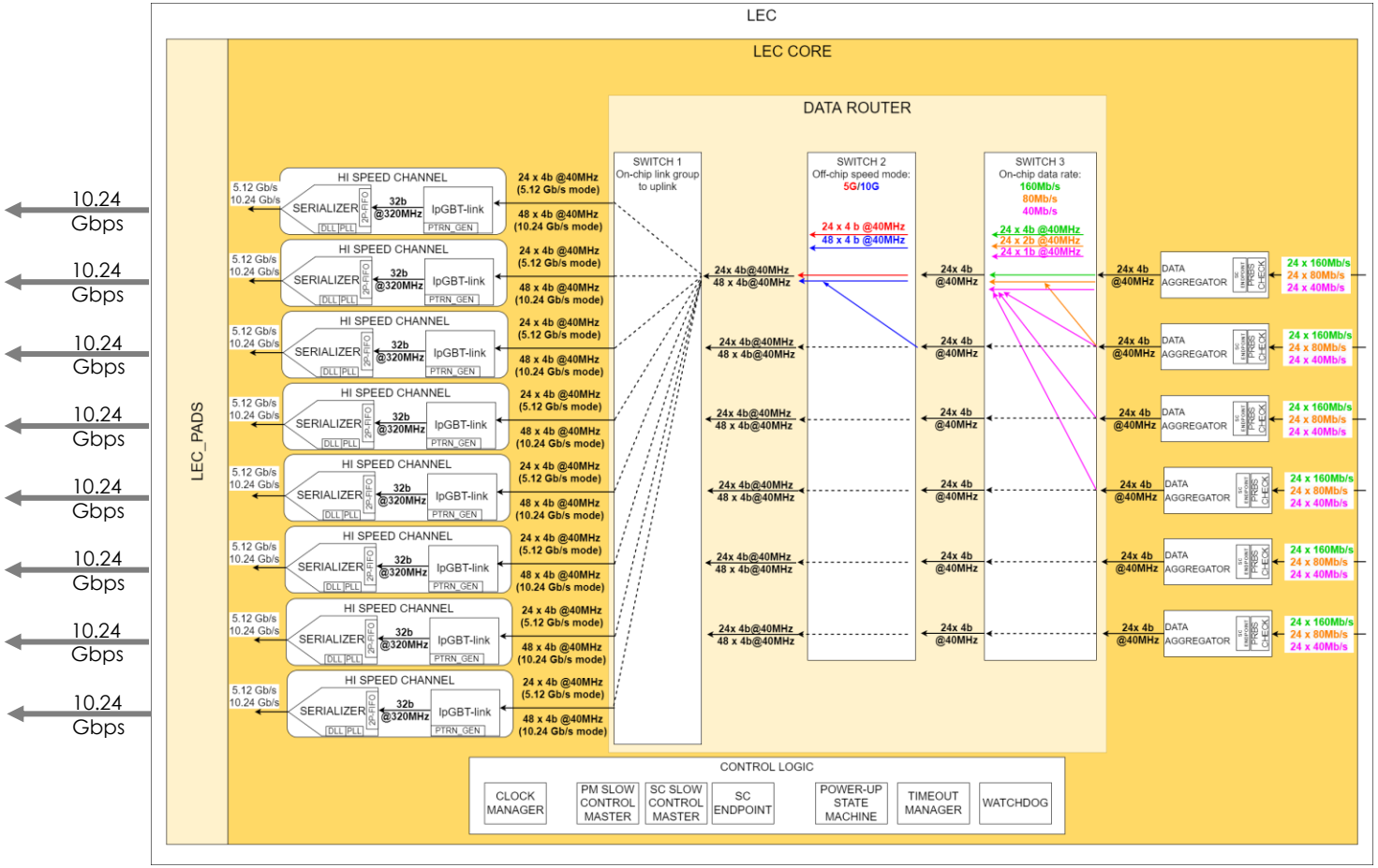
U.S. DEPARTMENT OF ENERGY

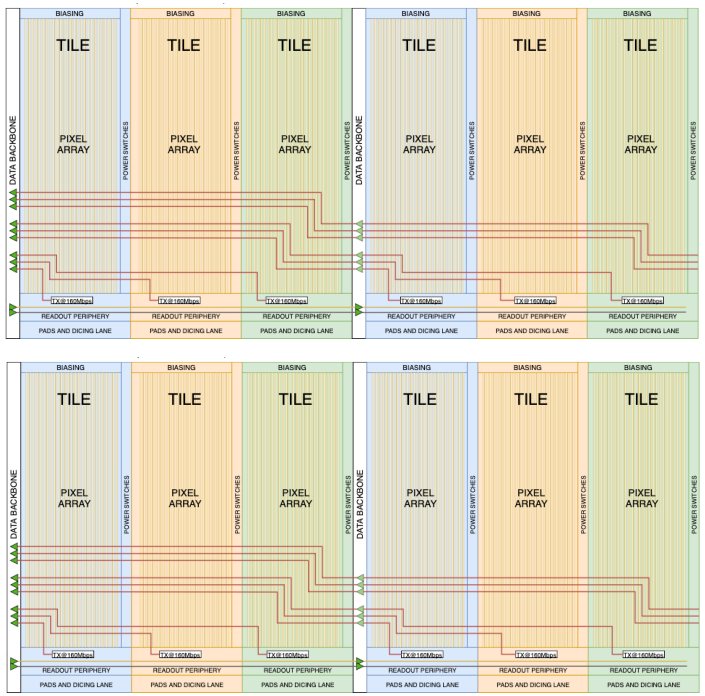
Data Flow – From Tiles to Left Endcap



x 12 RSU

72 Links

72 Links



12-RSU MOSAIX (SVT IB)

The data encoding block is the **lpGBT's TX** core
160 Mbps x 144 = 22.5 Gbps
Full capacity: 8 HS serializers = 80 Gbps (10 Gbps each, only 3 used)
Fallback: 40 Gbps, 5 Gbps each (6 used)
4 serializer data outputs drive one VTRx+

SVT Outer Barrel & Disks

6-RSU LAS
72 Tiles
1 HS serializer = 10 Gbps

5-RSU LAS
60 Tiles
1 HS serializer = 10 Gbps

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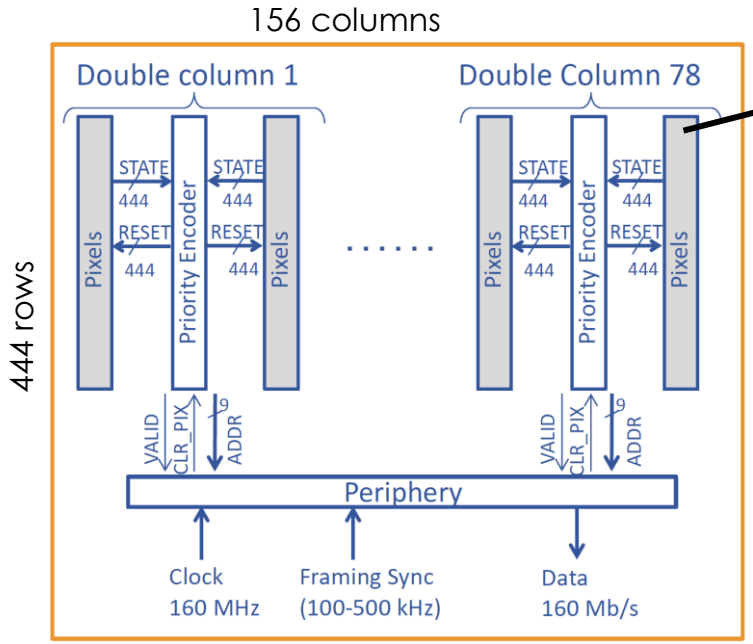
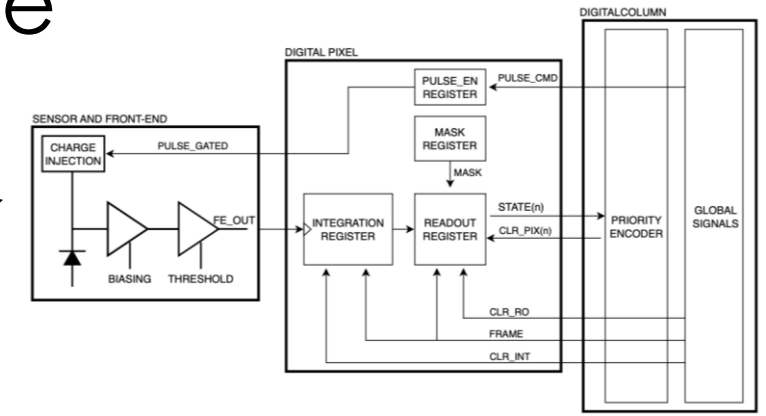
Domain (Tile) Architecture





444 x 156 pixels / domain
831168 pixels per RSU
144 domains / segment
9.974 Mpixels / segment

20.8 µm x 22.8 µm pixel pitch(*)
Continuously active front-end (40 nW typ.)
Global shutter
Zero-suppressed matrix readout
Continuous readout mode
Integration time: 2µs to 2^{16}*25ns = 1.6384ms

(*) **Baseline: 20.8 µm * 22.8 µm**
Abs. Max: 22.5 µm * 25 µm

In pixel:

- Amplification
- Discrimination
- Hit integration register and readout register
- Test charge injection
- Digital pulsing
- Masking

Digital pixel designed with low-leakage, high reliability std cells

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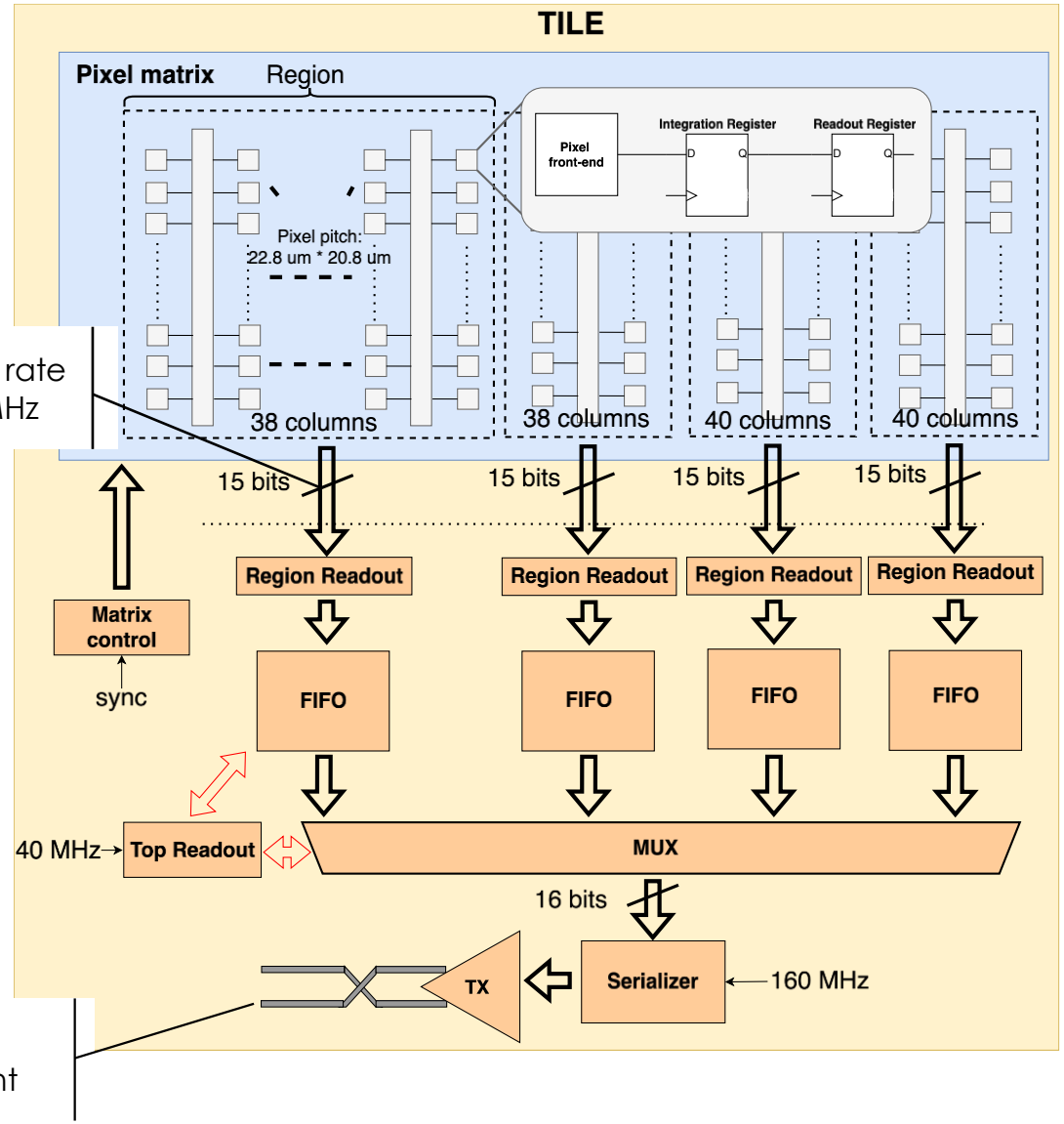
On-chip Readout Scheme in the Periphery

- Framing time base re-generated in each TILE periphery
  - FRAME local signal synchronizes pixels, Region Readout and Top Readout
  - Global SYNC input signal *aligns in time* the integration intervals across tiles
- Four parallel readout processes in each tile
  - Regions have 38 or 40 columns
  - Double columns in one region are sequentially read out
  - Region data packet is stored in FIFOs
  - Double columns and full regions can be masked
- Serial transmission of tile packet to LEC
  - Top readout aggregates region data packets for the same frame interval
  - Tile transmits one data packet for each frame interval, in order



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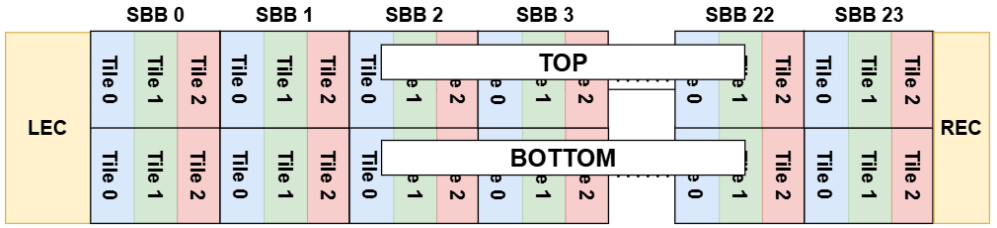
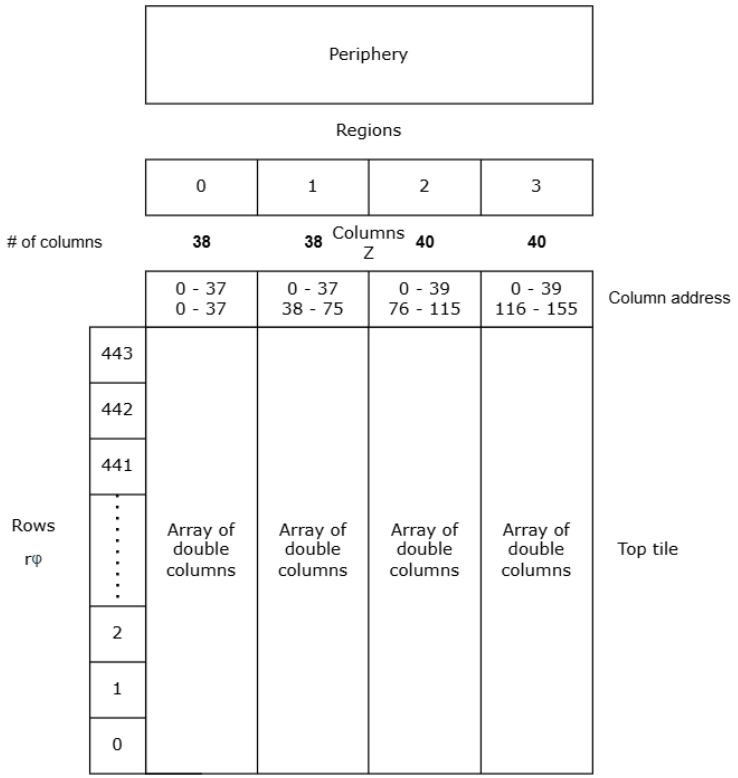
Addressing

- Stitched Back Bone (SBB) -> 5 bits for SBB, 2 bits for tile in SBB, 1 bit for Top/Bottom



- Pixel row: 0 -443 -> 9 bits
- Pixel columns per region 38 or 40 ->6 bits
- 4 regions -> 2 bits



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Tile Readout Protocol

READOUT PROTOCOL																
Word type	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IDLE	1	1	0	0	0	1	0	1	IDLE config [7:0]							
LOCK	1	1	0	0	1	0	1	0	IDLE config [7:0]							
READOUT_STATUS_1	1	0	0	1	1	1	0	0	Integration Window Counter [15:8]							
READOUT_STATUS_2	1	1	1	1	IWC Checksum [3:0]				Integration Window Counter [7:0]							
TILE_HEADER	1	0	1	0	0	0	0	0	Unit Slice [4:0]					Tile [1:0]		T/B
REGION_HEADER	1	0	1	0	1	1	Region Address [1:0]		Integration Window Counter [7:0]							
DATA	0	Pixel Address Row [8:0]							Pixel Address Column [5:0]							
TILE_TRAILER	1	0	1	1	TRU Status Flags [3:0]				Packet Checksum [7:0]							
EMPTY_INTEGRATION_WINDOW	1	1	1	0	TRU Status Flags [3:0]				Integration Window Counter [7:0]							
DROPPED_INTEGRATION_WINDOW	1	1	0	1	TRU Status Flags [3:0]				Integration Window Counter [7:0]							
RECOVERY	1	0	0	1	0	0	1	1	'0							
RESERVED	1	0	0	0	RESERVED											

Bit Counts

1 tile noise pixel:
- 1 tile header
- 1 region header
- 1 data
- 1 tile trailer

4 words
-> 64 bits per pixel

1 tile hit (3 pixels):
- 1 tile header
- 1 region header
- 3 data
- 1 tile trailer

6 words
->96 bits
-> 32 bits per pixel

1 hit (3 pixels) per region:
- 1 tile header
- 1 region header
- 3 data
- 1 region header
- 3 data
- 1 region header
- 3 data
- 1 region header
- 3 data
- 1 tile trailer

18 words
-> 288 bits
-> 24 bits per pixel

2 hits (3 pixels) in 1 region:
- 1 tile header
- 1 region header
- 6 data
- 1 tile trailer

9 words
-> 144 bits
-> 24 bits per pixel

4 hits (3 pixels each) in 1 region:
- 1 tile header
- 1 region header
- 12 data
- 1 tile trailer

15 words
-> 240 bits
-> 20 bits per pixel

1 tile hit (2 pixels):
- 1 tile header
- 1 region header
- 2 data
- 1 tile trailer

5 words
-> 80 bits
-> 40 bits per pixel

1 row threshold scan:
- 1 tile header
- 1 region header
- 38 data
- 1 region header
- 38 data
- 1 region header
- 40 data
- 1 region header
- 40 data
- 1 tile trailer

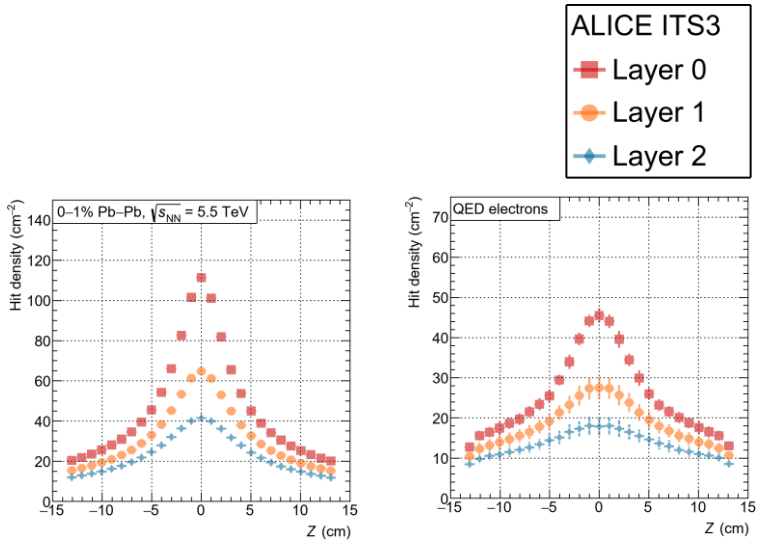
162 words
-> 2,592 bits

ITS3 simulation for central PbPb

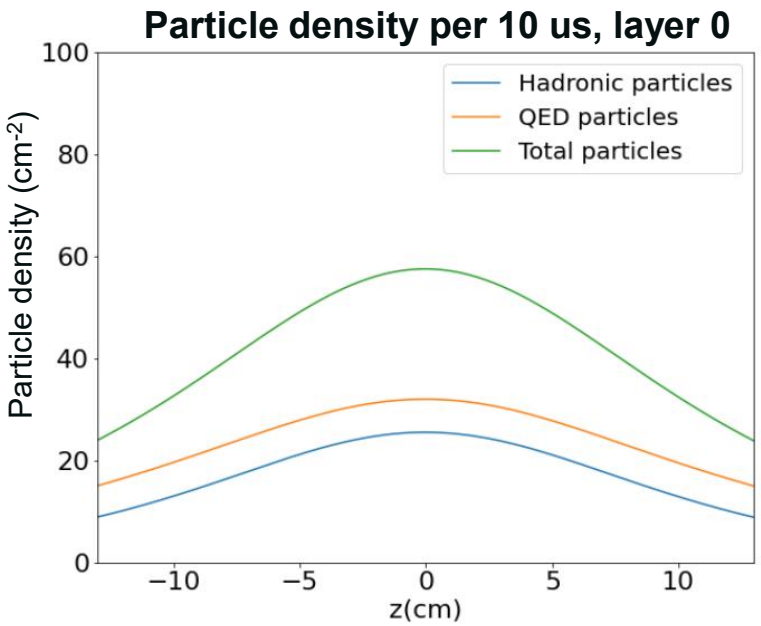
From simulation of MOSAIX, the cluster size for MIPs is given by:

a + b*(number pixels crossed)

where **a** and **b** are ~**1** and **number of pixels crossed** is given by geometry considering an active sensor thickness of **10µm**.

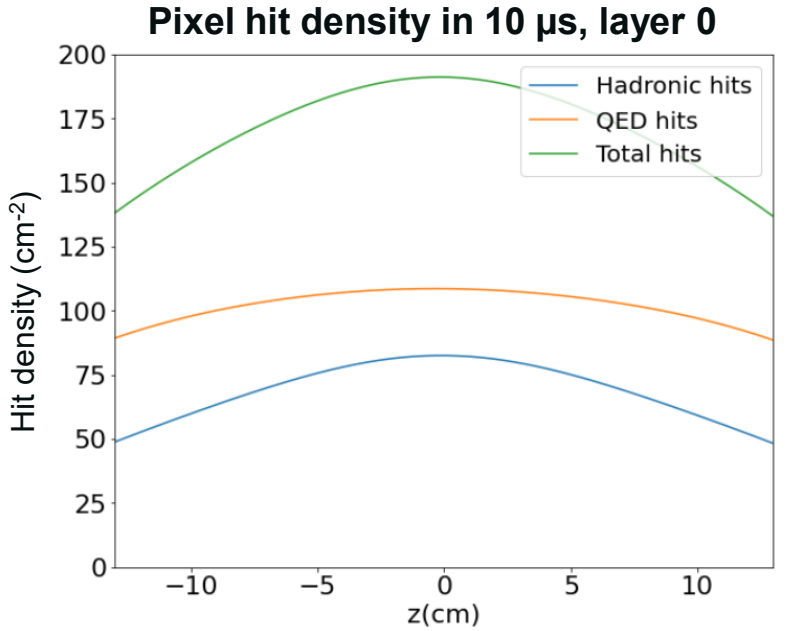


2 – 6 pixels per hit ("cluster")



X

=



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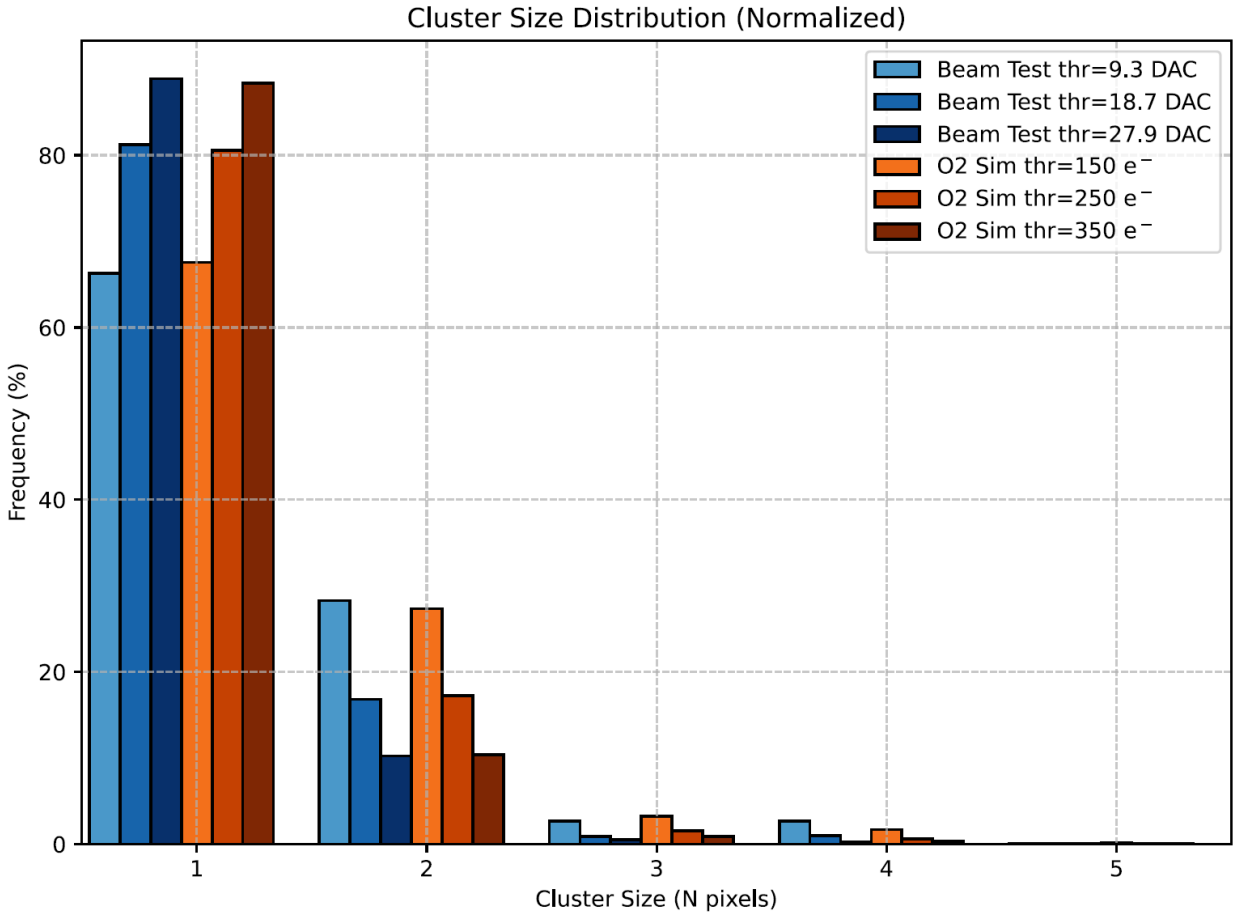
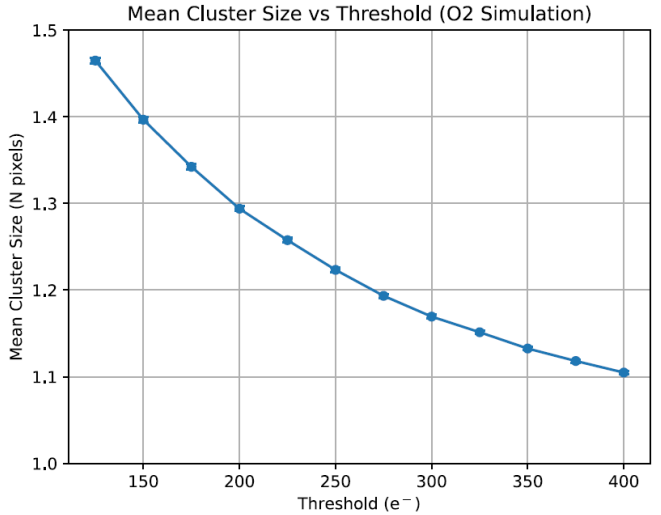
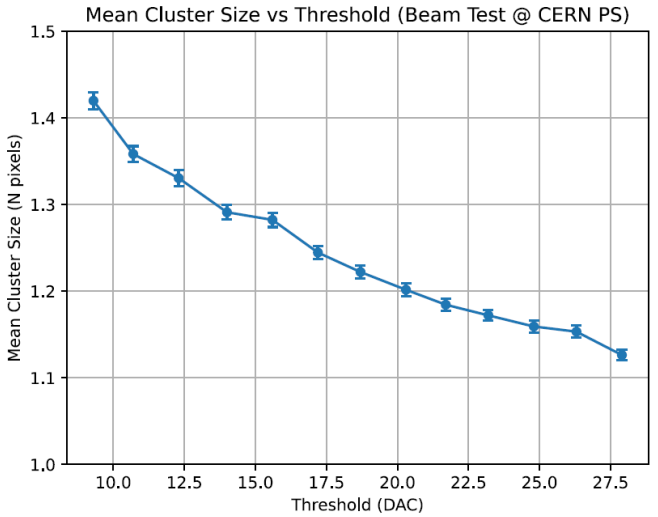
Chip response in the simulation – comparison with test beam data

F. Grosa (CERN)
fgrosa@cern.ch







- Distributions of cluster size (shape) compared between simulation and test beam data to verify that they are realistic
  - ➡ Dependencies on incident angle, particle species, particle momentum to be reproduced

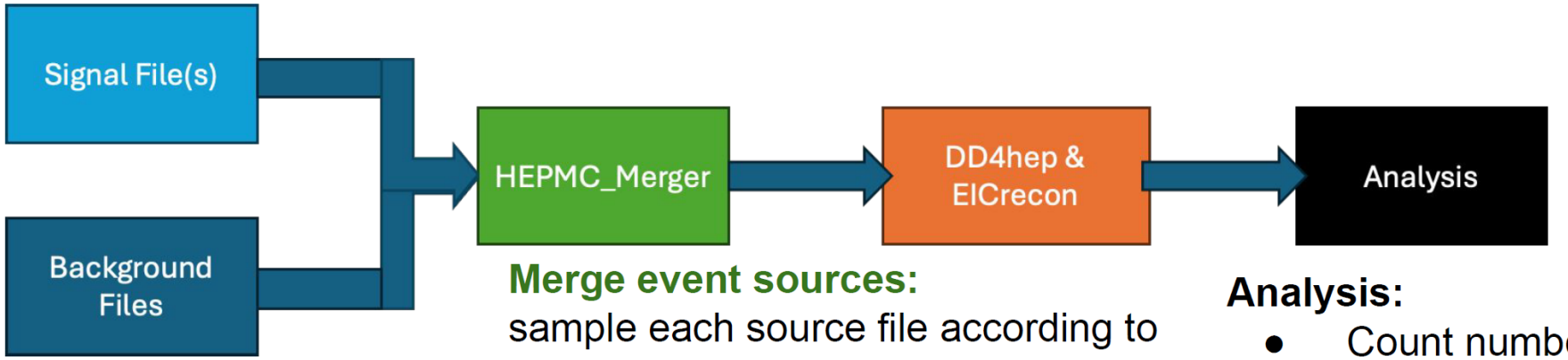
C. Wang

Shujie's presentation to TIC:

1. Signal+Background Simulation:

Prepare realistic event sample

- One event = one 2us time slice with merged signal and background.



Merge event sources:
sample each source file according to their frequency within a fixed-length (2us) time window

Analysis:

- Count number of digitized hits on SVT per area per time

Configuration to use for SVT rate study:

- **10x275** GeV beam (highest rate)
- Forced DIS + background events. Each contains:
  - One Q^2>1 GeV^2 NC DIS vertex
  - Several beam background collisions (SR, Bremsstrahlung, Coulomb, Touschek, proton beam gas) at calculated freq. See details at ePIC wiki

Previous studies presented at TIC (Barak and Shujie):

- 26.01 geometry with 10um Au coating, **10x275** beam link
- Simulation campaign 26.03, **10x100** beam link

Link to spreadsheet

26.04.1 DIS+Background rate summary 10x275 beam

Simulation campaign , 26.04.1 — Shuije Li, 06.2026

10x275 GeV setting with 10um gold beampipe coating — All counts are per millisecond (ms) --> kHz

1ms of mixed data = 1000 events x (one DIS collision at Q2 >1 GeV2 per 2us + beam background per event) / 2

			Hit rate (kHz) by source					
Layer name	Total hits (kHz)	MAX hit on a single RSU (20x20mm)	DIS	SR	Bremstrahlung	Coulomb	Touschek	Proton beam gas
E-Si Disk 4	32,767	75	684	29,245	2,177	218	133	311
E-Si Disk 3	146,187	370	701	142,384	2,398	235	154	316
E-Si Disk 2	225,029	1336	742	221,153	2,456	232	141	304
E-Si Disk 1	233,208	1641	761	229,330	2,430	238	152	297
E-Si Disk 0	130,914	1594	470	127,760	2,104	196	128	255
H-Si Disk 0	112,586	1421	901	108,933	2,177	199	127	249
H-Si Disk 1	156,696	1270	1,381	152,188	2,456	239	129	302
H-Si Disk 2	37,582	180	1,879	32,603	2,451	238	118	293
H-Si Disk 3	8,362	170	3,009	2,634	2,162	212	85	260
H-Si Disk 4	6,431	155	3,201	738	2,006	199	62	225
L0	362,256	4451	1,067	357,406	3,049	298	307	129
L1	252,161	2221	961	247,634	2,817	231	239	279
L2	154,604	521	481	152,647	1,305	94	39	39
L3	183,494	270	598	182,065	679	78	36	38
L4	138,915	100	565	137,366	798	57	49	81

Sensor Response in Simulation: adding details

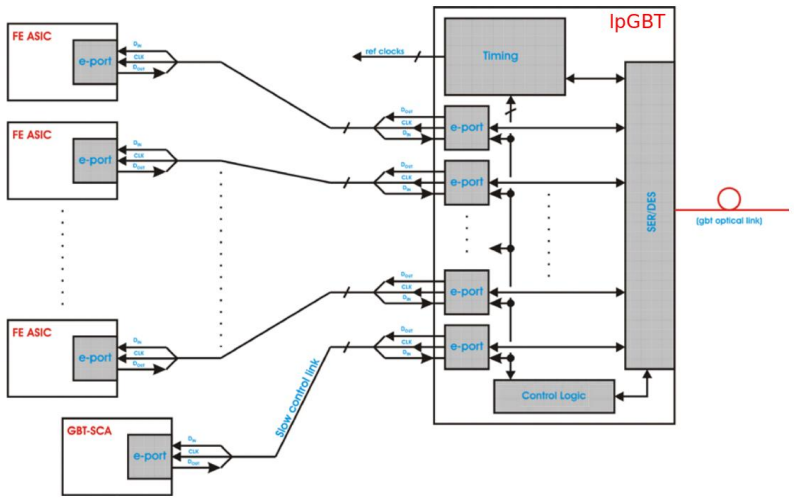
- Sensor structure:
  - 40um thick of active silicon, 20um x 20um grid to simulate the pixel size.

    How to describe epitaxial and substrate in simulation with the settings of active/inactive? See Yu Hu's talk next

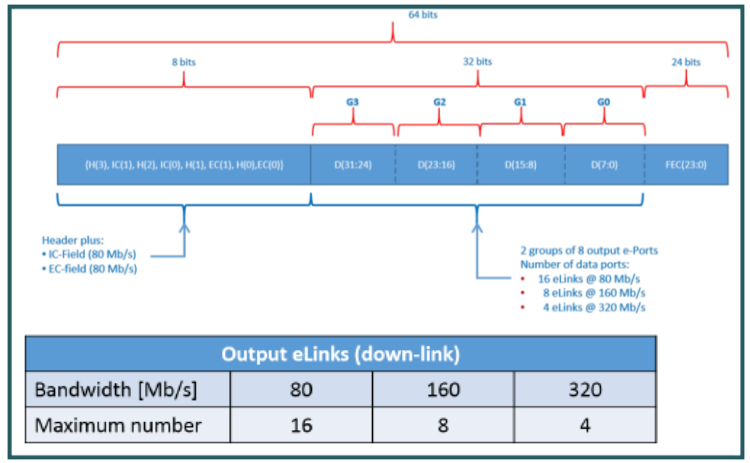
- Particle dependence:
  - Charged particle:
    - Usually going through the material
    - # of pixels per hit can be parameterized as a function of incident angle according to beam test, then introduce clustering algorithm accordingly.
  - Low energy photon:
    - absorption → photo-electron emission
    - Interaction probability sensitive to material thickness (see next slide for example)
    - # of pixels per photon?

Left Endcap Routing

lpGBT Protocol



- Front Ends connect to “e-links”
- The fiber protocol includes “Forward Error Correction”
- Downlink runs at 2.56 Gbps
  - Downlink frame is 64bit wide, of which 32 bits are payload
  - 1.28 Gbps payload
  - Up to 16 e-links @ 80 Mbps
- Uplink runs at either 10.24 Gbps or 5.12 Gbps
  - Uplink frame is either 128bit or 256bit
  - 256bit frame contains 192bits of payload (7.68 Gbps)
  - Up to 24 e-links at either 160 Mbps or 320 Gbps



Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

Downlink

Line Rate: **2.56 Gbps**
32 out of 64 bits are data:
Payload = **1.280 Gbps**

Data Uplink

192 out of 256 bits are data:
Payload = **7.680 Gbps**

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Field	5.12 Gbps FEC5	5.12 Gbps FEC12	10.24 Gbps FEC5	10.24 Gbps FEC12
Frame [bits]	128		256	
Header [bits]	2		2	
IC [bits]	2		2	
EC [bits]	2		2	
D [bits]	112	96	224	192
FEC [bits]	10	24	20	48
LM [bits]	0	2	6	10
Correction [bits]	5	12	10	24
# of eLink groups	7	6	7	6

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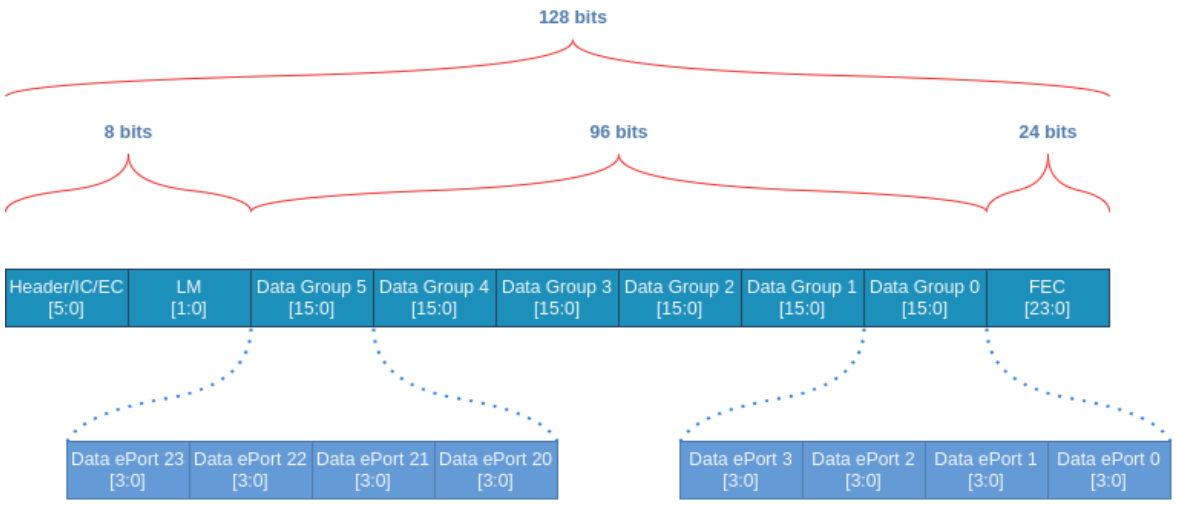
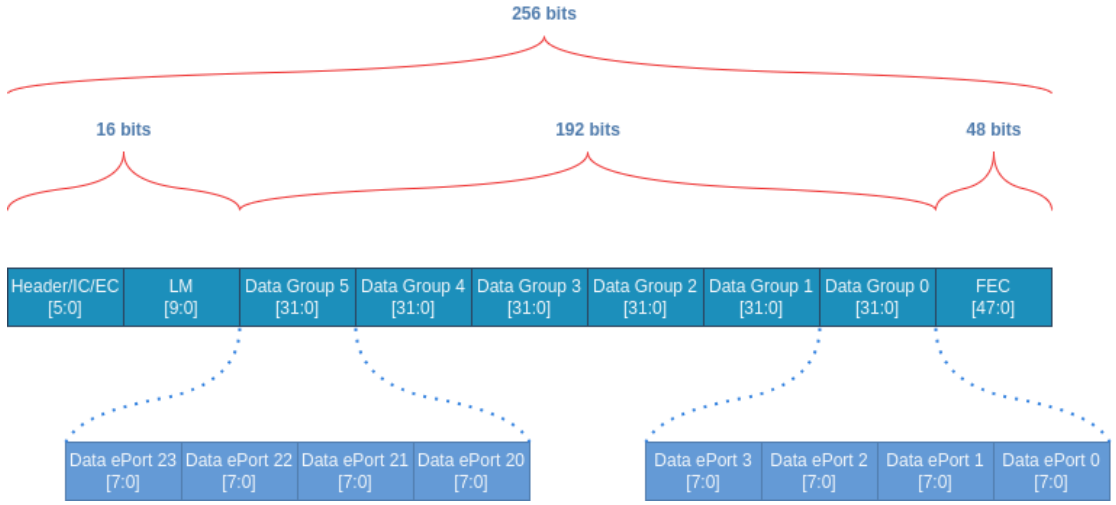
lpGBT ePort Routing

5.12Gbps



10.24Gbps



MOSAIX uplink						
Uplink bandwidth (Gbps)	5.12			10.24		
FEC Coding	FEC12			FEC12		
Tile bandwidth (Mbps)	40	80	160	40	80	160
Tiles per uplink [1]	48	48	24	48	48	48
Bits per tile	1	2	4	1	2	4
Tiles per ePort	2	2	1	2	2	2
Bits per ePort	4	4	4	8	8	8
Used bits per ePort	2	4	4	2	4	8
Bandwidth efficiency	50%	100%	100%	25%	50%	100%

1. To simplify routing scheme, 48 tiles are connected in instances where there are bandwidth enough to support a higher number of tiles.

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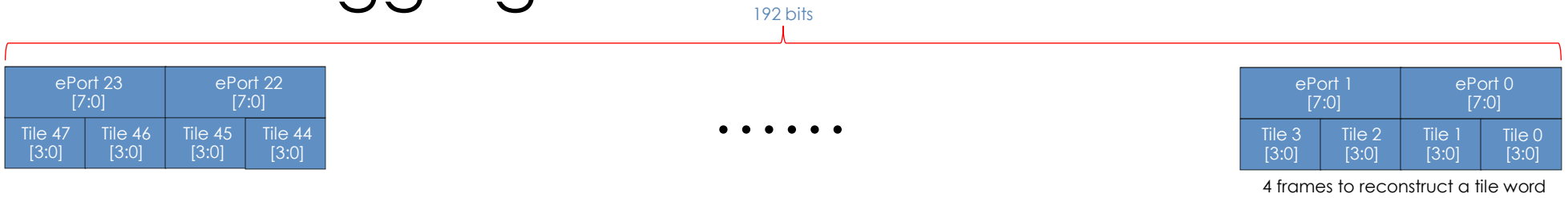
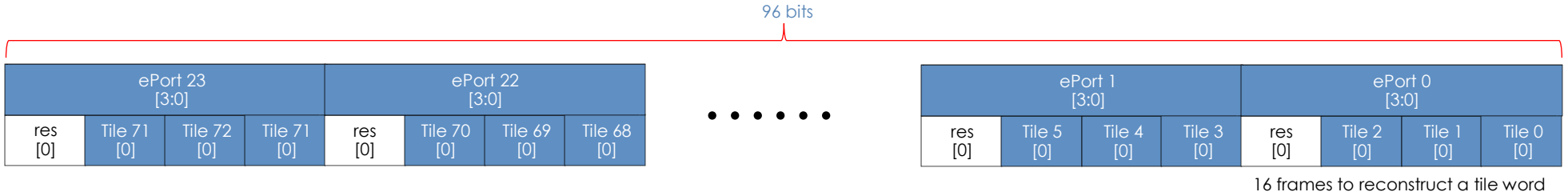
LEC Data Format & Aggregation

MOSAIX: 10.24 Gbps



LAS: 5.12 Gbps



Tile Data Words

READOUT PROTOCOL																
Word type	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDLE	1	1	0	0	0	1	0	1	IDLE config [7:0]							
LOCK	1	1	0	0	1	0	1	0	IDLE config [7:0]							
READOUT_STATUS_1	1	0	0	1	1	1	0	0	Integration Window Counter [15:8]							
READOUT_STATUS_2	1	1	1	1	IWC Checksum [3:0]				Integration Window Counter [7:0]							
TILE_HEADER	1	0	1	0	0	0	0	0	Unit Slice [4:0]					Tile [1:0]		T/B
REGION_HEADER	1	0	1	0	1	1	Region Address [1:0]		Integration Window Counter [7:0]							
DATA	0	Pixel Address Row [8:0]									Pixel Address Column [5:0]					
TILE_TRAILER	1	0	1	1	TRU Status Flags [3:0]				Packet Checksum [7:0]							
EMPTY_INTEGRATION_WINDOW	1	1	1	0	TRU Status Flags [3:0]				Integration Window Counter [7:0]							
DROPPED_INTEGRATION_WINDOW	1	1	0	1	TRU Status Flags [3:0]				Integration Window Counter [7:0]							
RECOVERY	1	0	0	1	0	0	1	1	'0							
RESERVED	1	0	0	0	RESERVED											

Drop
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