ePIC SVT Inner Barrel (IB) Signal Flexible Printed Circuits (FPCs)

WIP

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SVT WP3 Meeting

09.07.2026

OUTLINE

Introduction and Broad Boundary Conditions

Part – I: Calculations and Simulations

- Workflow and Caveats
- Max. Data Rate and Min. FPC Material
- Mitigation Strategies

Part – II: Experimental Characterisation

- Benchmark Studies with ITS3 Copper FPCs
- Test Setup with IB Aluminium FPCs
- First Results with LTU FPCs

INTRODUCTION

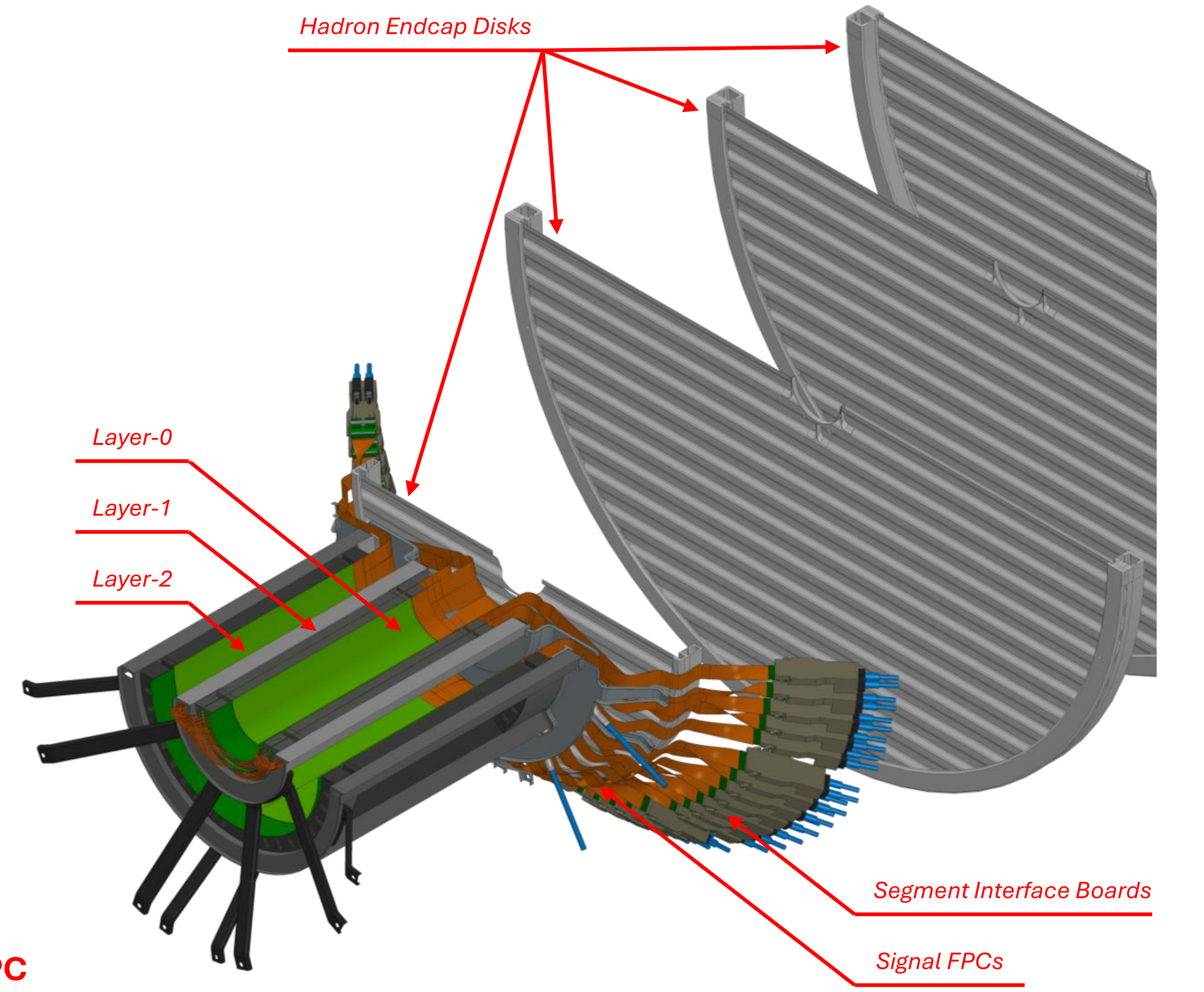
SVT-IB Signal FPCs

FPCs between MOSAIX (Left End-Cap) and Segment Interface Board

- MOSAIX LEC
  - 8 high-speed diff. lines for data throughput (5.12/10.24 Gb/s)
  - Serialiser with defined pre-emphasis settings
  - 8 low-speed diff. lines for sensor slow control (5 … 160 Mb/s)
- Segment Interface Board
  - VTRx+ Tx uplink for electrical-to-optical data conversion
  - VTRx+ Rx downlink for sensor slow control
  - Located outside the acceptance of the forward disks
- Additional signal loss sources
  - Wire bonds on LEC-end
  - ZIF connector on SIB-end

SVT-IB Parameters	Layer-0	Layer-1	Layer-2
Barrel Radius [mm]	38	50	126
No. of MOSAIX Segments	12	16	40
Signal FPC Length [mm]	415	387	310

Signal integrity of IB FPCs benchmarked w.r.t. eye properties of ITS3 FPC



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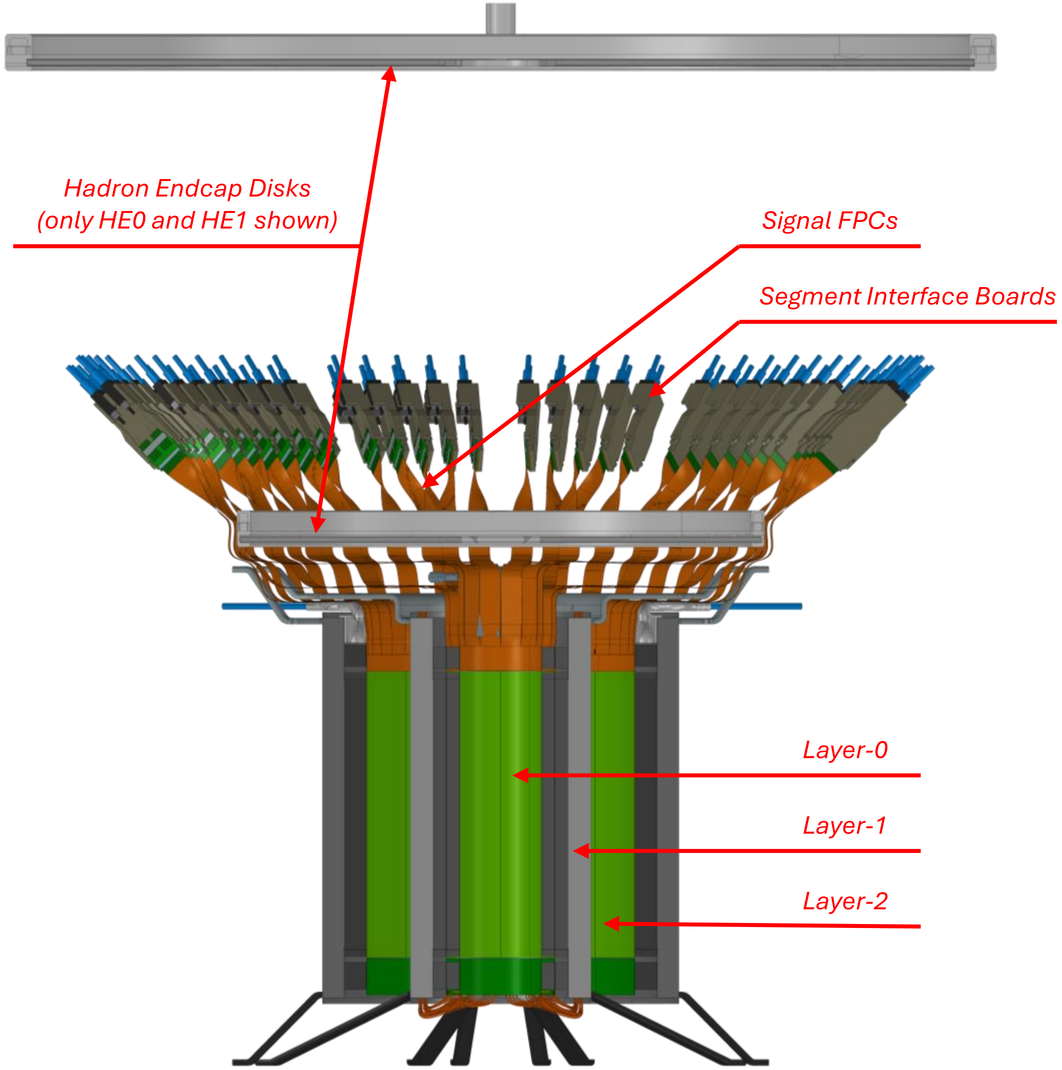
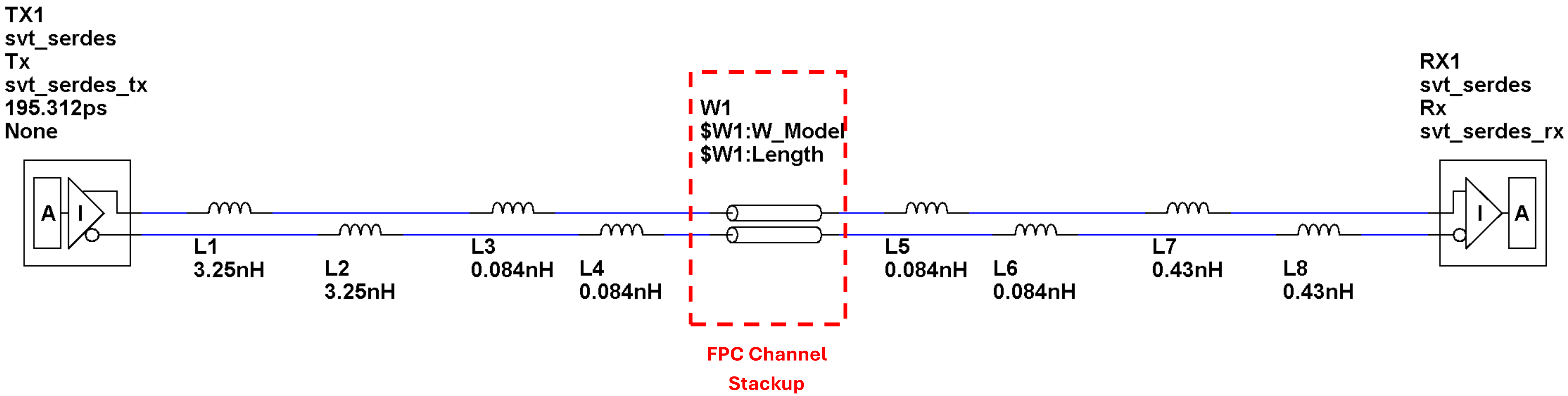


Part – I
Calculations And Simulations

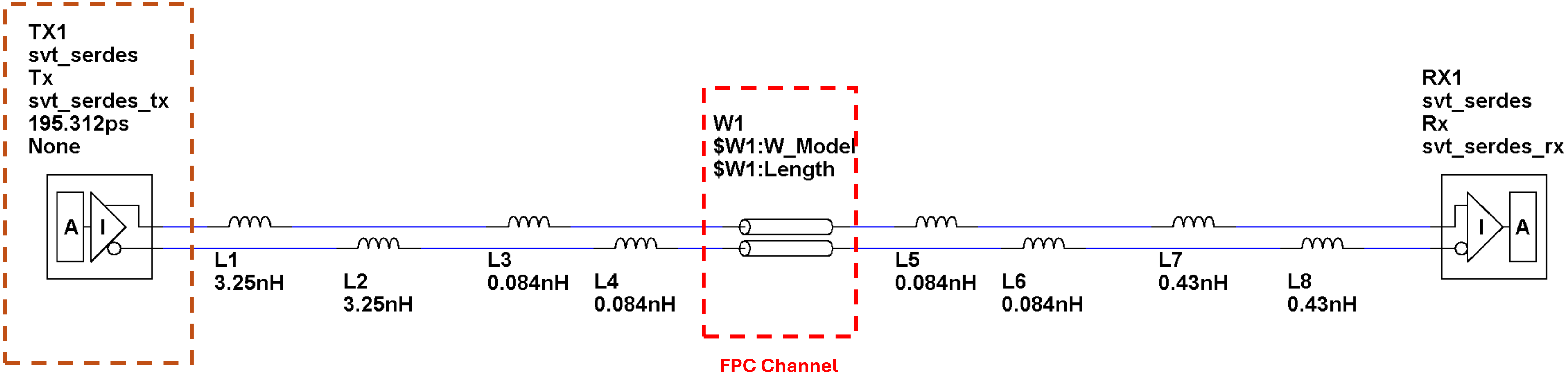
MATLAB CALCULATION FRAMEWORK



Various SVT-IB FPC stackups studied in conjunction with various elements from Tx to Rx in the signal transmission chain

- Based on MATLAB and Simulink's SerDes and Serial Integrity toolboxes

MATLAB Calculation Framework



MOSAIX Transmitter

FPC Channel Stackup

Various SVT-IB FPC stackups studied in conjunction with various elements from Tx to Rx in the signal transmission chain

- Based on MATLAB and Simulink's SerDes and Serial Integrity toolboxes
- **Transmitter (Tx):** MOSAIX-like serialiser with nominal jitter and pre-emphasis settings

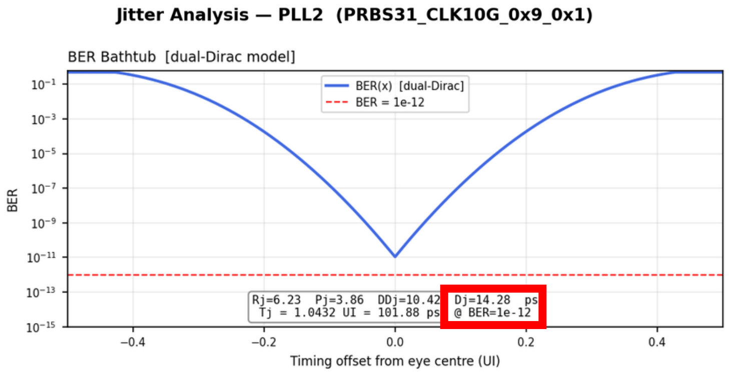
Setting Up Transmitter (GWT-PSI) – Jitter

Scenario	Total Jitter (TJ_{pp})	Random Jitter (RJ)			Deterministic Jitter (DJ_{pp})	
		σ_{RJ}	$Q = \sqrt{2} \cdot \mathrm{erfc}^{-1}(2 \cdot \mathrm{BER})$ (BER)	$2 \cdot Q \cdot \sigma_{RJ}$	Duty Cycle Distortion (DCD_{pp})	Residual DJ_{pp}
GWT_PSI Qualification Plan	0.300 UI	0.0100 UI	7.035 (1×10^{-12})	0.141 UI	0.050 UI	0.109 UI
GWT_PSI First Measurements	1.043 UI	0.0612 UI		0.860 UI	0.140 UI	
VTRx+ Tx Input Requirements	0.260 UI	0.0085 UI		0.120 UI	0.140 UI	
GWT_PSI Potential Performance	0.703 UI	0.0400 UI	7.035 (1×10^{-12})	0.563 UI	0.140 UI	

Safe to assume σ_{RJ} to be close to simulations and DJ_{pp} to remain consistent with first measurements

Test Name	Configuration	Acceptance Criteria	Reference
Tx Output Jitter (Intrinsic)	**Rate:** 10.24 Gbps **Pattern:** PRBS-31 **Pre-emph:** OFF (cfg=00)	**Total Jitter (TJ):** < 0.30 UI (standard) **Random Jitter (RJ):** $< 0.04\ \mathrm{UI}_{RMS}$ (simulation) $< 0.01\ \mathrm{UI}_{RMS}$ (standard) **Duty Cycle Distortion:** < 0.05 UI	**[OIF-CEI]** 11G-MR Tx Spec, Table 9-3. $RJ = 0.15\ \mathrm{UI}_{pp}/16 = 0.0094\ \mathrm{UI}_{RMS}$ derived from Uncorrelated High Probability Jitter req. **Note the big discrepancies between the standard and the simulation expectations, thus TJ requirement is probably too strict.**

GWT-PSI Chiplet Characterisation and Qualification Plan (2026) | Link



Q. Wittermans, ALICE ITS3 WP3 Meeting, 19.05.2026 | Link
Q. Wittermans, Private Communication, 16.06.2026
S. Caregari, ALICE ITS3 WP3 Meeting, 28.04.2026 | Link

Table 5: VTRx+ module electro-optical specifications.

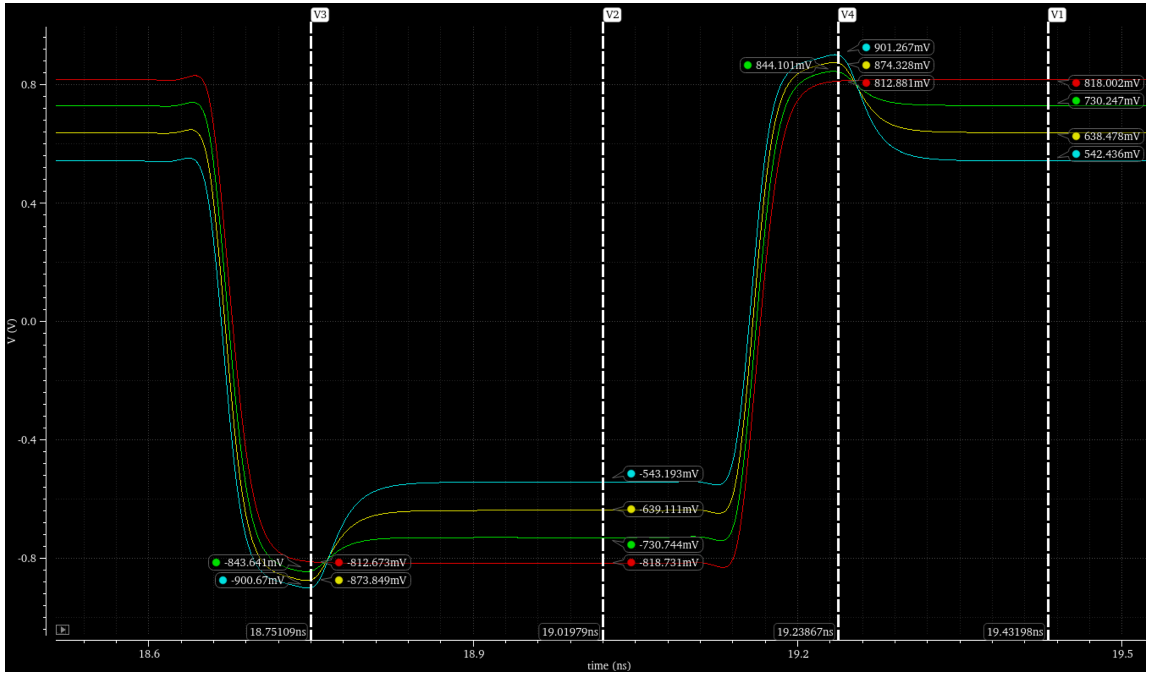
#	Specification	Min.	Typ.	Max.	Unit
4.2.1	Tx Differential input voltage	200		1200	mV
4.2.2	Tx Input rise/fall time[b]		30	40	ps
4.2.3	Tx Input Total Jitter[c]			0.26	UI
4.2.4	Tx Input Deterministic Jitter			0.14	UI
4.2.5	Tx Input Eye Mask	*see Table 6 & Figure 6*			
4.2.6	Tx Differential input impedance	90	100	110	Ω

Alan Prosser et al., Versatile Link Plus Technical Specification - Part 1, EDMS Document No.1719328 (2019)
J. Troska et al., Versatile Link+ Transceiver (VTRx+), EDMS Document No. 1719329 (2023) – v.2.9

Sam Palermo, ECEN720: High-Speed Links Circuits and Systems, Spring 2023, Texas A&M University | Link
Jitter Analysis: The dual-Dirac Model, RJ/DJ, and Q-Scale, Agilent White Paper (2004) | Link

Setting Up Transmitter (GWT-PSI) – Pre-Emphasis

Simulations by: Giacomo Ripamonti (CERN)
M. Rossewij (U. Utrecht), Private Communication, 08.06.2026
M. Rossewij, ALICE ITS3 WP3 Meeting, 09.06.2026 | Link



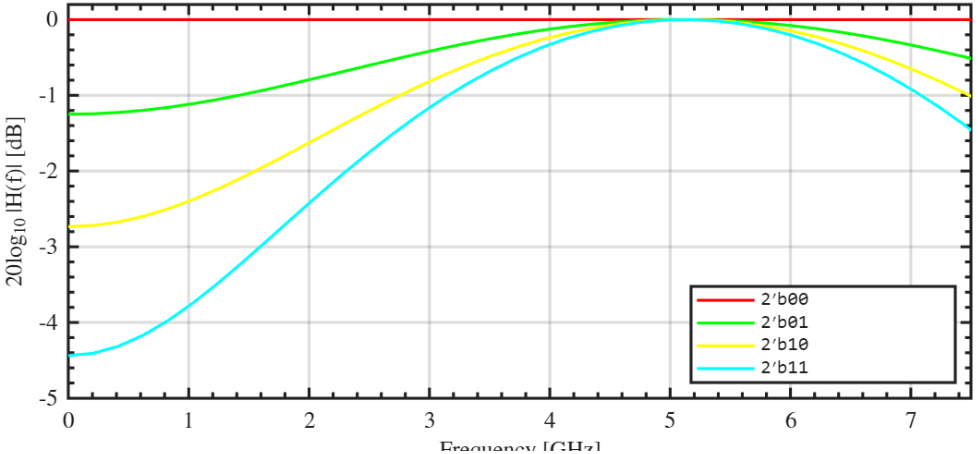
Pre-Emphasis Mode (`serializer_cfg_2`)			Cursor Tap (c_0)	Post-Cursor Tap (c_1)
(red)	Off	(2’b00)	+1.000	0.000
(green)	Mild	(2’b01)	+0.933	-0.067
(yellow)	Moderate	(2’b10)	+0.865	-0.135
(cyan)	Max	(2’b11)	+0.801	-0.199

- Feed Forward Equaliser (FEE) for transmitter pre-emphasis

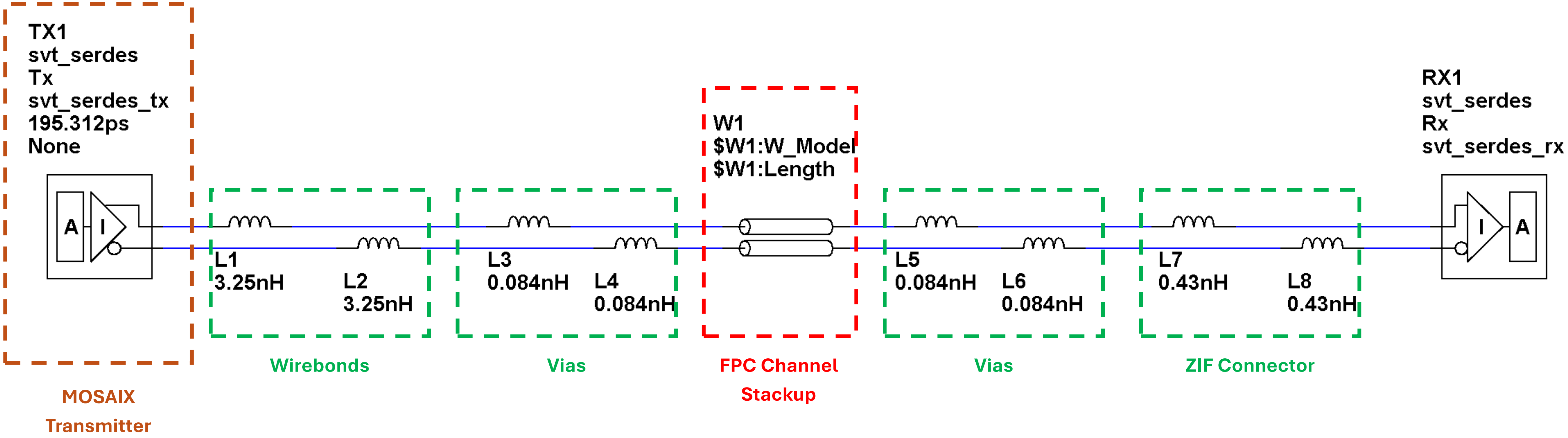
$$H(f) = \sum_k c_k \cdot e^{-j2\pi f k T_{sym}}$$

- For GWT-PSI transmitter with two taps, 1 cursor and 1 post-cursor
  - k : Tap indices [0, +1]
  - T_{sym} : Symbol period or 1 UI (1/10.24Gbps = 97.66 ps)
  - c_k : Tap coefficients $(\sum_k |c_k| = 1)$

$$c_0 = \frac{|V_{steady}| + |V_{peak}|}{2 \cdot |V_{peak}|} \qquad c_1 = \frac{|V_{steady}| - |V_{peak}|}{2 \cdot |V_{peak}|}$$



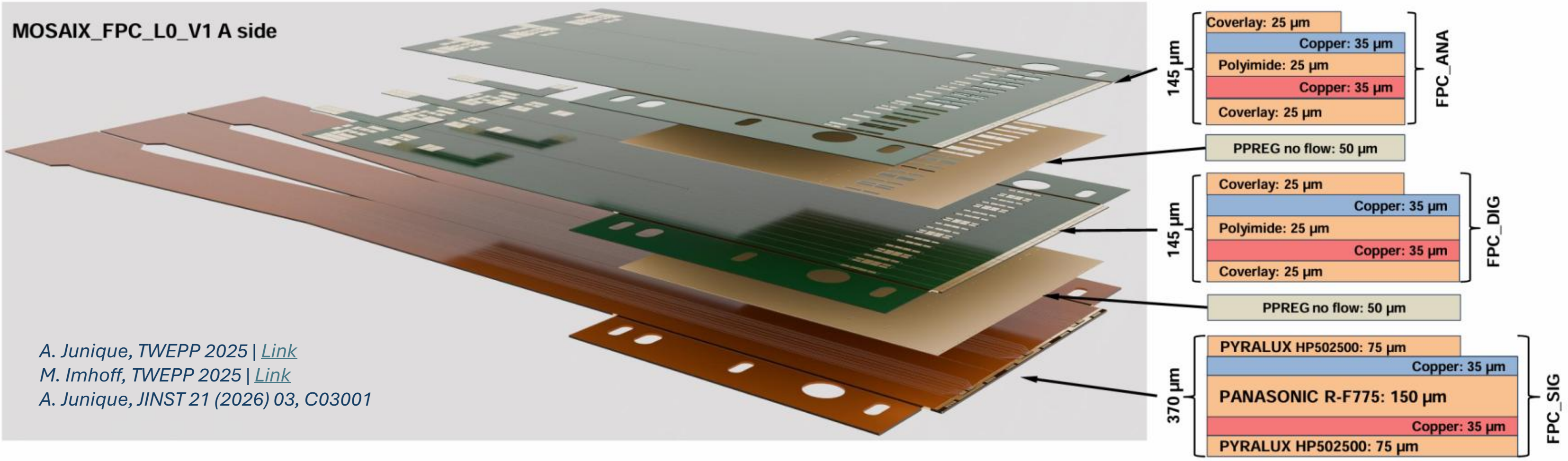
MATLAB Calculation Framework



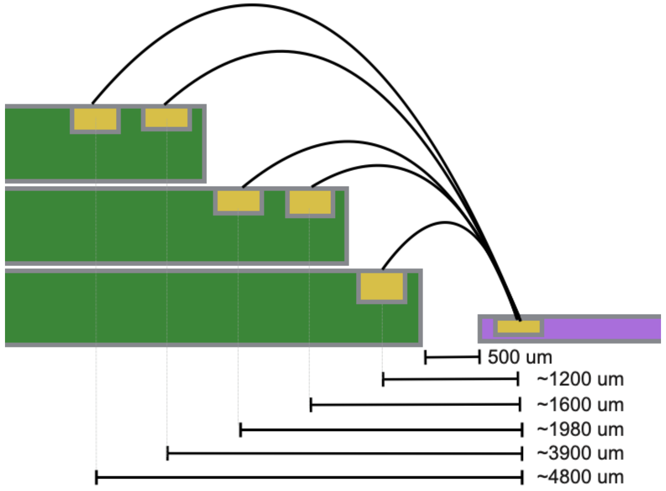
Various SVT-IB FPC stackups studied in conjunction with various elements from Tx to Rx in the signal transmission chain

- Based on MATLAB and Simulink's SerDes and Serial Integrity toolboxes
- **Transmitter (Tx):** MOSAIX-like serialiser with nominal jitter and pre-emphasis settings
- **Connectors and Vias:** Inductances caused from wirebonds (LEC-end), ZIF connector (SIB-end)

Wirebonds b/w MOSAIX And Signal FPC



A. Junique, TWEPP 2025 | Link
M. Imhoff, TWEPP 2025 | Link
A. Junique, JINST 21 (2026) 03, C03001



D. Colella (Uni. & INFN Bari), Private Communication, 09.06.2026

- Signal FPC is at the bottom of the FPC stackup, i.e., shortest bond wire $\lesssim$ 3 mm
- Inductance (L) for a straight bond wire
  - r : Bond wire radius (25 µm / 2 = 12.5 µm)
  - l : Bond wire length (3 mm)
  - μ_0 : Permeability of free space (1.2566 µH/m)

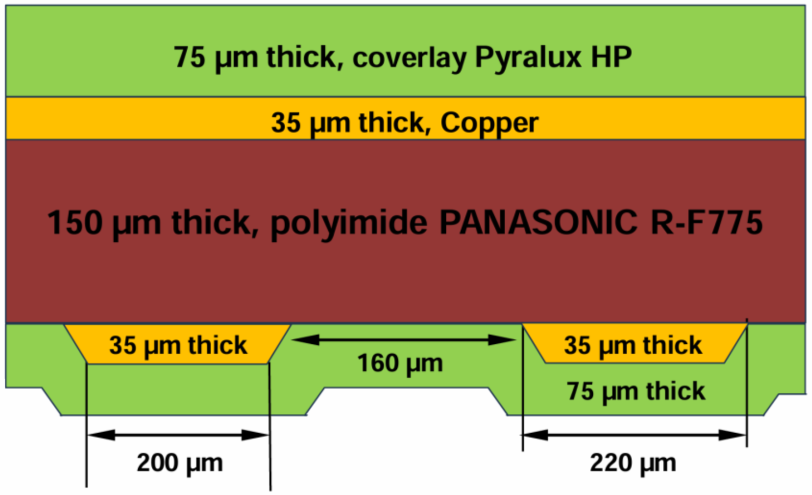
$$L = \frac{\mu_0}{2\pi} \times l \times \left[\ln\left(\frac{l}{r} + \sqrt{1 + \frac{l^2}{r^2}} \right) - \sqrt{1 + \frac{r^2}{l^2}} + \frac{r}{l} + \frac{1}{4} \right] \approx \frac{\mu_0}{2\pi} \times l \times \left[\ln\left(\frac{2l}{r} \right) - 0.75 \right]$$

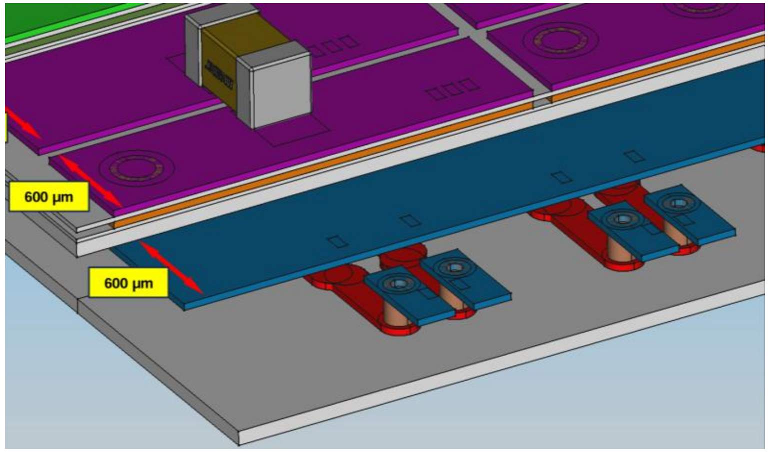
For the signal FPC, the bond wire inductance is ≈ 3.25 nH, or ≈ 1 nH/mm

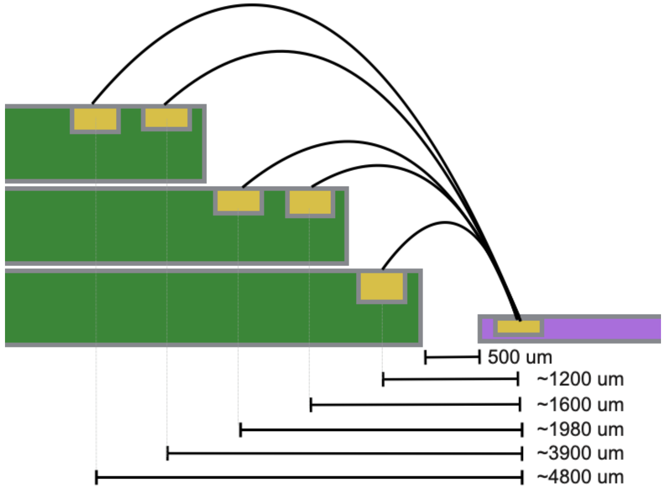
Xiaoning Qi, PhD Dissertation, Stanford University (2001) | Link
Joerg Berkner, Klaus-Willi Pieper, Bondwire Inductance, Infineon | Link
Straight-wire model overestimates the inductance by 10 to 50%

VIAS B/W FPC SIGNAL AND RETURN PLANE

A. Junique, TWEPP 2025 | Link
A. Junique, JINST 21 (2026) 03, C03001
A. Junique, ALICE ITS3 WP6 Meeting, 14.02.2024 | Link







D. Colella (Uni. & INFN Bari), Private Communication, 09.06.2026

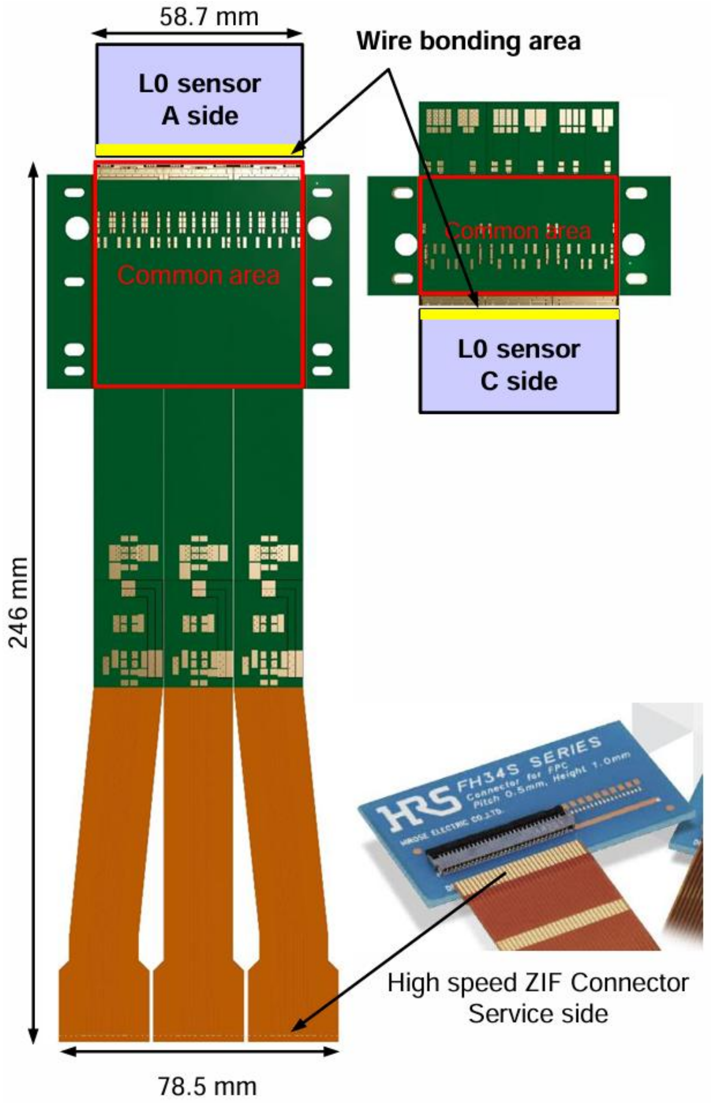
- Through-vias to bring signal and return layers on the same plane
- Inductance (L) for through via
  - r : Via radius (eyeballing to ≈ 50 µm)
  - h : Via height (≈ dielectric height = 150 µm)
  - μ_0 : Permeability of free space (1.2566 µH/m)

$$L = \frac{\mu_0}{2\pi} \times h \times \left[\ln\left(\frac{h}{r} + \sqrt{1 + \frac{h^2}{r^2}} \right) - \sqrt{1 + \frac{r^2}{h^2}} + \frac{3r}{2h} \right] \approx \frac{\mu_0}{2\pi} \times h \times \left[\ln\left(\frac{2h}{r} \right) + 1 \right]$$

For the signal FPC, the via inductance is ≈ 0.084 nH

M.E. Goldfarb and R.A. Pucel, IEEE Microwave and Guided Wave Letters (Vol.1, Iss.6, June 1991) | Link
Cadence System Analysis, Is There a Via Inductance Rule of Thumb? | Link
Samtec White Paper on Current Distribution, Resistance, and Inductance in Power Connectors, DesignCon 2020 | Link
Approximation considers loop inductance in addition to the self inductance from the IEEE paper

ZIF Connector b/w Signal FPC And SIB

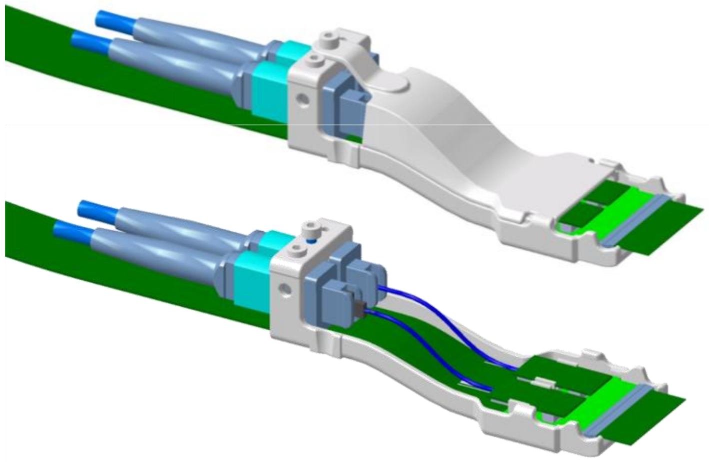


A. Junique, TWEPP 2025 | Link
A. Junique, JINST 21 (2026) 03, C03001
ZIF Connector Part Nr. FH34SRJ-40S-0.5SH | Link

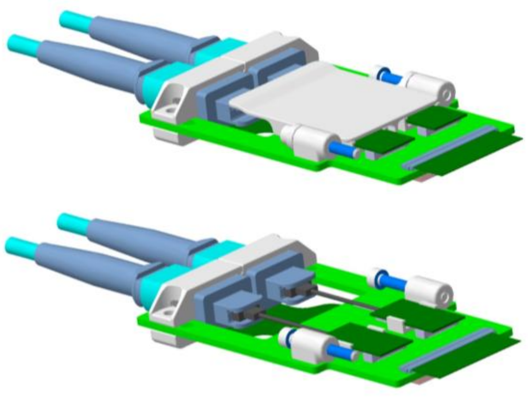
- Treating connector's contact path as a transmission line embedded in plastic
- Inductance (L) for through via
  - Z : Contact's local impedance (50 Ω)
  - l : Conductor length b/w SIB pad and FPC pad (≈ 1.5 mm)
  - ε_r : Plastic dielectric constant (≈ 3)

$$L = Z \times \tau = Z \times \frac{l}{v} = Z \times \frac{l}{c/\sqrt{\varepsilon_r}}$$

Equivalent inductance for ZIF connector's pin is ≈ 0.43 nH



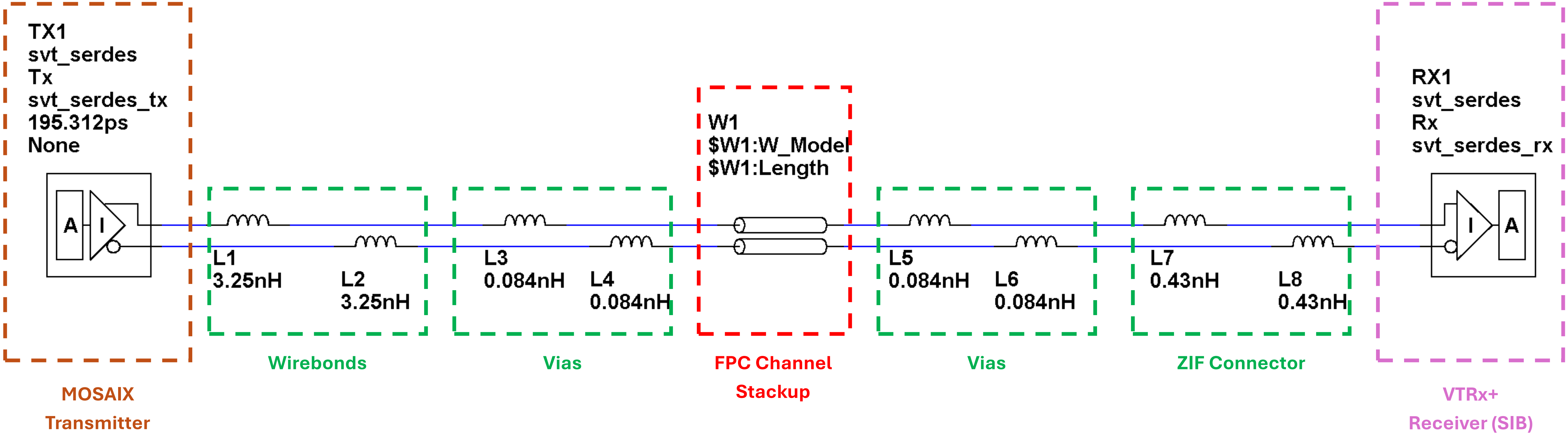
Segment Interface Board v-B2



Segment Interface Board v-A2

M. Angeletti, ALICE ITS3 WP6 Meeting, 17.09.2025 | Link

MATLAB CALCULATION FRAMEWORK



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- **Transmitter (Tx):** MOSAIX-like serialiser with nominal jitter and pre-emphasis settings
- **Connectors and Vias:** Inductances caused from wirebonds (LEC-end), ZIF connector (SIB-end)
- **Receiver (Rx):** Eye behaviour (area) comparison with ITS3 FPCs on the SIB with VTRx+

Setting Up Receiver (VTRx+) Eye Mask

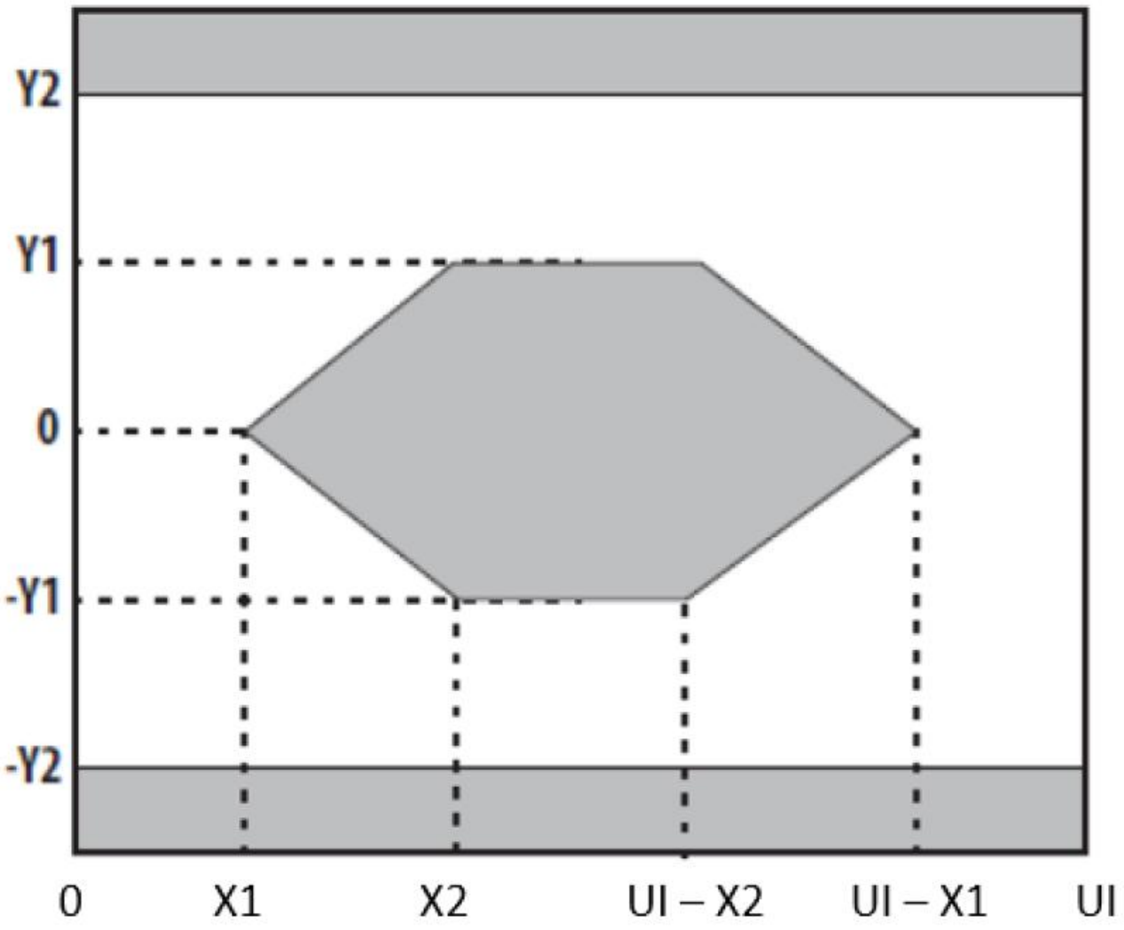


Figure 7.1 Mask 1

- Mask specs based on Optical Internetworking Forum's guidelines (OIF-CEI-05.3 Clause 8) for NRZ baud rates of 9.95 … 11.2 Gsym/s

Implementation Agreement OIF-CEI-03.0, Common Electrical I/O (CEI) (2011) | Link

Table 7.2. Uplink Electrical and optical eye mask for VTRx+ and TRx (UI = 97.66 ps)

		X1	X2	X3	Y1	Y2	Y3
7.2.1	VTx+ Elec. Input @TP1; (Mask 1, Fig. 7.1)	X1	X2	X3	Y1	Y2	Y3
	Value	10.7	30.3		95	350	
	Unit	ps	ps		mV	mV	
7.2.2	VTx+ Optical Output @TP2 (Mask 3, Fig. 7.3)						
	Value	22.5	33.2	42	0.27	0.35	0.40
	Unit	ps	ps	ps	Norm. Amp.*	Norm. Amp.*	Norm. Amp.*
7.2.3	COTS Rx Elec. Output @TP4 (Mask 2, Fig. 7.2)						
	Value	28.3	48.8		150	425	
	Unit	ps	ps		mV	mV	

*Normalized Amplitude

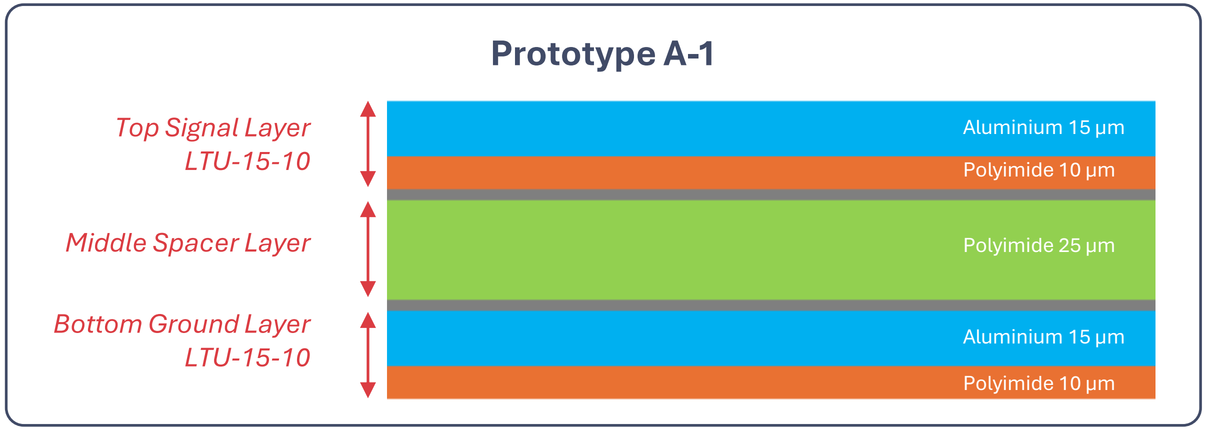
Alan Prosser et al., Versatile Link Plus Technical Specification - Part 1, EDMS Document No.1719328 (2019)
J. Troska et al., The Versatile Link+ Application Note, EDMS Document No. 2149674 (2021)

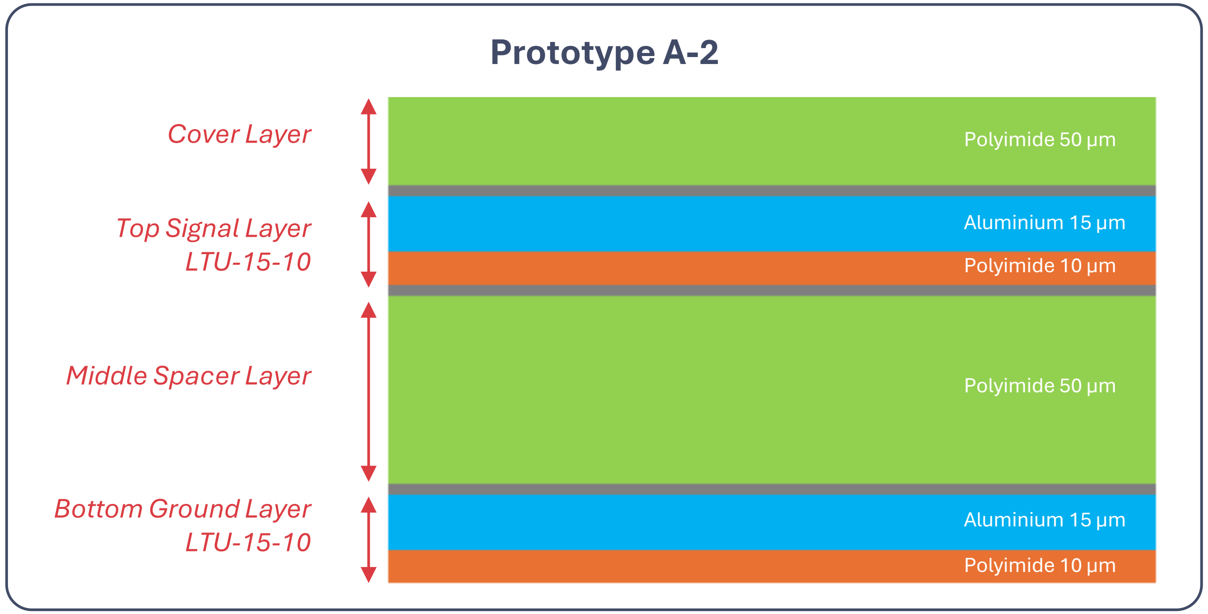
Maximum Data Rates And Minimum FPC Material

SVT-IB signal FPCs from LTU-Kharkiv

- Lightest option based on 15 µm thick aluminium per layer
- Comparable variants without (A1) or with cover layer (A2)

Properties	Variant A1	Variant A2
Differential Impedance [Ω]	100	
Trace Width [µm]	70, 60	
Differential Separation [µm]	80	
Cover Layer Thickness [µm]	N/A	50
Dielectric Thickness [µm]	25 + 10	50 + 10

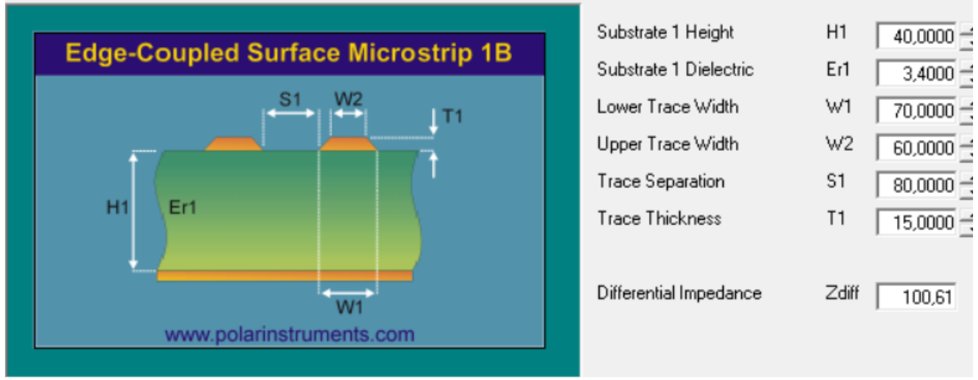




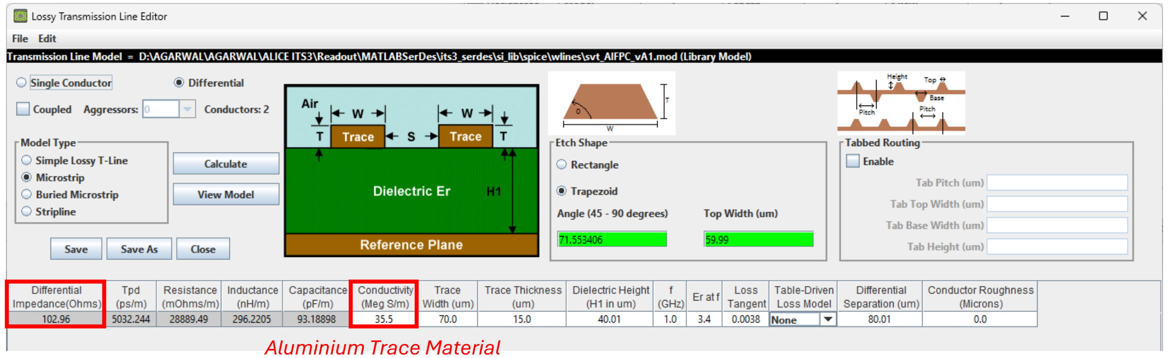
Implementing SVT Signal FPC

I. Tymchuk et al., Uni Trieste - STFC DL - RPE LTU
ePIC SVT IB work meeting, 11.07.2025

Calculations by LTU (Prototype A1)

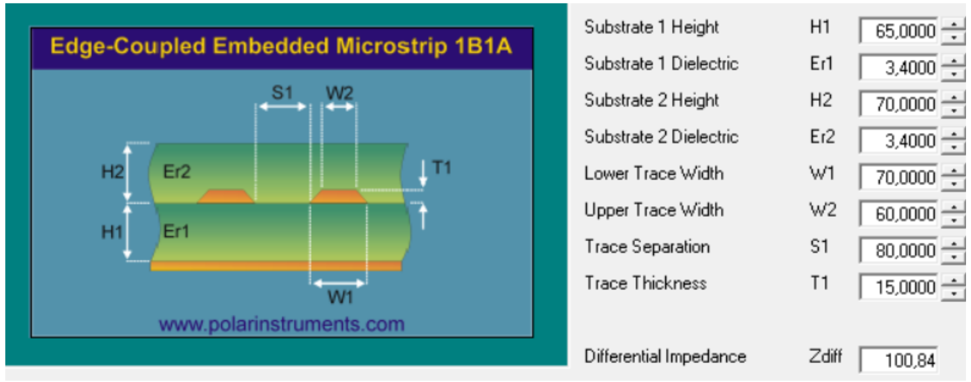


MATLAB Simulations

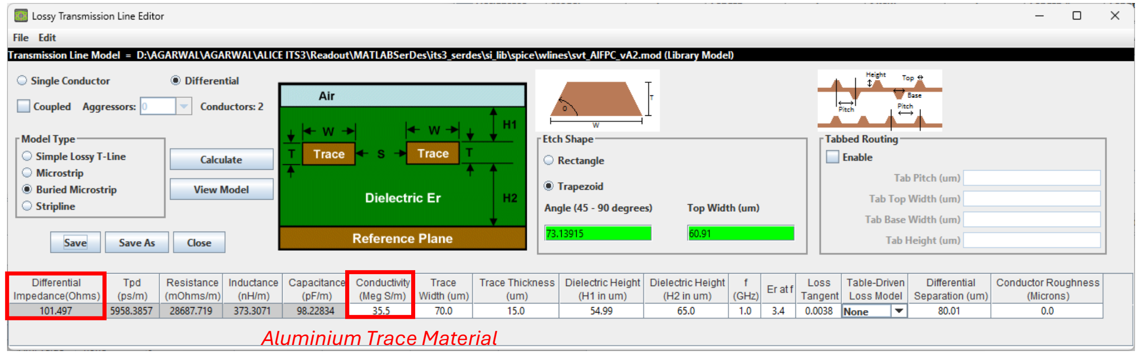


Comparable differential impedance (≈ 100Ω)

Calculations by LTU (Prototype A2)



MATLAB Simulations

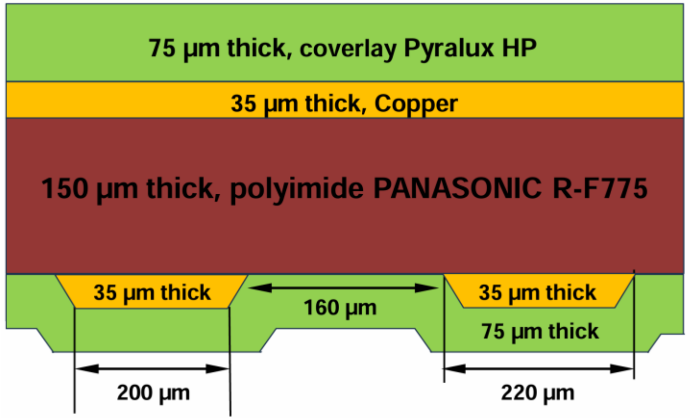


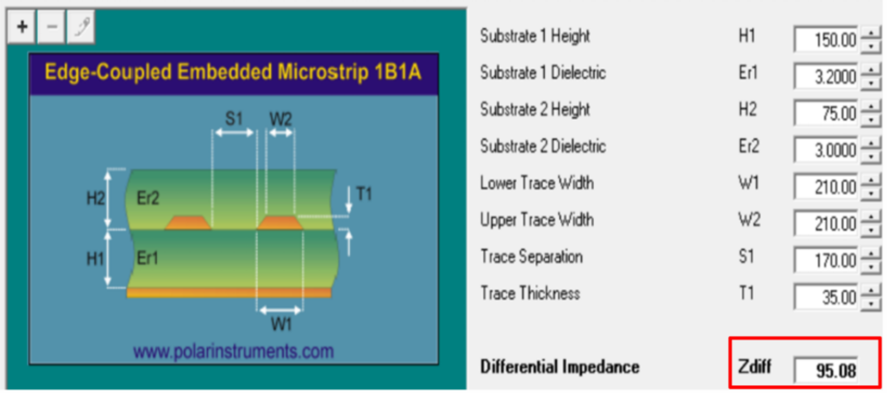
Comparable differential impedance (≈ 100Ω)

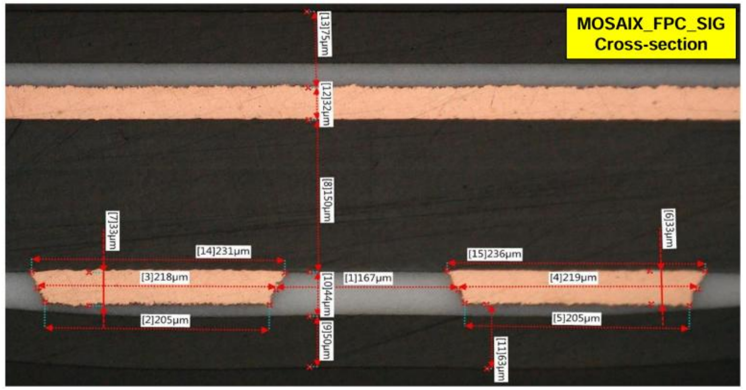
Implementing ITS3 Signal FPC

A. Junique's Calculations and Observations

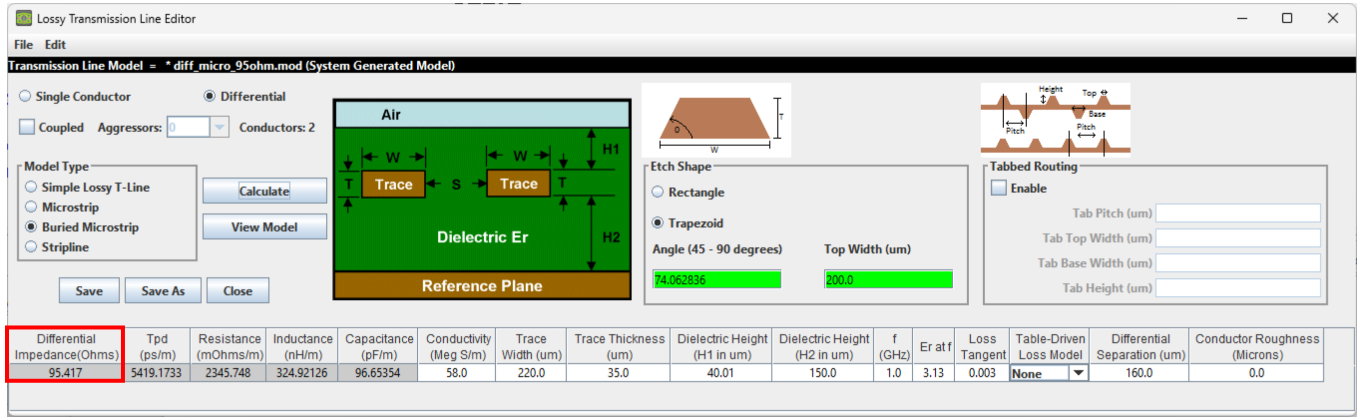
A. Junique, TWEPP 2025 | Link







MATLAB Simulations



- MATLAB uses a relatively simple FPC simulator, which requires calculating effective dielectric constant ($\varepsilon_{r\,\mathrm{eff}}$) of the FPC cross-section

$$\varepsilon_{r\,\mathrm{eff}} = \frac{\varepsilon_{r_1} \cdot h_1 + \varepsilon_{r_2} \cdot h_2}{h_1 + h_2} = 3.13$$

For ITS3, $\varepsilon_{r_1} = 3.2$, $h_1 = 150\,\mu m$; $\varepsilon_{r_2} = 3.0$, $h_2 = 75\,\mu m$

Comparable differential impedance (≈ 95Ω)

Maximum Data Rates And Minimum FPC Material

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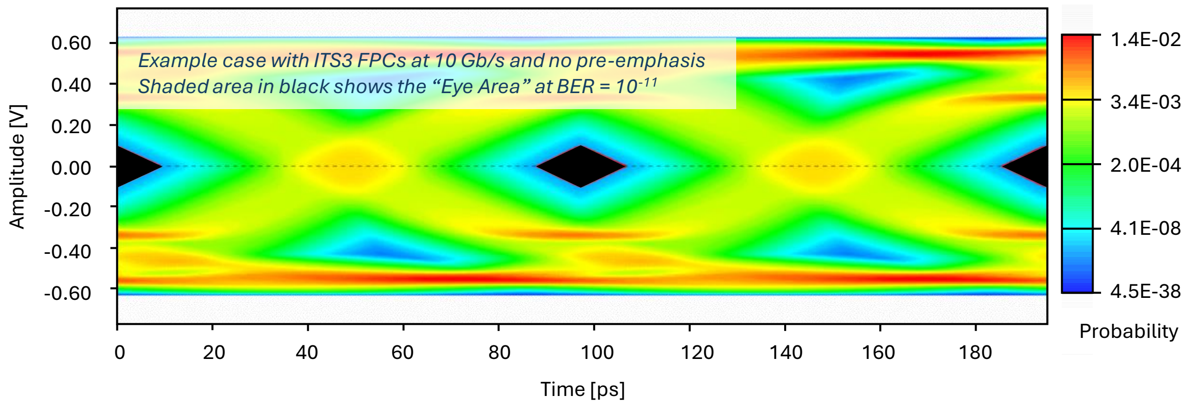
- Signal integrity compared to ITS3 FPCs in terms of "Eye Area" contour at target BER of 10^{-11}



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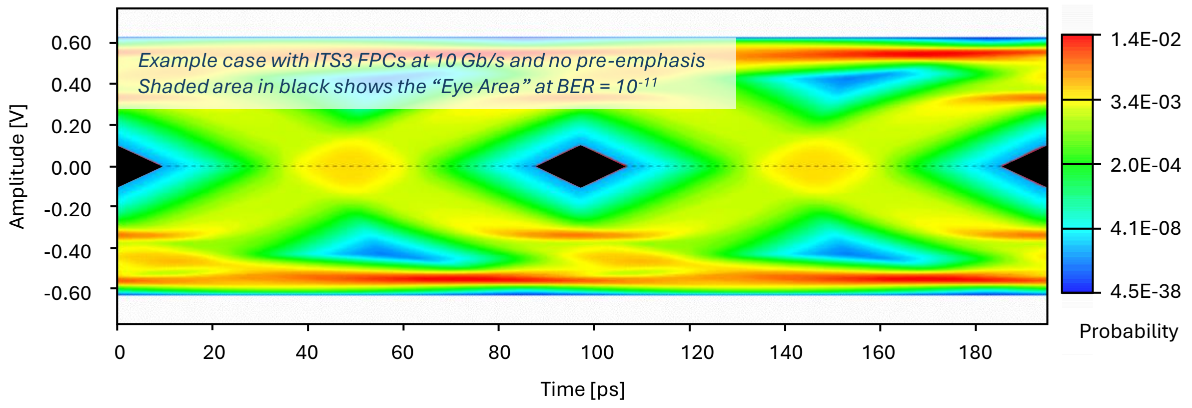
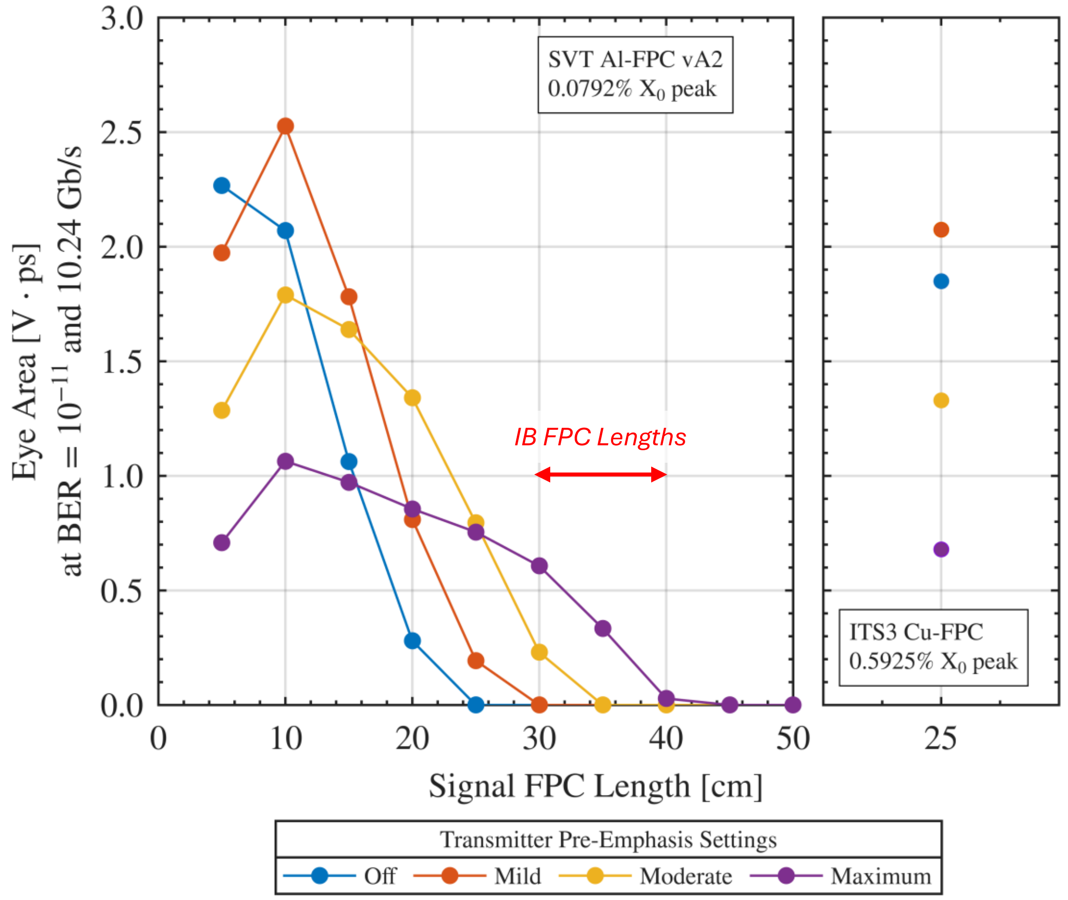


Eye is effectively close for IB FPCs (≈ 40 cm long) at max. data rates (10 Gb/s) and min. FPC material (15 µm Al)

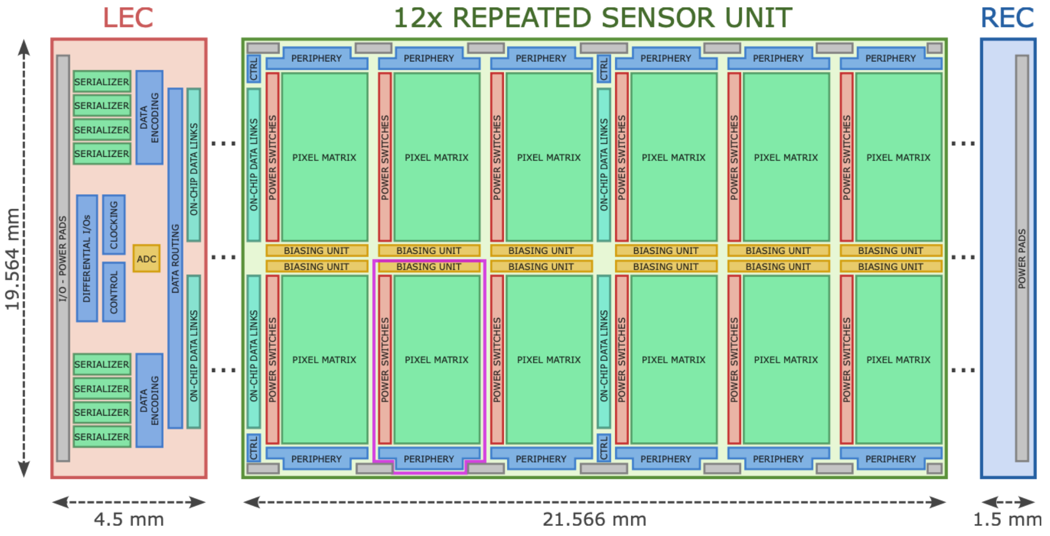


MITIGATION #1: LOWER DATA RATES

Configurable high-speed data transmission from MOSAIX

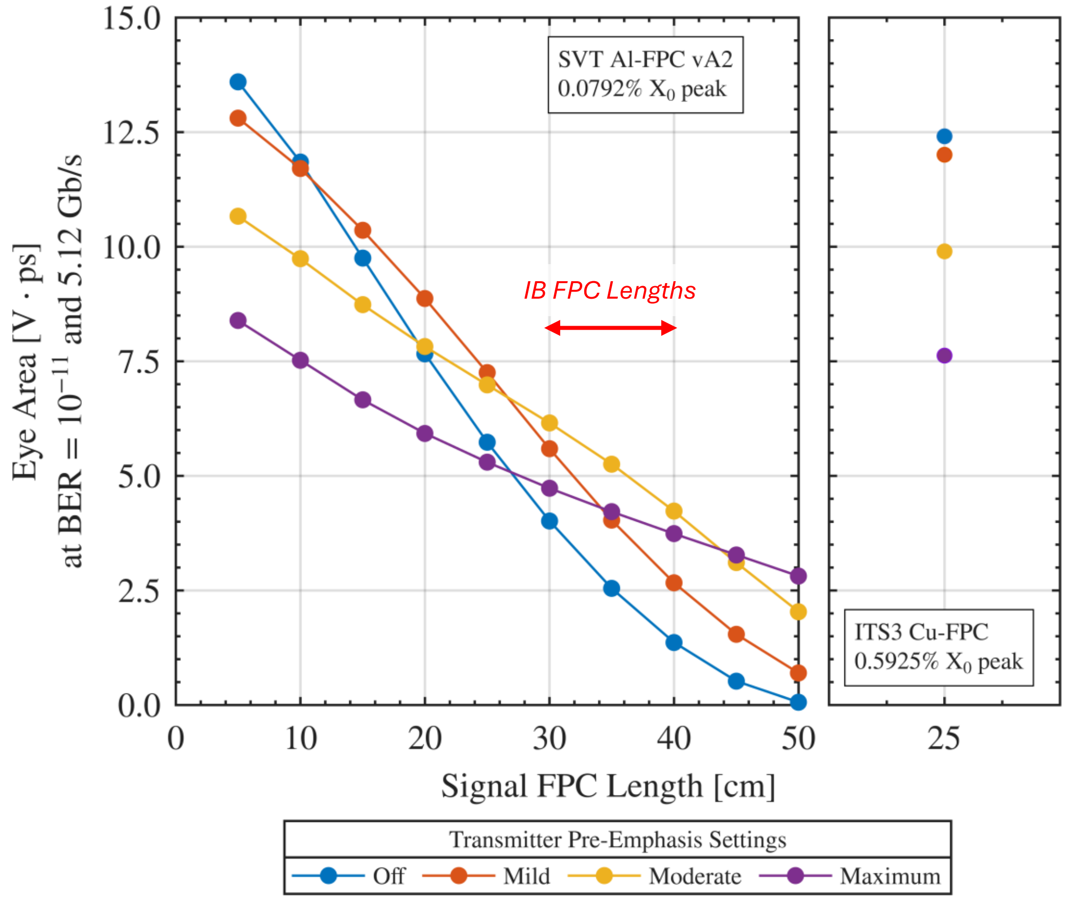
- Tiles (self-contained sensor block) can throughput 80 or 160 Mb/s
- Scenario nr. 2 and 4 allow MOSAIX to operate at 5.12 Gb/s

Parameter	Scenario 1	Scenario 2	Scenario 3	Scenario 4
Uplink Data Rate [Gb/s]	10.24	5.12	10.24	5.12
Tile Serialiser Speed [Mb/s]	160	160	80	80
Tiles per Uplink	48	24	48	48
Uplink Required	3	6	3	3



MOSAIX ASIC Documentation - https://mosaixdoc.docs.cern.ch/

Lowering transmitter data rates from 10.24 Gb/s to 5.12 Gb/s results in Eye Area > 0 at BER = 10^{-11} for ≈ 40 cm long IB FPCs



Mitigation #2: Higher FPC Material

Maximising trace cross-section to minimise conductor loss

- Conductor loss is the dominating contributor to signal loss
- Matching conductor loss between the FPCs, i.e., IB Al and ITS3 Cu

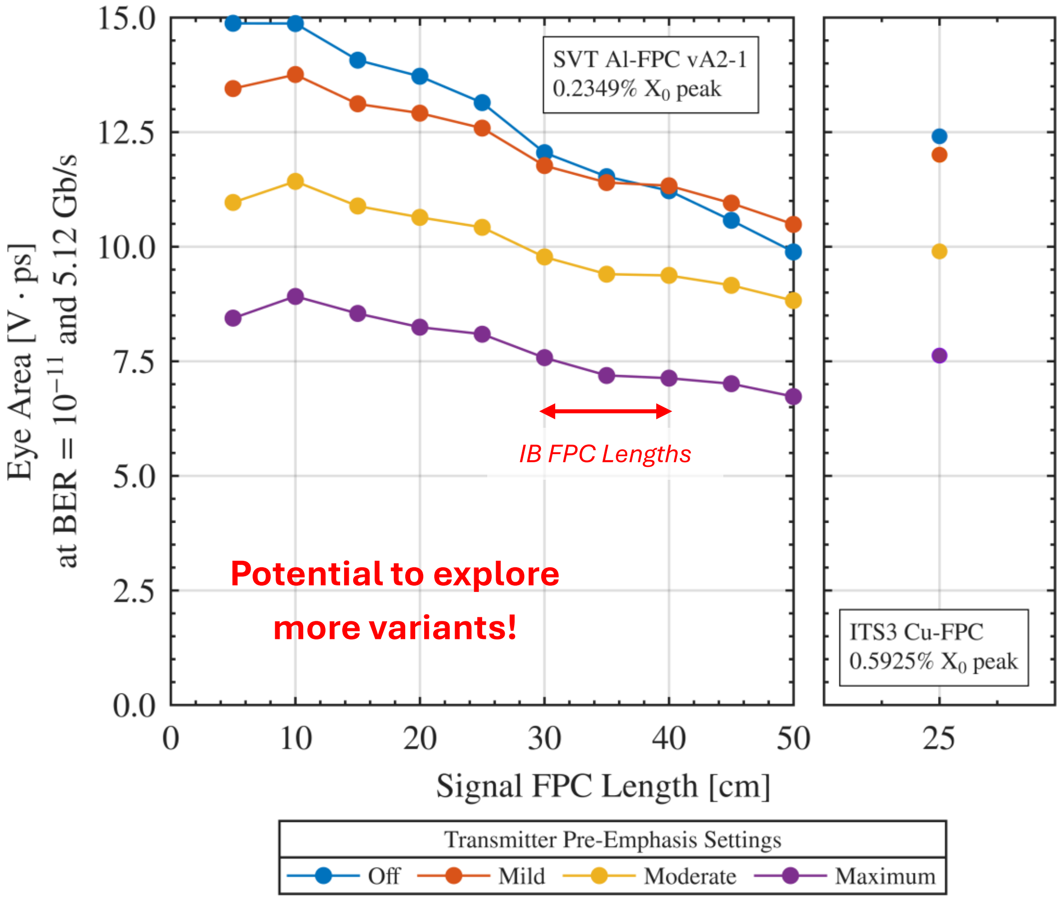
$$\alpha_C \propto \frac{\sqrt{\rho}}{w+t} \cdot l$$

$$\Rightarrow (w+t)_{IB} = (w+t)_{ITS3} \cdot \frac{l_{IB}}{l_{ITS3}} \cdot \sqrt{\frac{\rho_{IB}(\mathrm{Al})}{\rho_{ITS3}(\mathrm{Cu})}} \approx 500\ \mu m$$

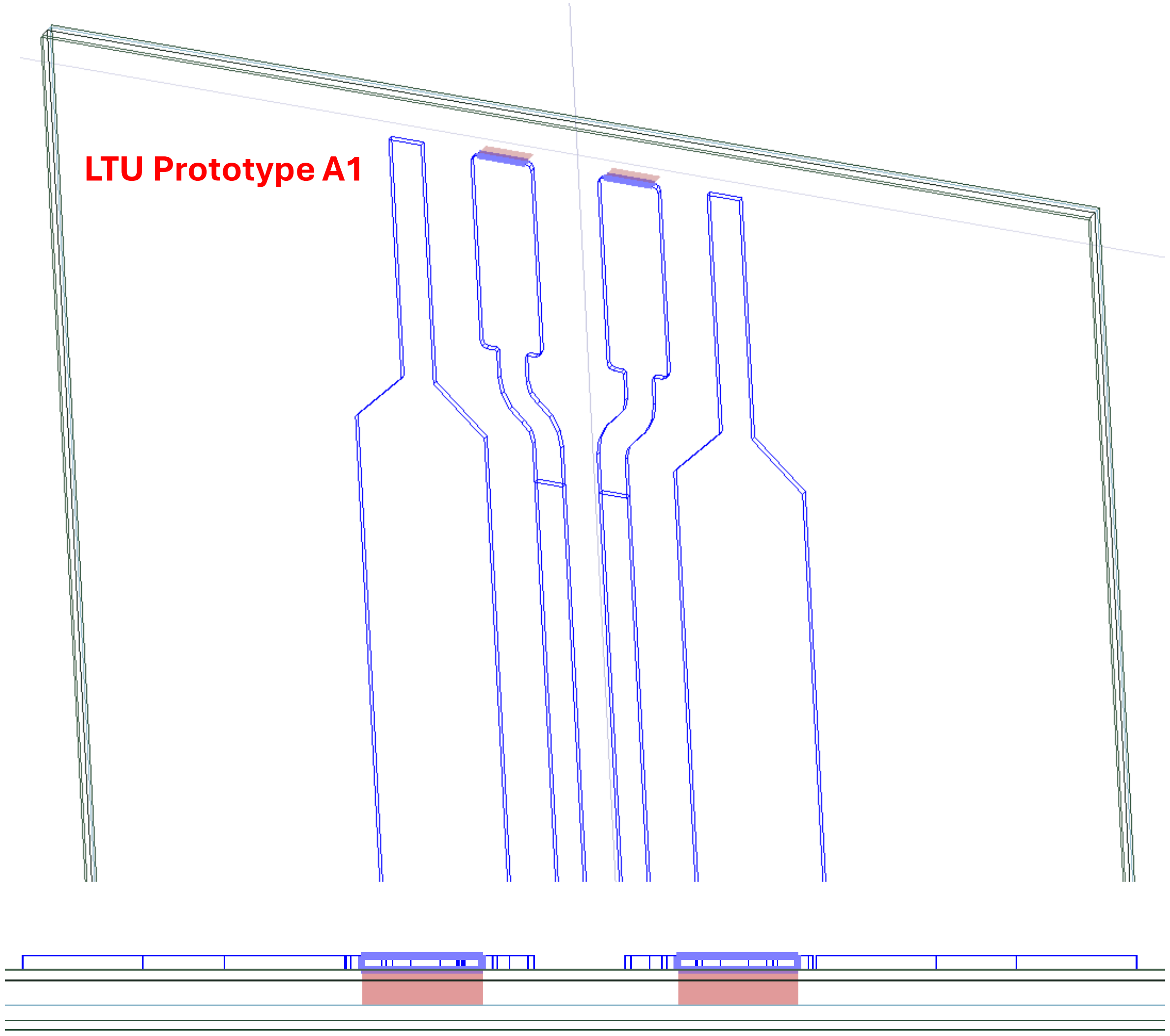
- Constraints to maximise trace cross-section and fill factor:
  - Trace width → MOSAIX pad layout and slow control lines
  - Trace thickness → Available LTU foils

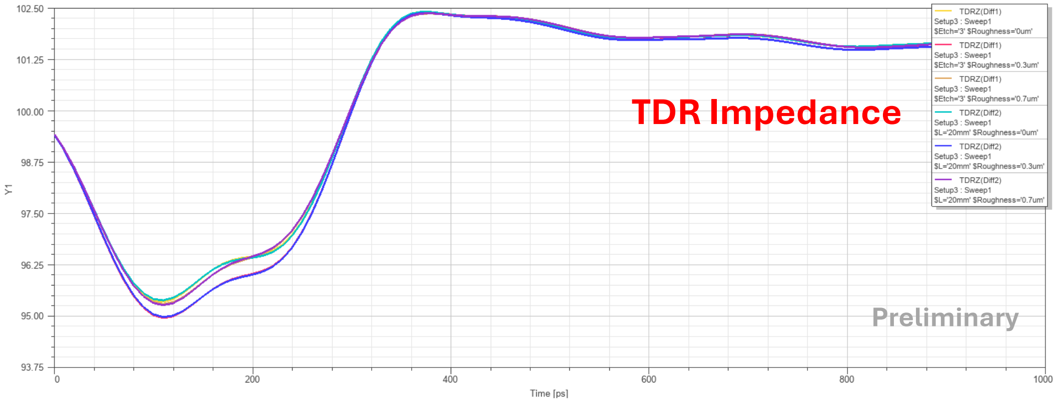
Properties	SVT IB Aluminium Variant A2	SVT IB Aluminium Variant A2-1	ITS3 Copper
Differential Impedance [Ω]		≈ 100	
Trace Thickness [µm]	15	50	35
Trace Width [µm]	70, 60	350, 310	220, 200
Differential Separation [µm]	80	300	160
Cover Layer Thickness [µm]	50	50	40
Dielectric Thickness [µm]	50 + 10	250 + 20	150

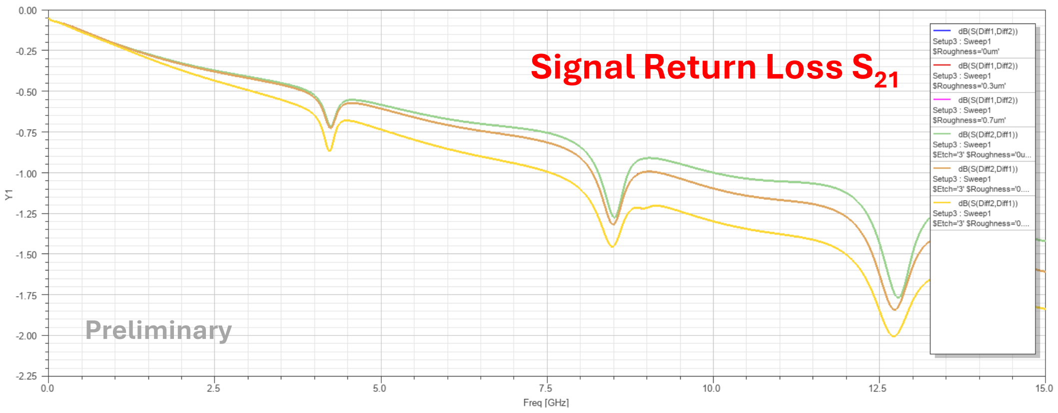
Increasing the FPC trace cross-section can sizably open the Eye Area at BER = 10^{-11} and 5.12 Gb/s for ≈ 40 cm long IB FPCs



ANSYS Signal Integrity Simulations







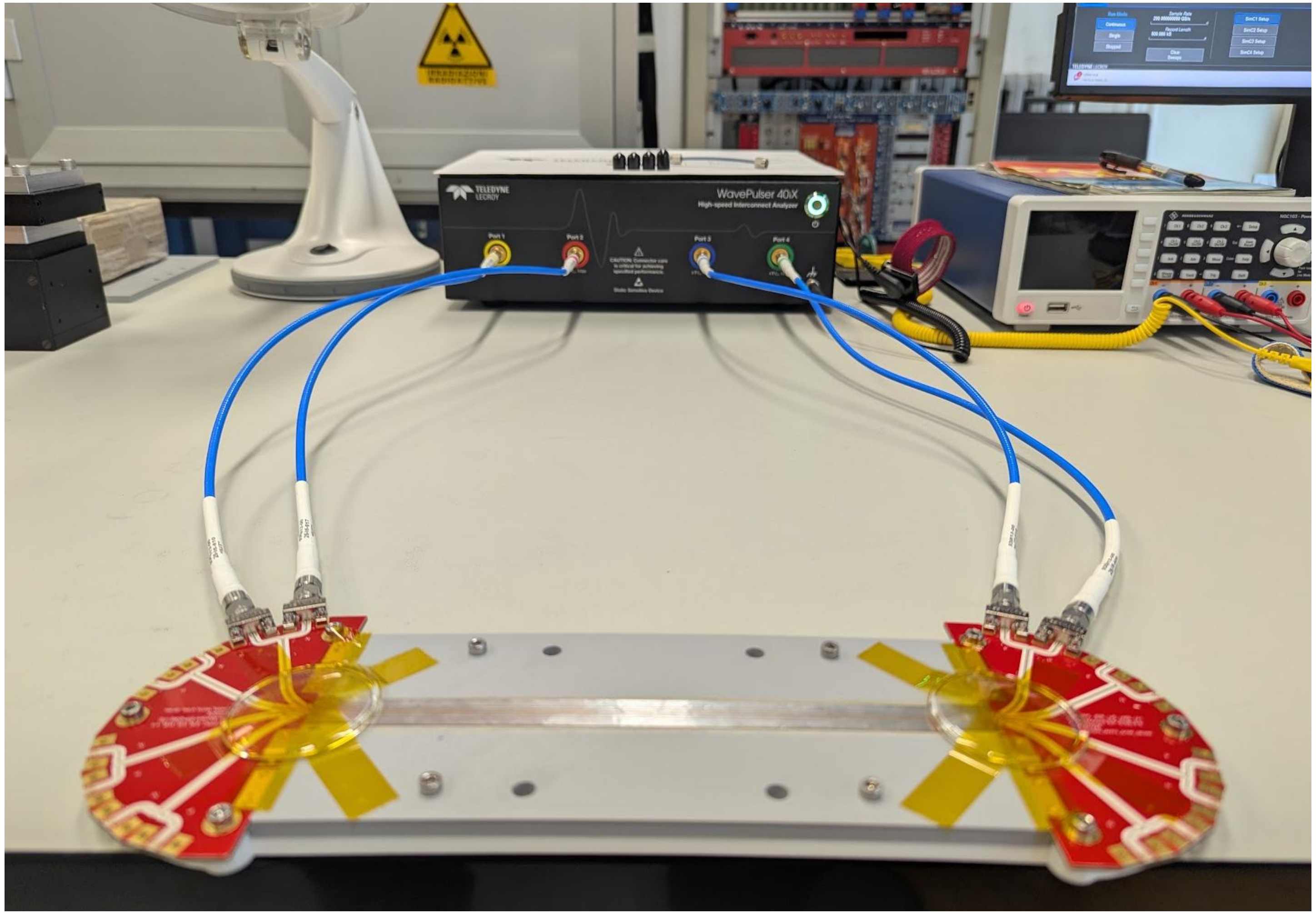
ANSYS simulations based on (quasi-) realistic CAD drawings

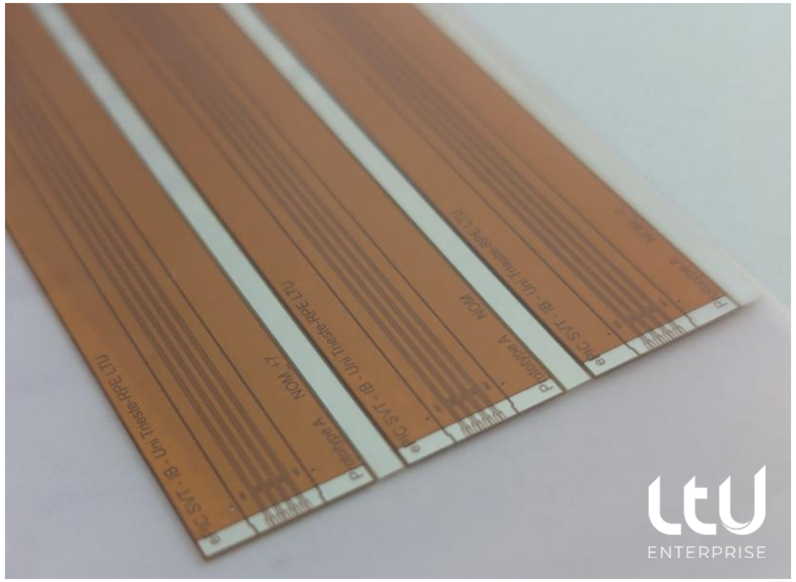
- Imports manufacturer drawings, thus minimising assumptions
- Allows understanding subtler features, such as trace roughness, etching factors and skin depth effects

Part – II
Experimental Characterisation

First LTU Samples

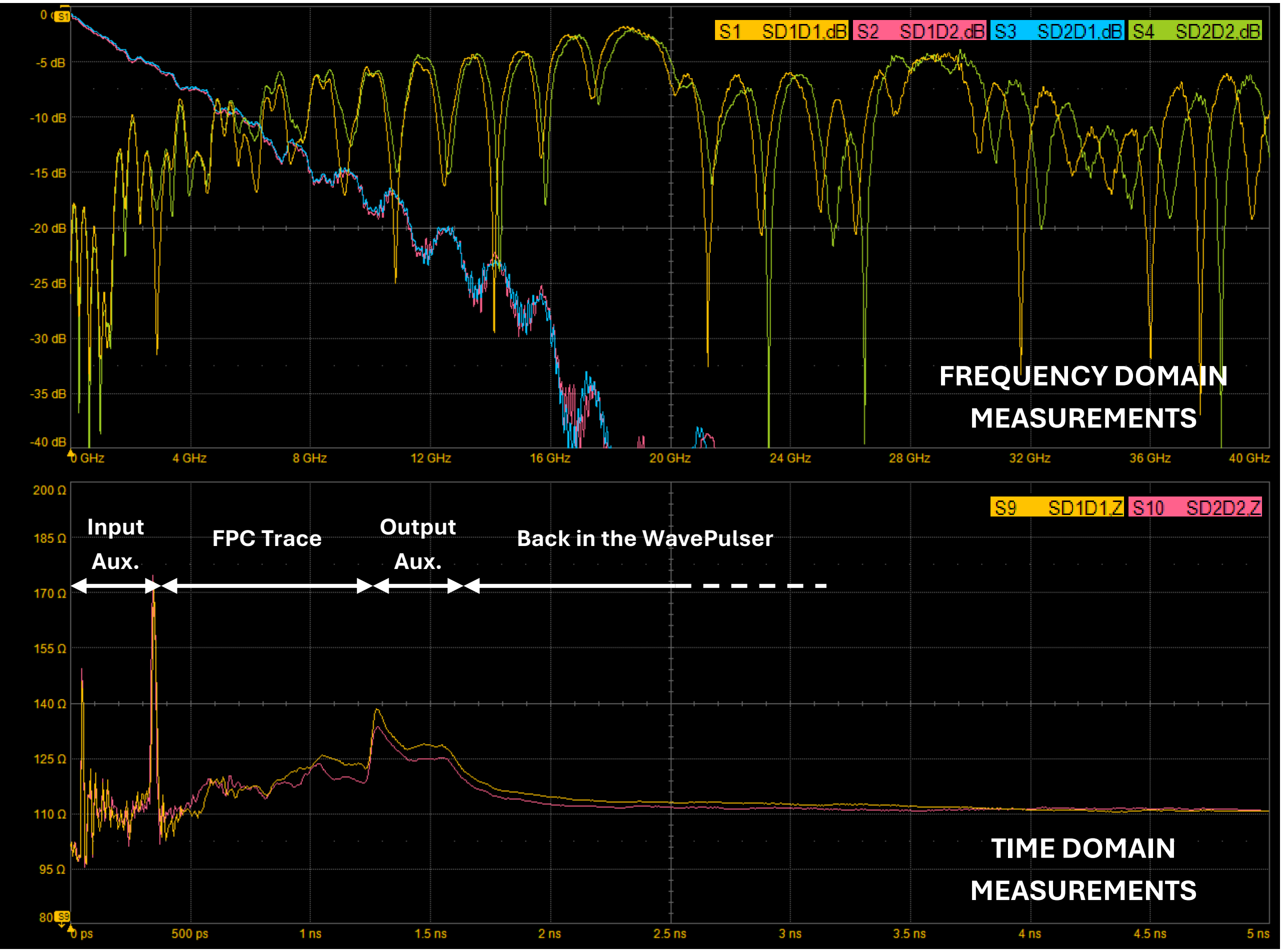
First FPC prototypes from LTU are being tested with LeCroy WavePulser 40iX





First Look Into LTU FPC Properties

Measurements with entire signal transmission chain



- **Time Domain Analysis (Diff. Impedance vs One-Way Travel Time)**

  Substantial impedance mismatches primarily due to wirebonds

  FPC differential impedance = 100 … 125 Ω

  FPC length is reasonably acceptable (≈ 15 cm for ε_r = 3)

Object	t_{start} [ps]	t_{end} [ps]	Δt [ps]
Input SMA Connector	0	70	70
Input Half-Moon PCB	70	320	250
Input Wirebonds	320	380	60
LTU FPC	380	1230	850
Output Wirebonds	1230	…	
Output Half-Moon PCB	…	…	330
Output SMA Connector	…	1560	

Auxiliary connections can be gated to access fundamental FPC properties

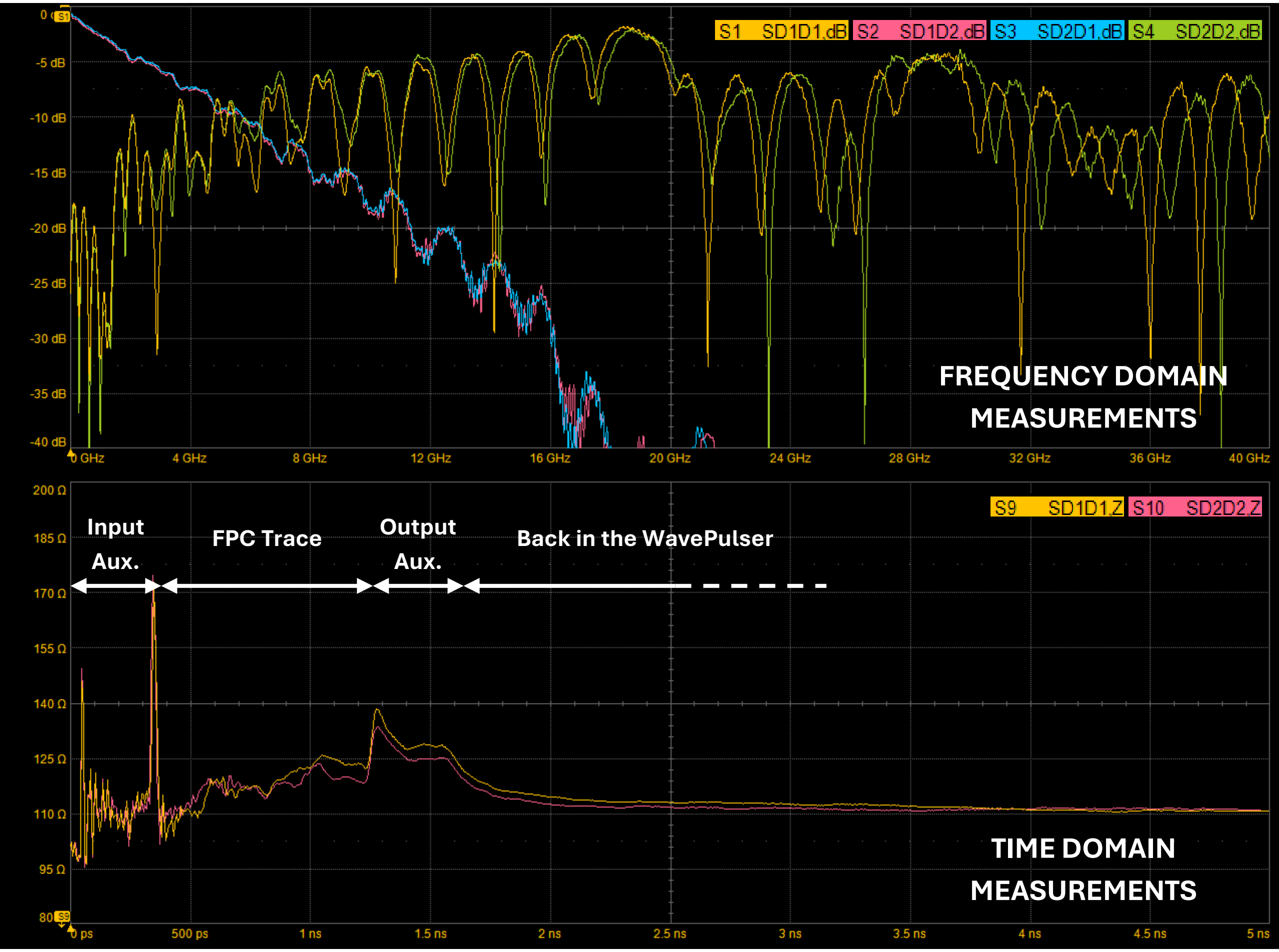
- **Frequency Domain Analysis (Signal Reflection/Transmission vs Frequency)**

  Reflection losses are dominating > 5 GHz → Interconnections

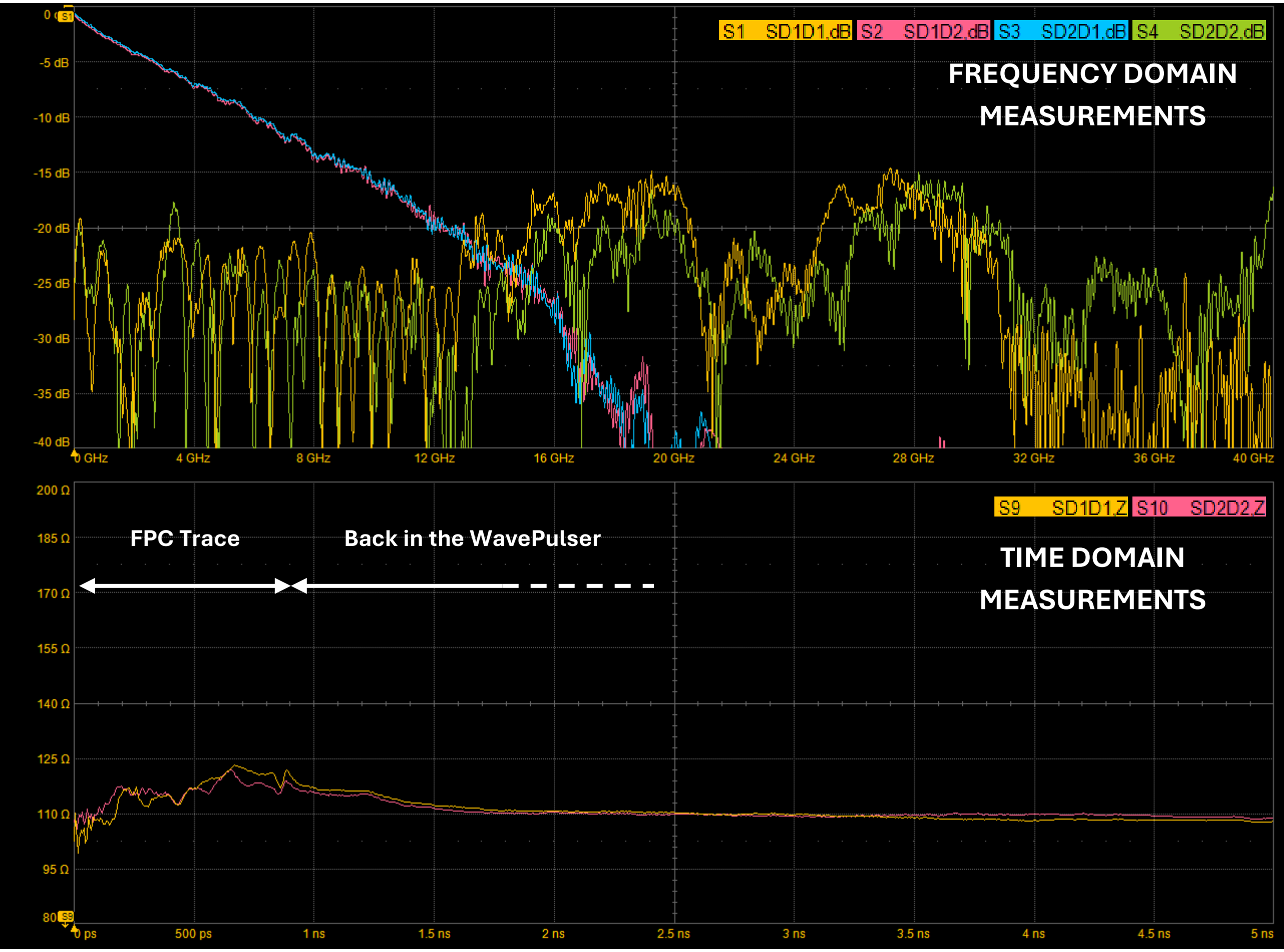
  Resonating structures are clearly visible > 10 GHz → FPC length

First Look Into LTU FPC Properties

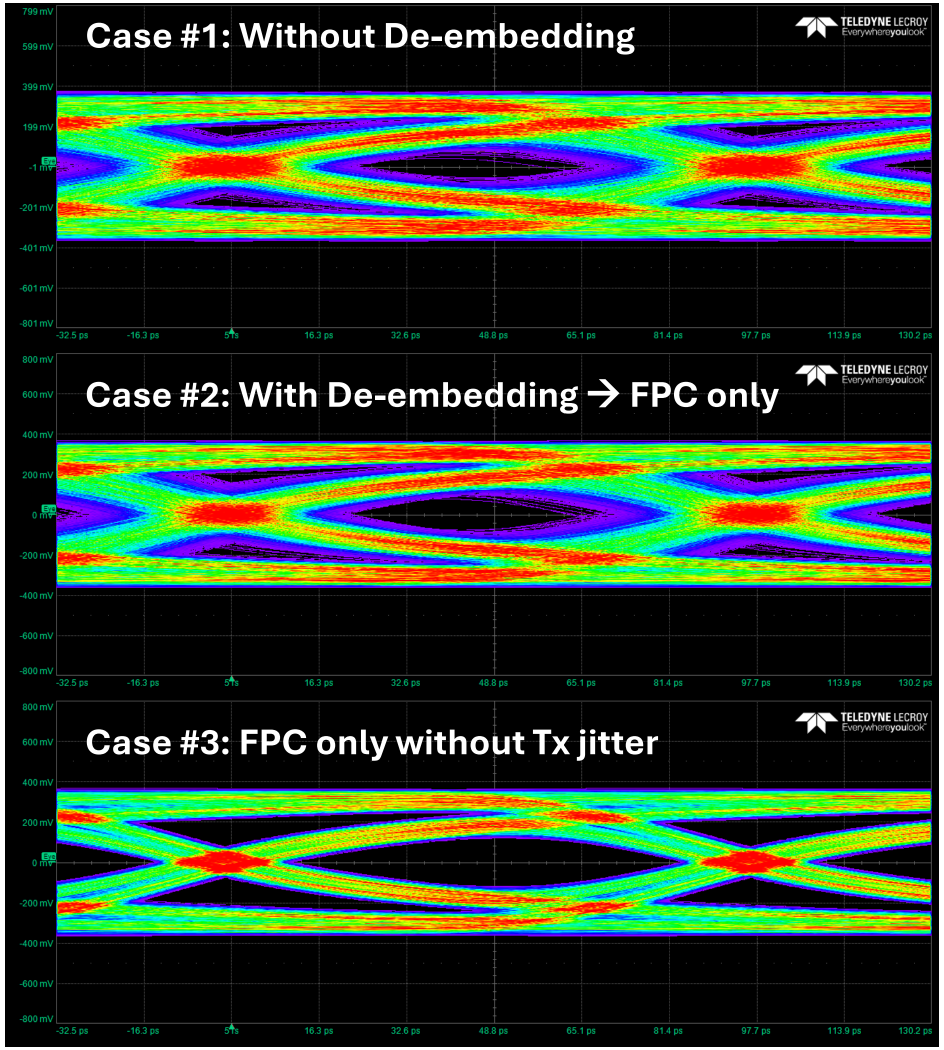
Without De-embedding / Gating (Auxiliary Connections + FPC)



With De-embedding / Gating (FPC)



First Look Into LTU FPC Properties



Eye Diagrams Simulations with WavePulser's Simulation Tool

- **(Quasi-)Realistic Transmitter Definition**

Signal Type	=	PRBS13 NRZ	Symbols per Bit	=	16 S
Data Rate	=	10.24 Gb/s	Signal Length	=	1 μs (≈ 164 kS)
Signal Amplitude	=	1 V	Tx Jitter	=	MOSAIX-like
Signal Rise Time	=	20 ps	Pre-Emphasis	=	OFF

- **BER target of 10^{-11} inaccessible despite turning off Tx jitter (case #3; unrealistic), although pre-emphasis might marginally help (to be done)**

Parameter	**Case #1**	**Case #2**	**Case #3**
Signal FPC	ON	ON	ON
Input Auxiliary Conn. (incl. wirebonds)	ON	OFF	OFF
Output Auxiliary Conn. (incl. wirebonds)	ON	OFF	OFF
Transmitter Jitter	ON	ON	OFF
Transmitter Pre-Emphasis	OFF	OFF	OFF
Bit Error Rate @ 5% Central Slice Width	**0.53E-3**	**0.16E-3**	**0.11E-3**

SUMMARY AND OUTLOOK

Introduction and Broad Boundary Conditions

Part – I: Calculations and Simulations

- Workflow and Caveats
- Max. Data Rate and Min. FPC Material
- Mitigation Strategies

Part – II: Experimental Characterisation

- Benchmark Studies with ITS3 Copper FPCs
- Test Setup with IB Aluminium FPCs
- First Results with LTU FPCs

Next Steps and Opportunities

- Understand First Prototypes (Cal., Sim., Exp.)
- Design and Order Next Prototypes (Q4-2026) for the System-Level Qualification Model

THANK YOU

EXTRA SLIDES