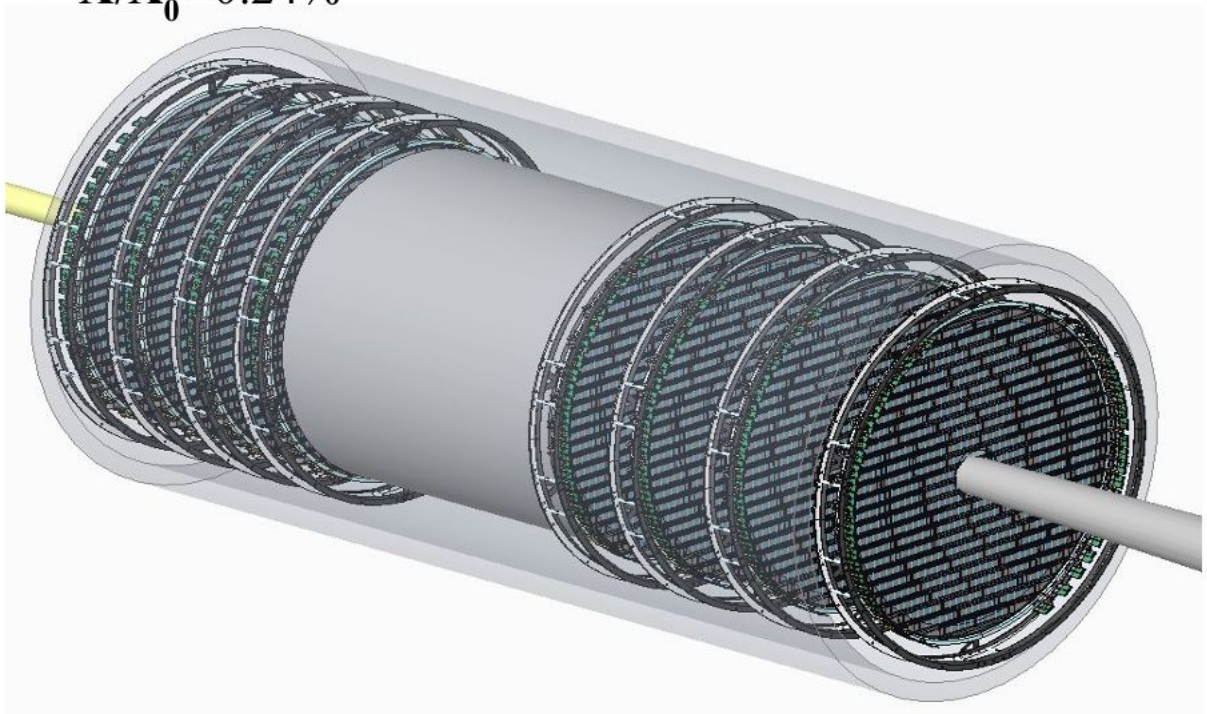
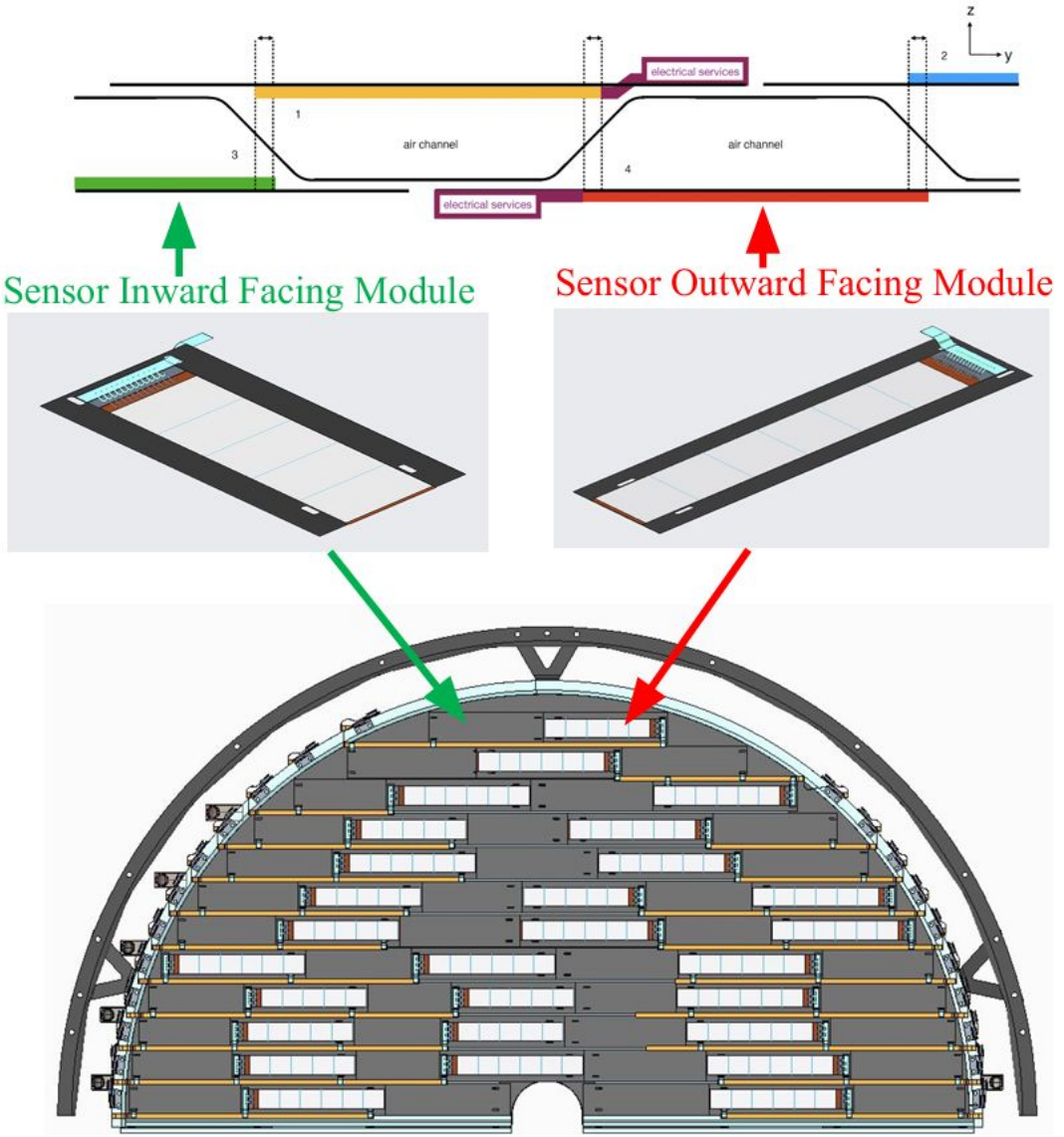
ePIC SVT Disks

- **EIC Large-Area Sensor** with design based on ITS3 MOSAIX, mounted on low-mass CF support structure with integrated air cooling
- **AncASIC** provide negative sensor bias voltage, serial power and slow control
- **Outer radius** ranging from 24 to 40 cm
- **X/X_0** ~0.24%





Summary and Outlook from 06/11/2026

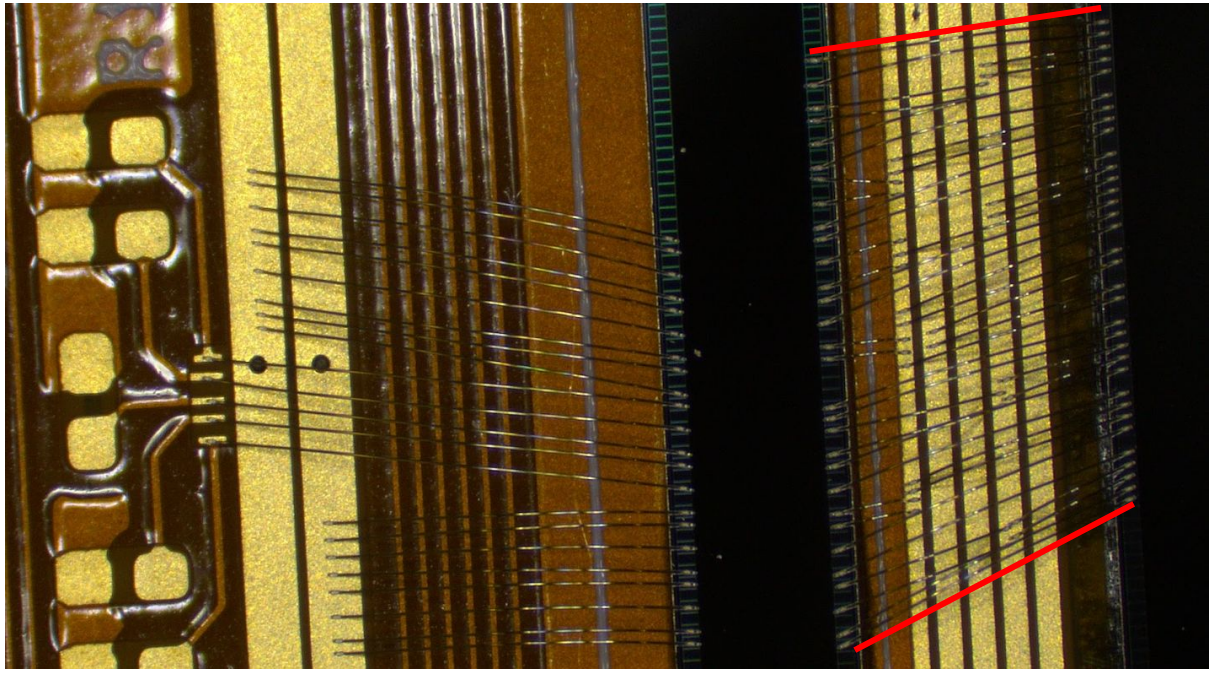
- **The first version of Cu-based FPCs from JLC (including BFPCs for outward facing modules and MFPC) arrived:**
  - **The main purpose was to facilitate disk module assembly**
  - **The following tests have been completed:**
    - Visual Inspection;
    - Soldering SMD components onto BFPC;
    - Cutting BFPCs;
    - Soldering BFPCs onto MFPC;
  - **The stiffener is not necessary, will be removed in the next design**
  - **Need to improve soldering of left BFPC to MFPC**

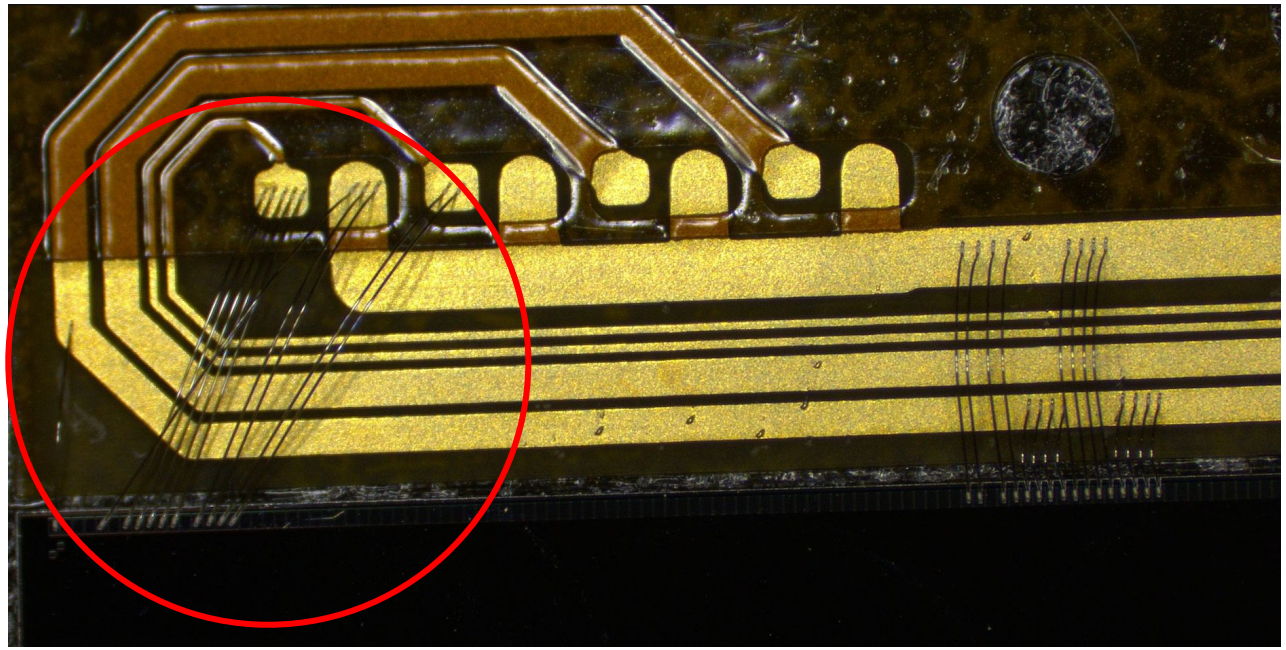
- **Outlook**
  - Mount and wire-bond between dummy EIC-LASs, AncASICs and BFPCs;
  - Design BFPCs for inward facing modules.

Previous meeting link: ePIC SVT WP3 Electrical Interfaces Meeting (June 11, 2026) · Indico

Mount dummy chips and BFPC

wire-bond between BFPC and dummy chip

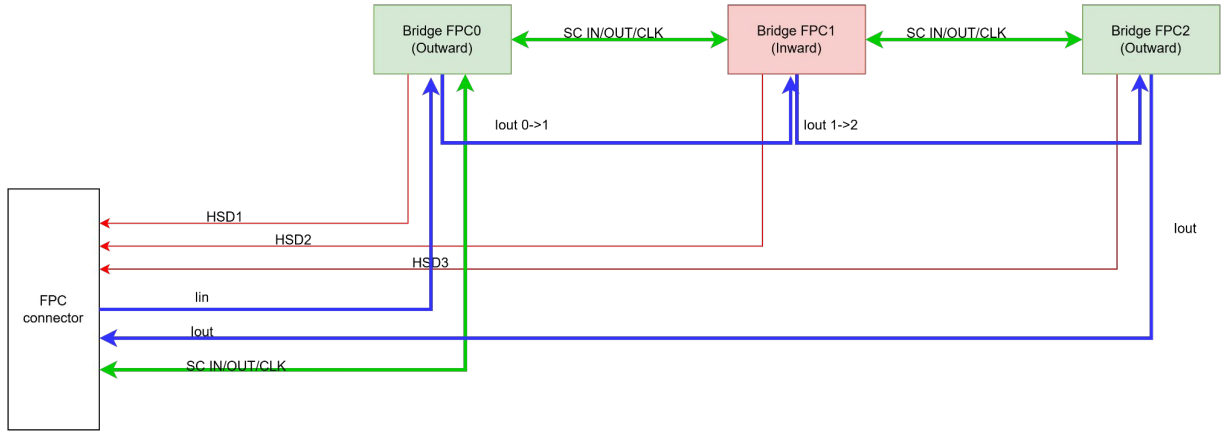


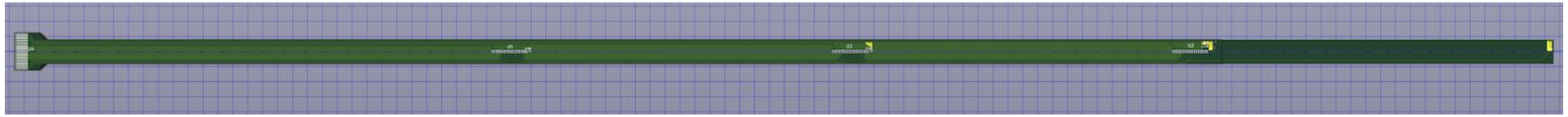


Wire bonding on selected regions has been completed, with no major issues overall. The wire bonding tech provided the following recommendations:

- **Left side**: The position of the AncASIC and its bonding pads should be positioned to facilitate straight wire-bonds, especially for those directly connecting between the AncASIC and LAS.
- **Right side**: the power bus lines aren't long enough, which makes wire bonding of the top pads of the LAS to BFPC somewhat difficult.

New MFPC Overview

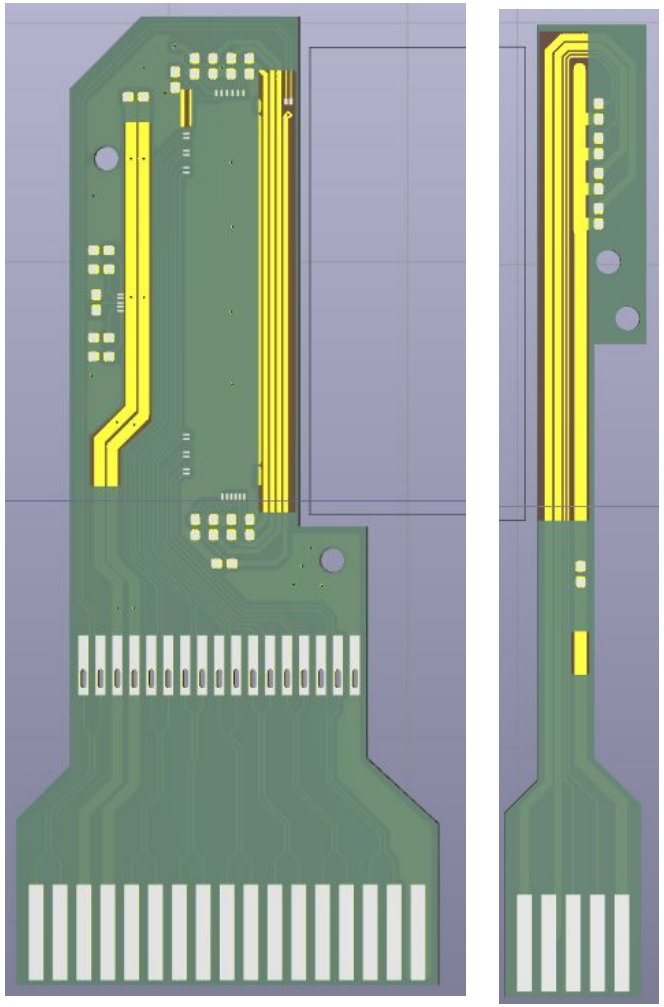




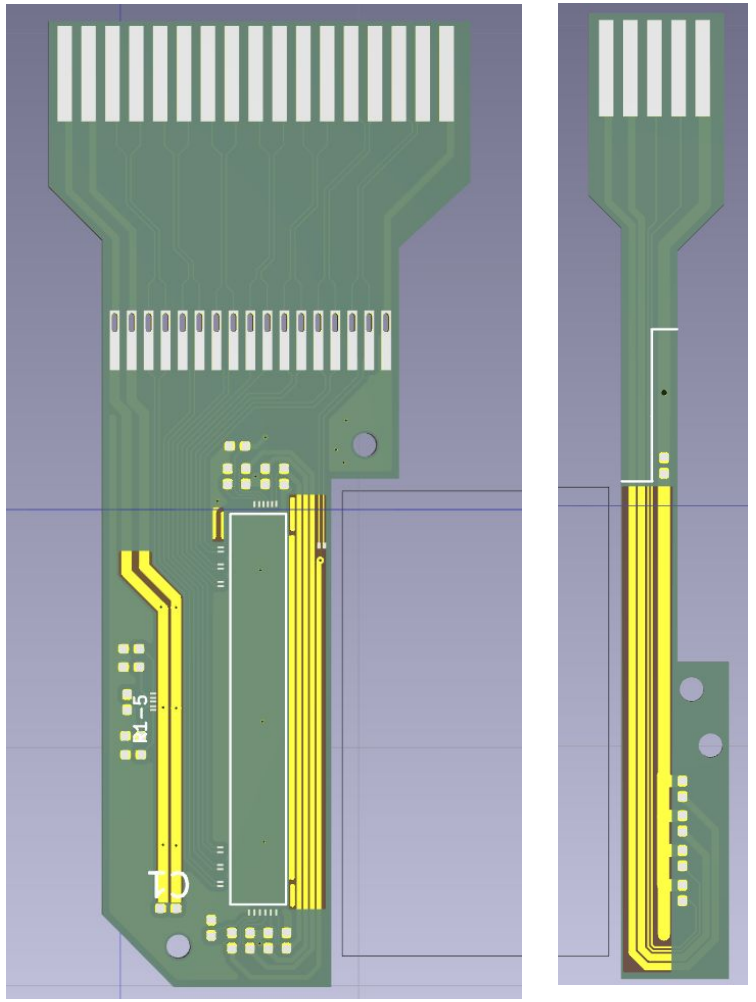
	Area (mm^2)	Trace Area (mm^2)	Power net area (mm^2)	Fill factor
Top Layer	4747.6	221.5	1875.6	0.45
Bottom Layer	4747.6	0 → 3	3202.2 → 3177.5	0.68 → 0.67

Compared to the previous version, the new MFPC has no major changes. Only the connection to BFPC1 was partially modified to accommodate the inward facing module. See page 9 for more details.

New BFPC Overview



Top view of outward facing module BFPCs



Bottom view of inward facing module BFPCs

Main modifications:

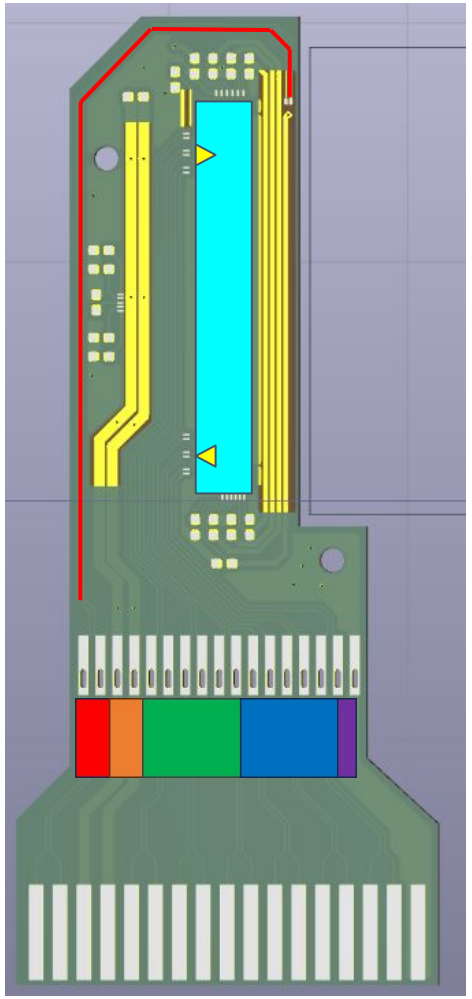
BFPC on left side:

1. Design the Inward version.
2. connected the decoupling capacitors to the power buses.
3. Optimizing the soldering pads to solder on MFPC

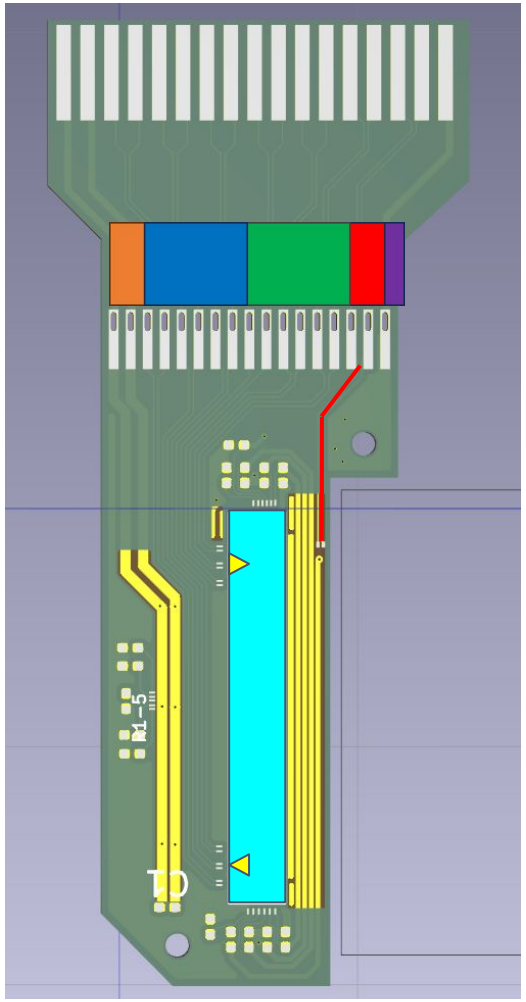
BFPC on right side:

1. Design the Inward version.
2. Increased the length of power buses for better wire bonding.

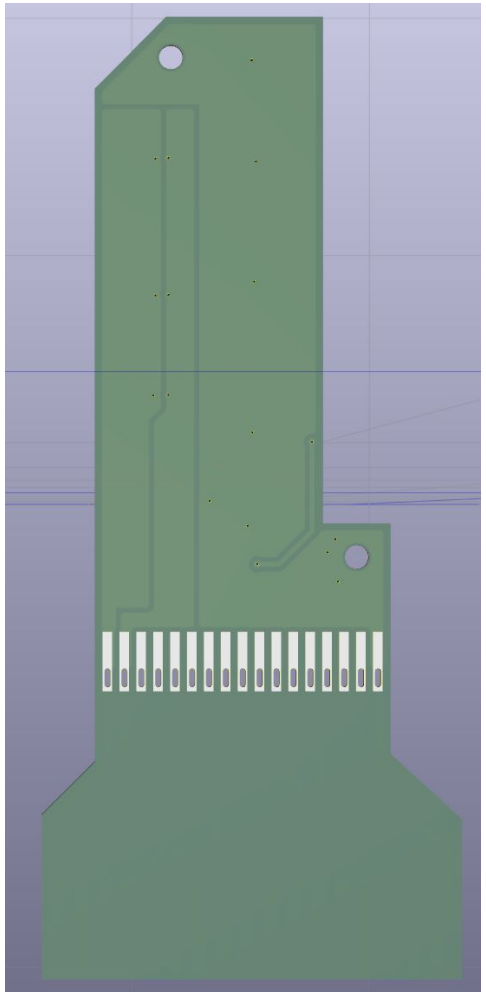
Outward vs Inward facing module BFPC



Top view of outward facing module BFPCs



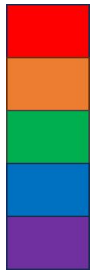
Bottom view of inward facing module BFPCs



Top view of inward facing module BFPCs

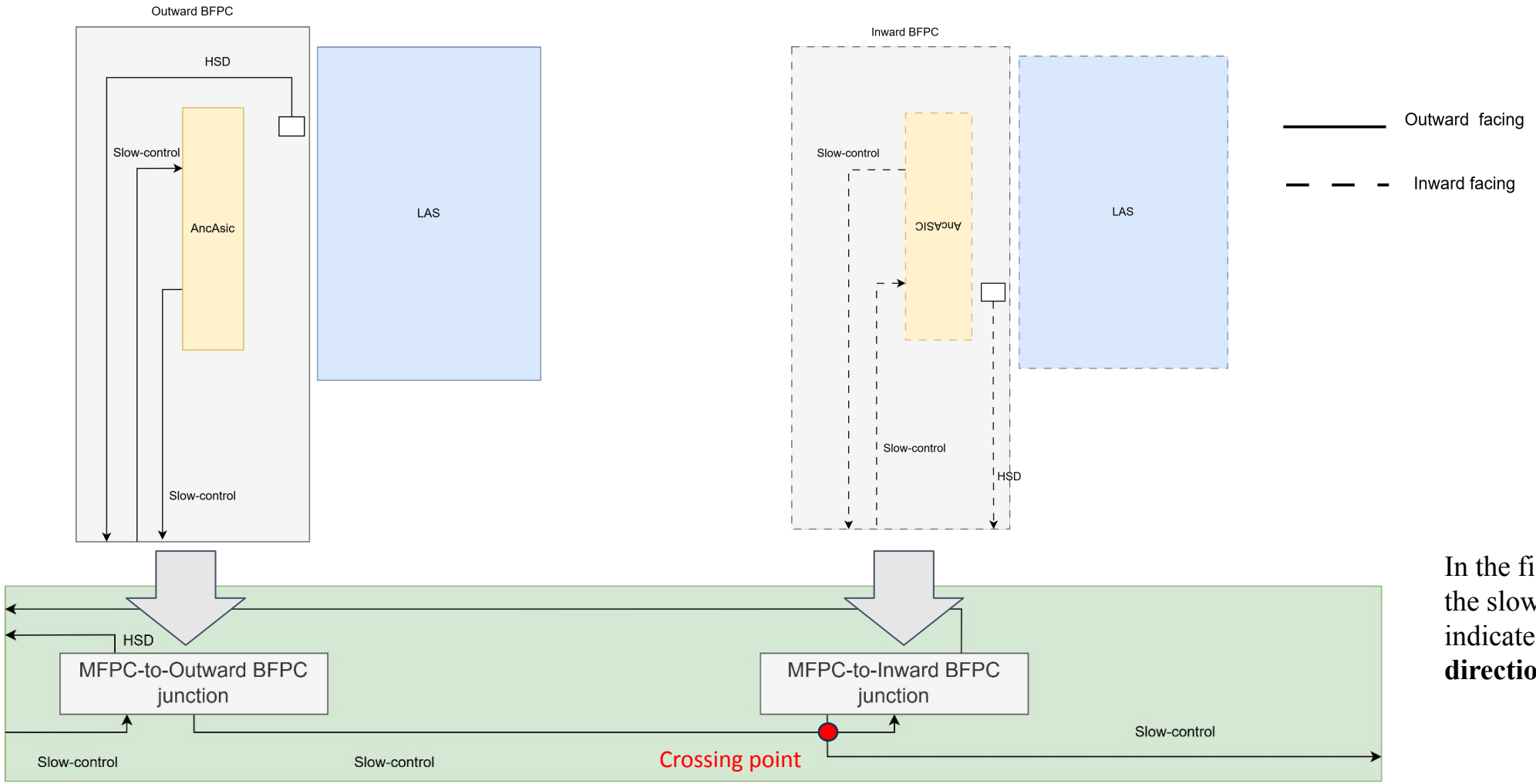
To convert the outward-facing module BFPC into an inward-facing module BFPC:

1. the pin assignment at the interface between the BFPC and the MFPC was adjusted.
2. the connection scheme for the HSD and slow-control signals was modified.
3. In addition, after moving the entire main circuit to the bottom layer, the structures used for connecting to the MFPC were retained on the front side.



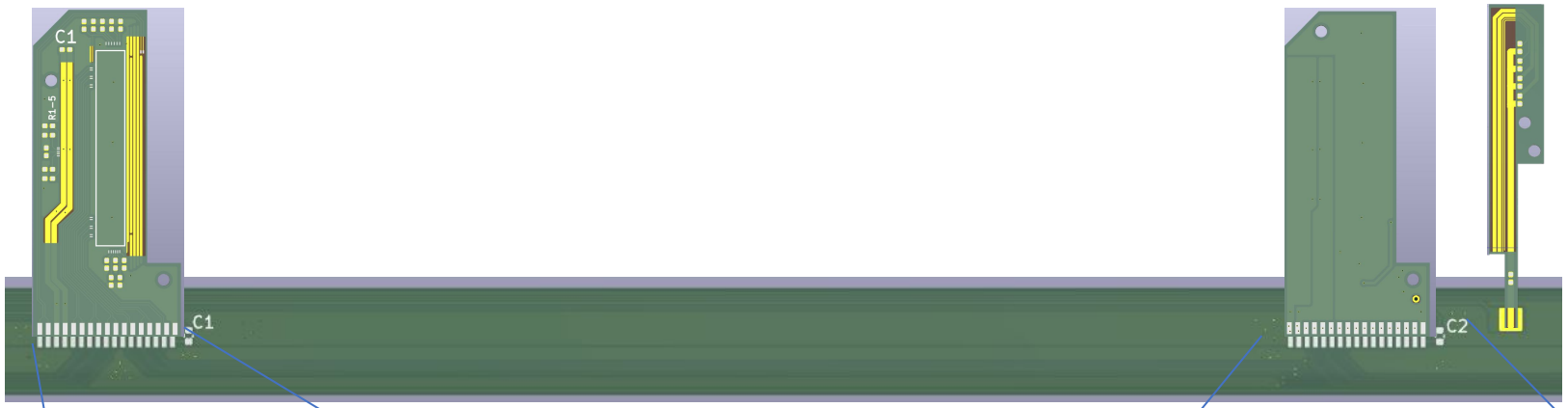
HSD
Iin/Iout
Slow-control from previous board
Slow-control to next board
Gnd

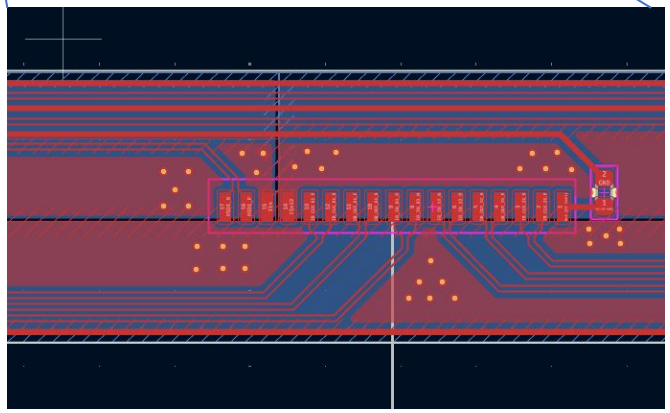
HSD and slow-control connections



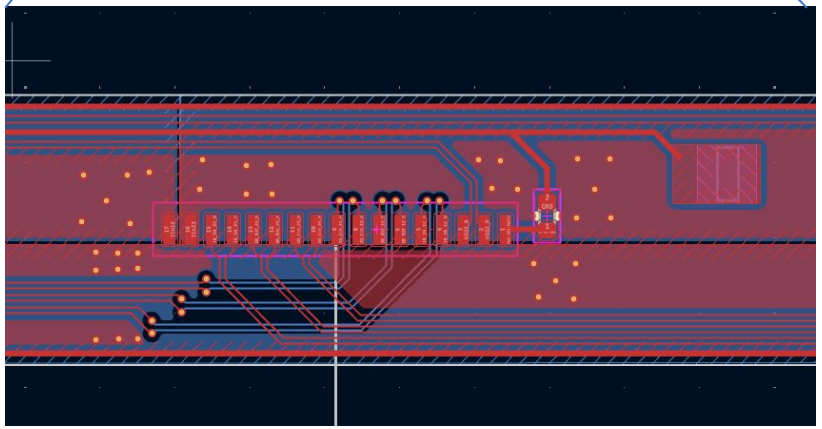
In the figure, the direction of the slow-control arrows indicates the **downlink direction.**

Inward/Outward FPC assembly





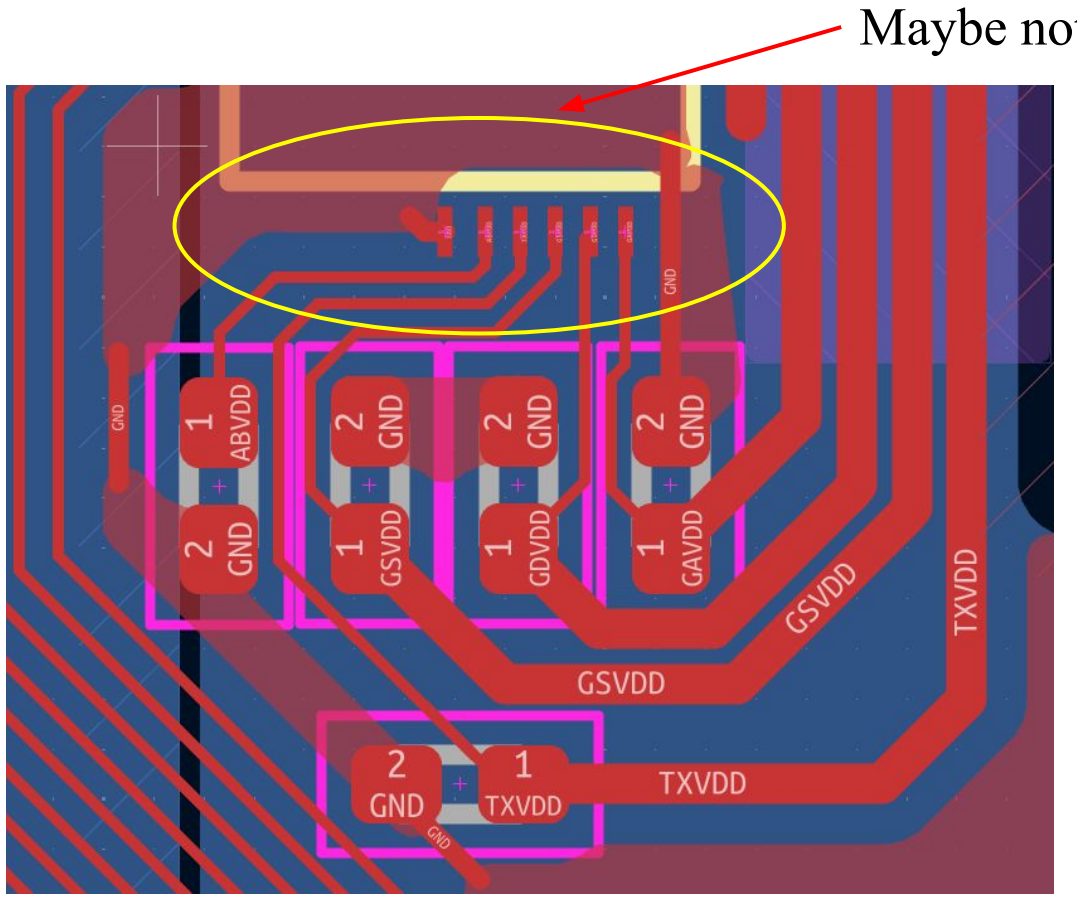
Outward facing module BFPC



Inward facing module BFPC

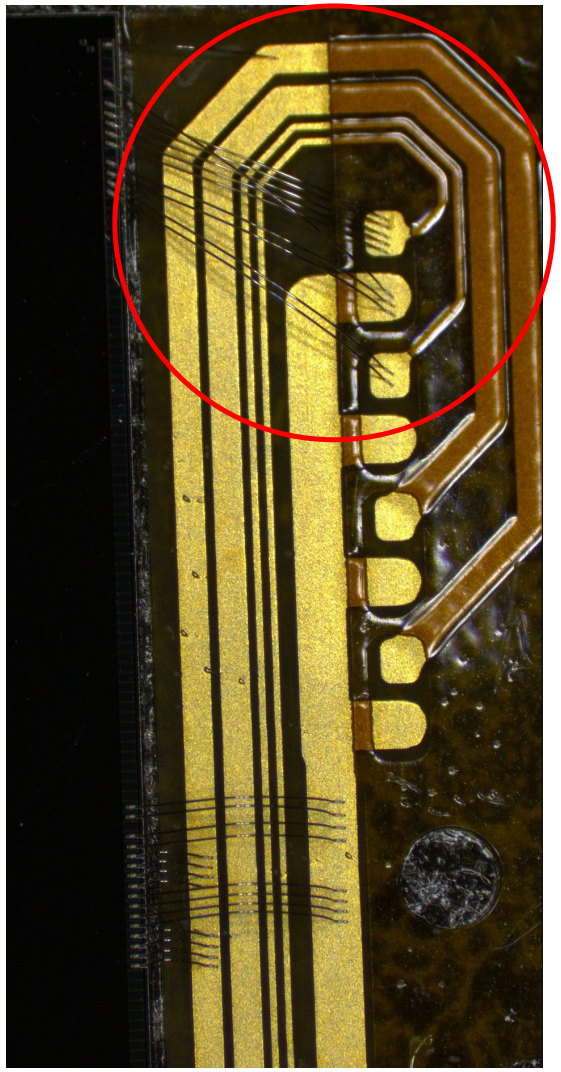
The layout of the solder pads on the Main FPC for the **second** Bridge FPC has been adjusted. To resolve the trace crossing issue, part of the Iout net width on the MFPC was sacrificed.
As a result, the power consumption of Iin/Iout on the Main FPC is expected to increase slightly compared to the first version (473 mW → 479 mW).

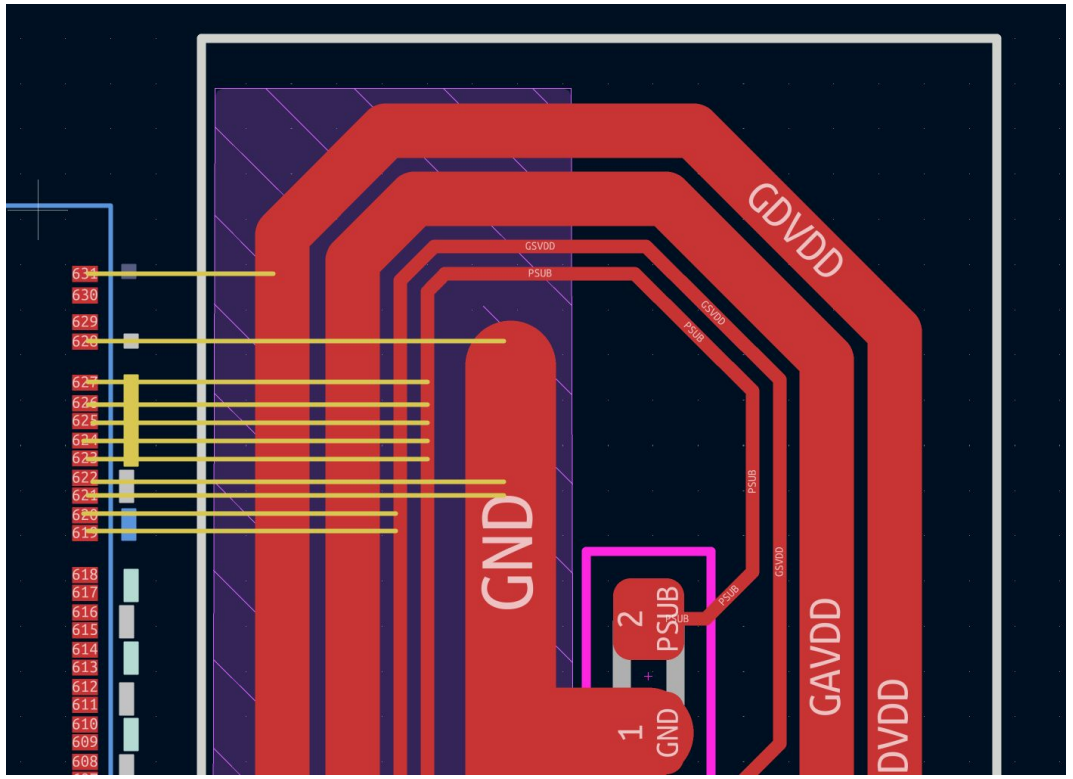
Decoupling capacitors on the left BFPC



Following the suggestion from AncASIC designer, the power buses on the left BFPC are connected to the decoupling capacitor now.
We are still discussing whether the pads on the top/bottom edge of the AncASIC can be left floating. If so, the capacitors can be placed closer to the chip.

Extended the power buses on the right BFPC

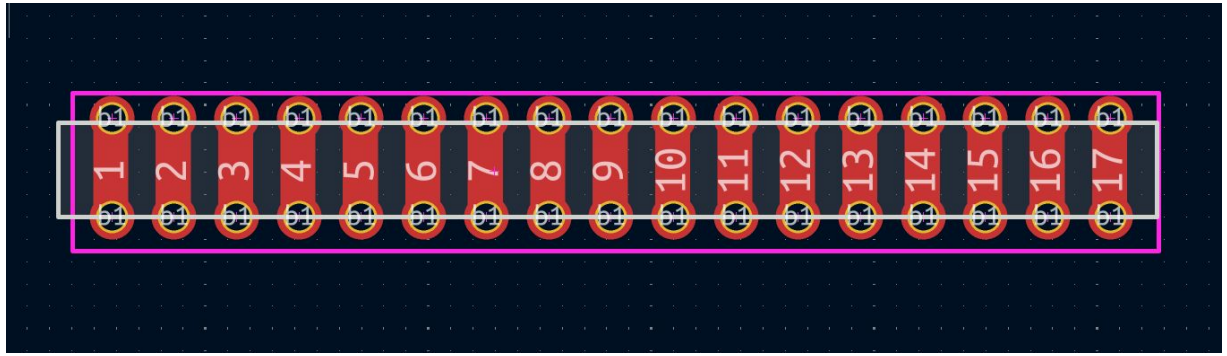


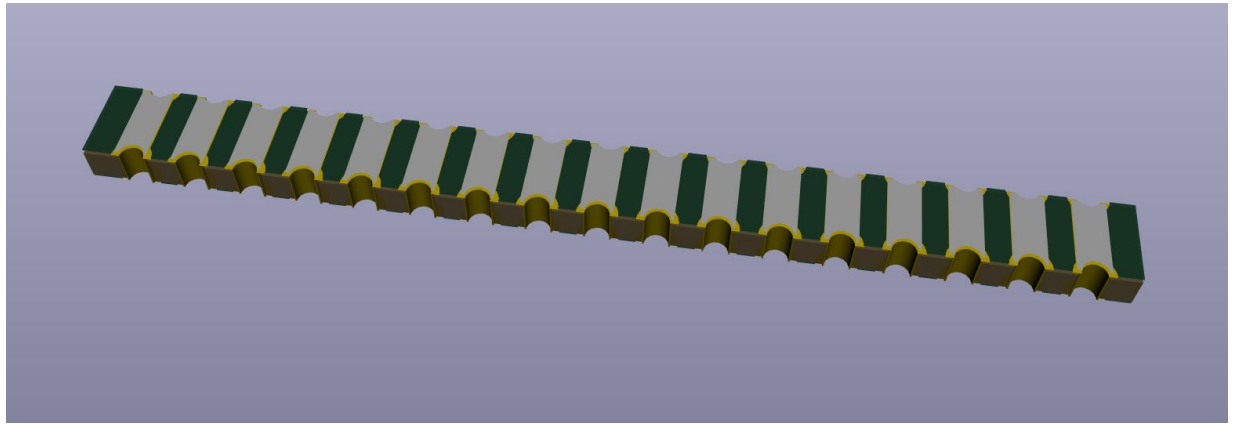


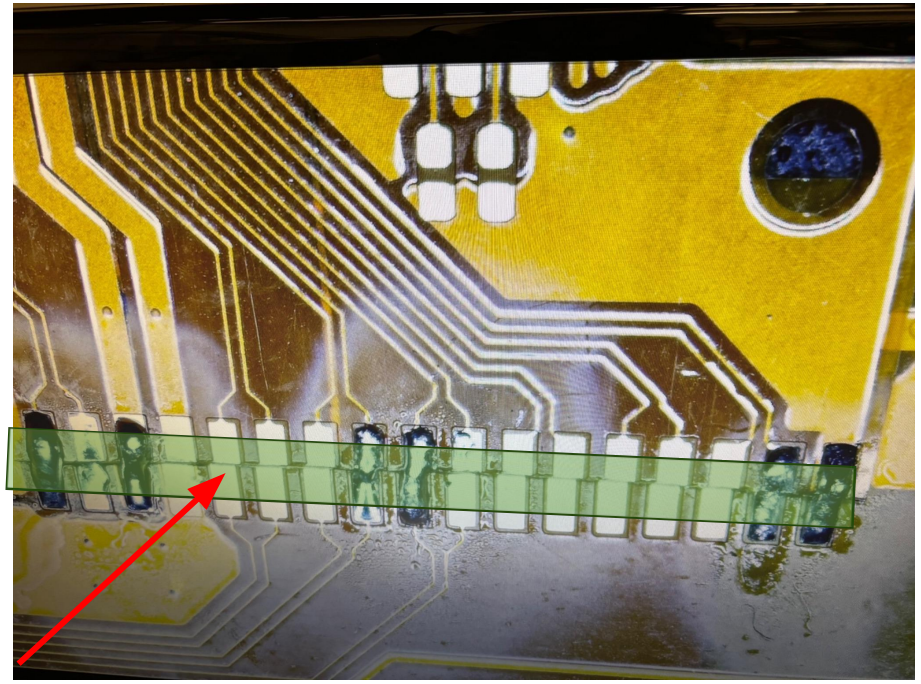
Wire bonding diagram for the new right BFPC

To allow the pads on the right side of the LAS to be straight-bonded to the power buses, the length of the right-side BFPC was extended by approximately 0.96 mm.

BFPC-to-MFPC Interconnection: Bridge PCB



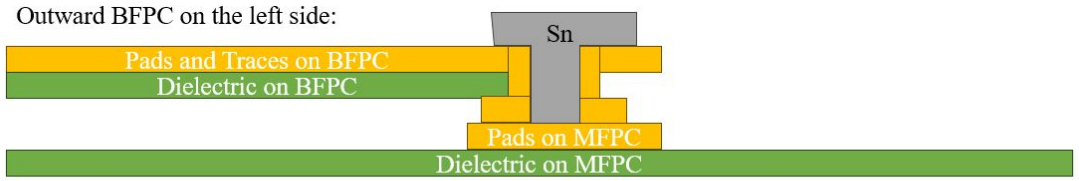


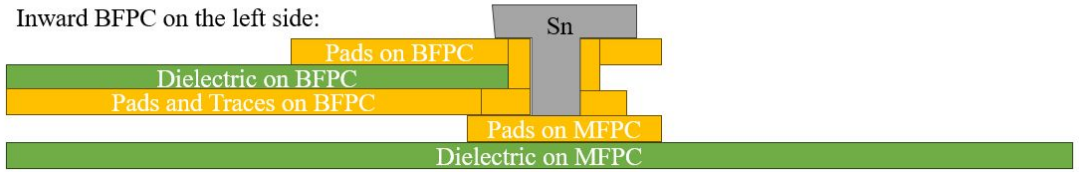


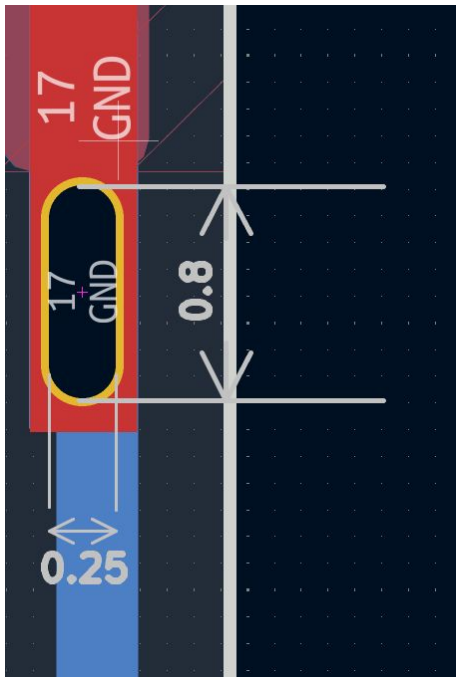
Bridge PCB

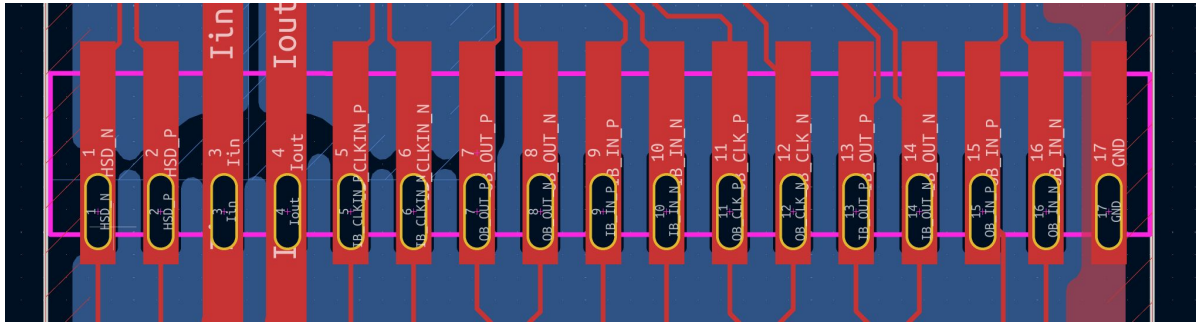
A Bridge PCB with **castellated holes** could be helpful.

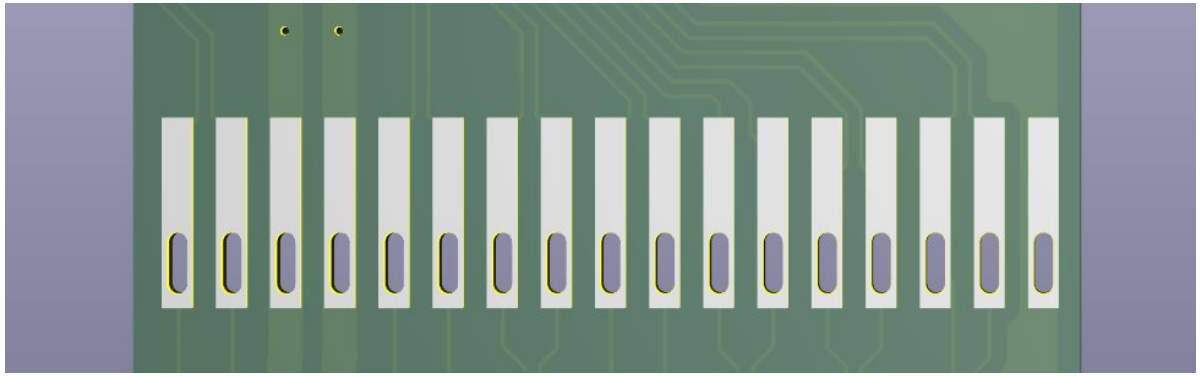
BFPC-to-MFPC Interconnection: Through-hole











Another method to assemble the BFPC to the Main FPC is through oblong-shaped through-holes, as shown in the figure. The through-hole has a length of 0.8 mm and a width of 0.25 mm, and the soldering pads on the BFPC have been extended to a length of 2.5 mm.

Summary & Next steps

Summary

1. Wire-bonding tests between the FPC and the dummy chip are complete.

- Both chip-to-power-bus bonding and chip-to-chip wire bonding were verified as feasible.
- To make the wire bonding easier, recommendation: adjust the chip positions and pad assignments to have straight wire bonds, and extend the right BFPC.

2. The new version of the FPC design is largely complete.

- Designed the BFPCs for inward-facing modules.
- Connected the decoupling capacitors to the power buses.
- Extended the power buses on the right BFPC.

3. Two approaches will be explored to improve BFPC-to-MFPC soldering.

- To address the difficulty of soldering the BFPC onto the MFPC, the new version will try both a bridge PCB and a through-hole approach.

Next Steps

1. Design testing boards for the new FPCs to test signal transmission quality, power consumption, and measure characteristic impedance.
2. Build the FPC simulation model in Ansys.