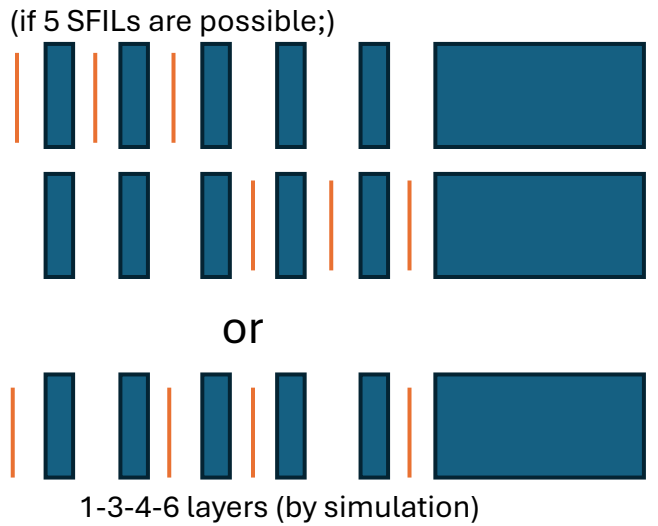
AstroPix readiness : (1) Possible Set-up

- Additional AstroPix 9chip prototype modules or quad-chips needed
  - Only available at ANL: Two 9chip prototype modules & Two quad-chips (chip0 malfunction; chip2 low hit eff.) + two A-STEP boards at least
    - One quad-chip will be changed into new quad-chip.
  - Only available at Korea: One 9chip prototype module + two A-STEP boards

→Two additional 9chip prototype modules are promising? (by Manoj)

→Need to discuss with Manoj and Maria tomorrow: how many additional astropix 9-chip/quad-chip can be produced.

- Previous AstroPix Setup
  - Hall D (Mar-Jun, 2026): Two-layer of quad-chips + A-STEP board
  - KEK (May, 2026): One 9-chip prototype module + A-STEP board (Stable operation at ~2.7 kHz beam rate)
- AstroPix Setup for the upcoming beam test
  - If **three-layer** of 9-chip/quad-chips + A-STEP is enough for the upcoming beam test;
    - 40 MHz external clock; 1 channel of waveform generator
  - If **four-layer** of 9-chip/quad-chips + two A-STEP;
    - 40 MHz external clock; two channels of waveform generator
    - Add one more astropix to RCDAQ
    - Need to check synchronization between two A-STEP using external clock before beam test



AstroPix readiness : (2) Test

- Data rate measurement study (On-going)
  - Updated sw/fw (same as Hall D): Readout FIFO depth increased from 4096 to 16384 bytes
  - Achieved up to **~2.2 kHz per chip** and **< 5 Hz per pixel** at 7 mm collimator (vs **~1.6 kHz per chip** and **3.6 Hz per pixel** at 7 mm collimator)

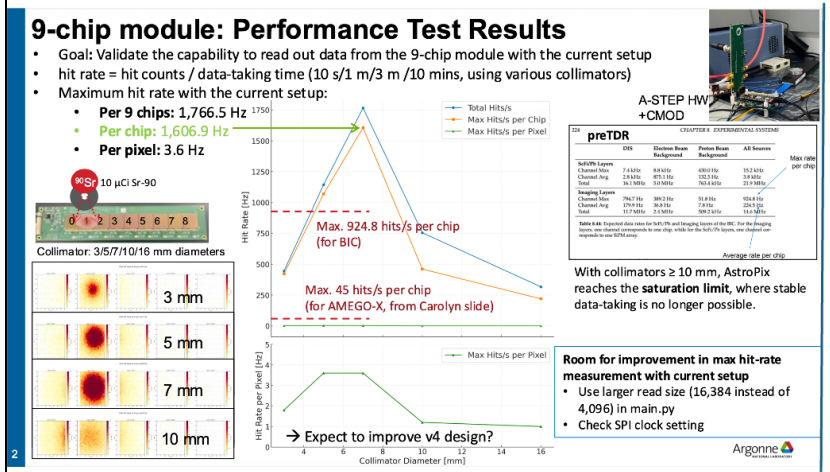
  → [on-going] checking faster SPI readout clock

  →Checking the data rate with two layers

Data rate measurement (prev. vs curr.): Hit rate per chip

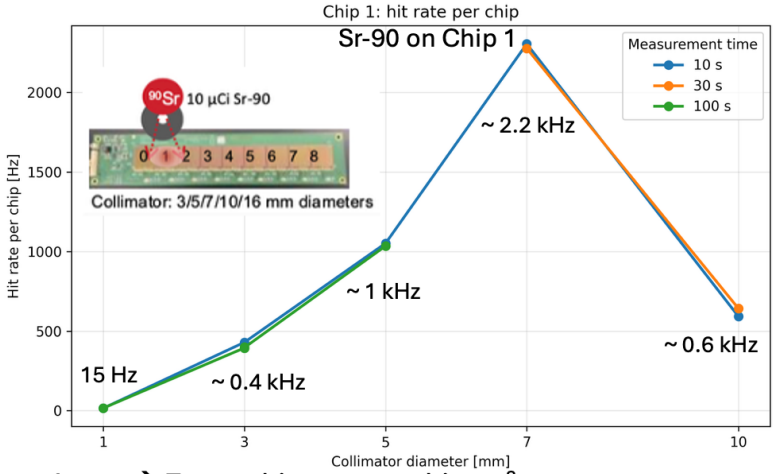
9-chip module: Performance Test Results

- Goal: Validate the capability to read out data from the 9-chip module with the current setup
- hit rate = hit counts / data-taking time (10 s/1 m/3 m /10 mins, using various collimators)
- Maximum hit rate with the current setup:
  - **Per 9 chips:** 1,766.5 Hz
  - **Per chip:** 1,606.9 Hz
  - **Per pixel:** 3.6 Hz



- 3 mm → 5 mm : hit rate per chip ~ r^2

Readout buffer size reported by readoutGetBufferSize() in main.py
7 mm ~ 4000



- 1 mm → 7 mm : hit rate per chip ~ r^2

Readout buffer size reported by readoutGetBufferSize() in main.py
1 mm: ~ 0 - 44
3 mm: ~ 300 - 400
5 mm: ~ 1000 - 1400
7 mm: ~ 6000 - 10000

- **Possible Reasons for Faster Data Readout (need to double-check, again)**
  - **Software (main.py)**
    - SPI divider reduced from 20 to 10 → faster SPI readout clock
  - **Firmware updates**
    - Packet mode enabled by default → readout FIFO filled only with complete frames
    - Improved readout size reporting → reduced empty-byte readout
    - Readout FIFO depth increased from 4096 to 16384 bytes → larger buffering margin

7/6/26 Bobae Kim 4

- Any signal from AstroPix to H2GCROC
  - During the single-chip + GECCO setup in Korea, the **MISO signal** was sent to the combined DAQ system.
  - Similarly, we plan to send the any **1.8 V hit signal generated in the first imaging layer** to the H2GCROC.

  →Check **interrupt signal** from A-STEP board
  - The signal can be embedded in the **unused 8-byte data packet** for event synchronization.

Data rate measurement (prev. vs curr.): Hit rate per chip

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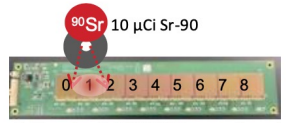
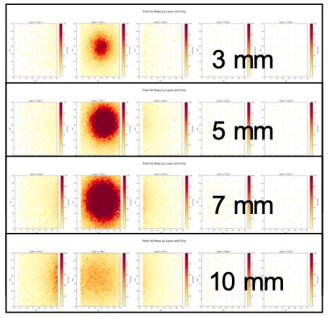
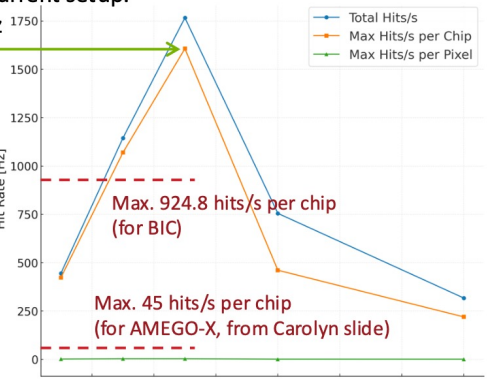
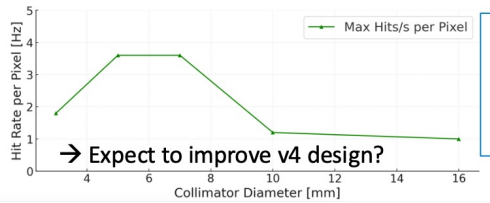


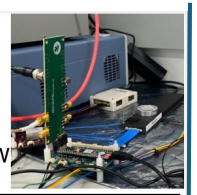
Collimator: 3/5/7/10/16 mm diameters

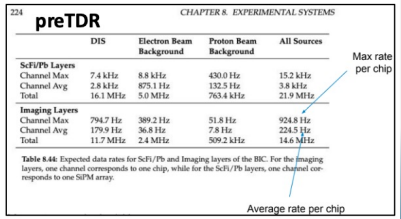






A-STEP HW +CMOD





With collimators ≥ 10 mm, AstroPix reaches the **saturation limit**, where stable data-taking is no longer possible.

Room for improvement in max hit-rate measurement with current setup
- Use larger read size (16,384 instead of 4,096) in main.py
- Check SPI clock setting

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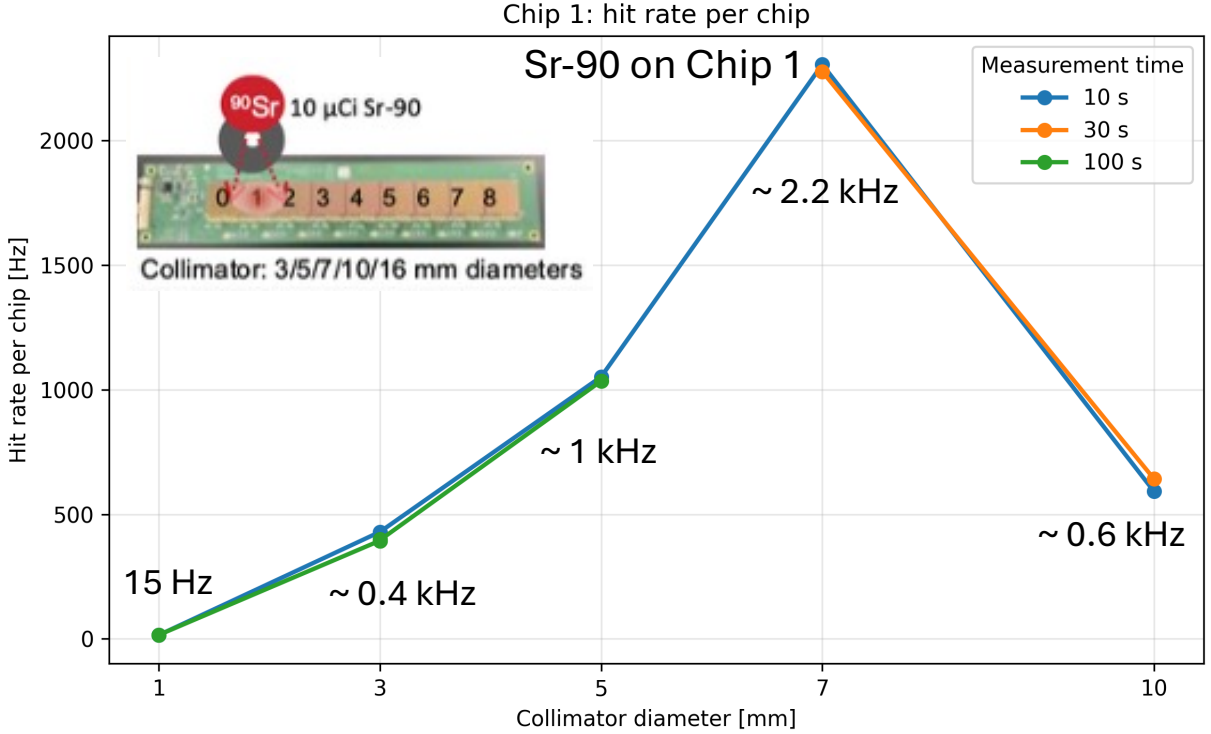
- 3 mm → 5 mm : hit rate per chip ~ r^2

Readout buffer size reported by readoutGetBufferSize() in main.py
7 mm ~ 4000



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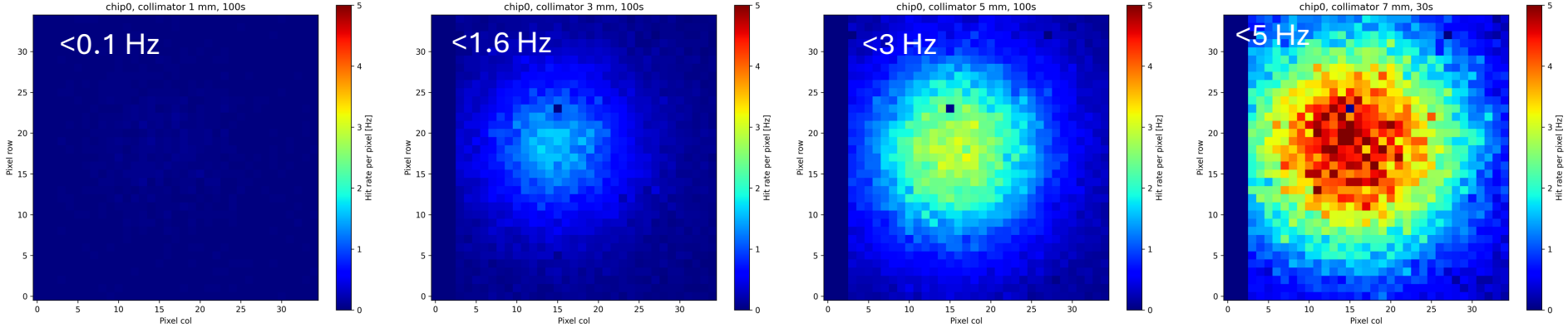
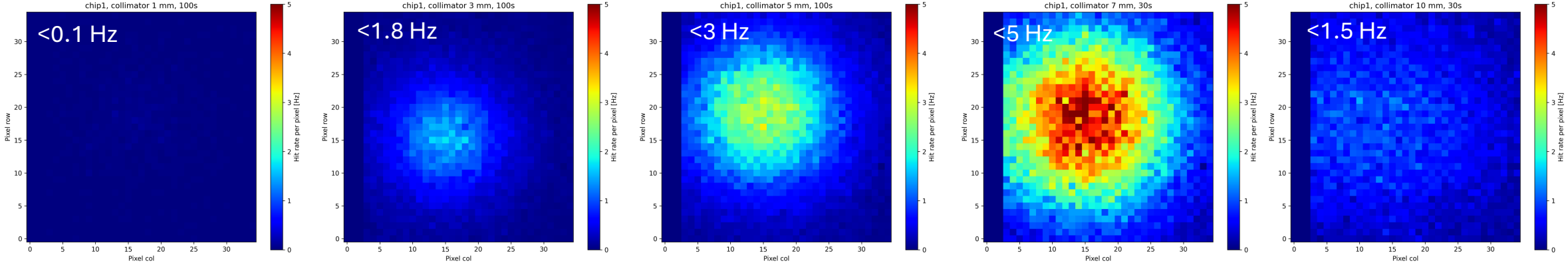
Current Data rate measurement result (2): **Hit rate per pixel**

- Measure for 10 s, 30 s, 100 s using different collimator diameter (**1/3/5/7**/10/15 mm) → hit rate = #.hits/times
- Max. hit rate per chip and per pixel
- Used sw/fw = A-STEP (ext-clock_260225 based on Richard's branch, uploaded Feb. 5, 2026. (a90645d))
  - AstroPix3 Timestamp clk = 10 MHz, AstroPix3 sample clk = 100 MHz

chip0



chip1

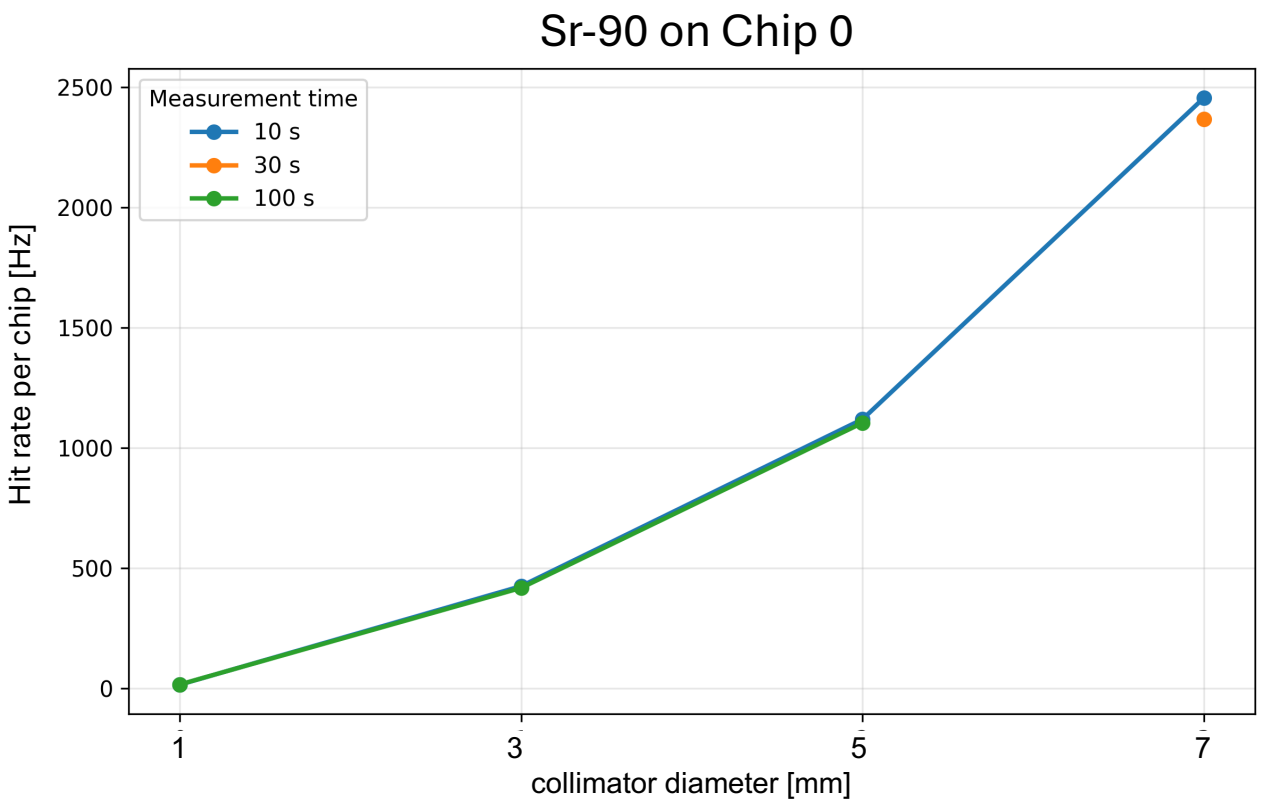


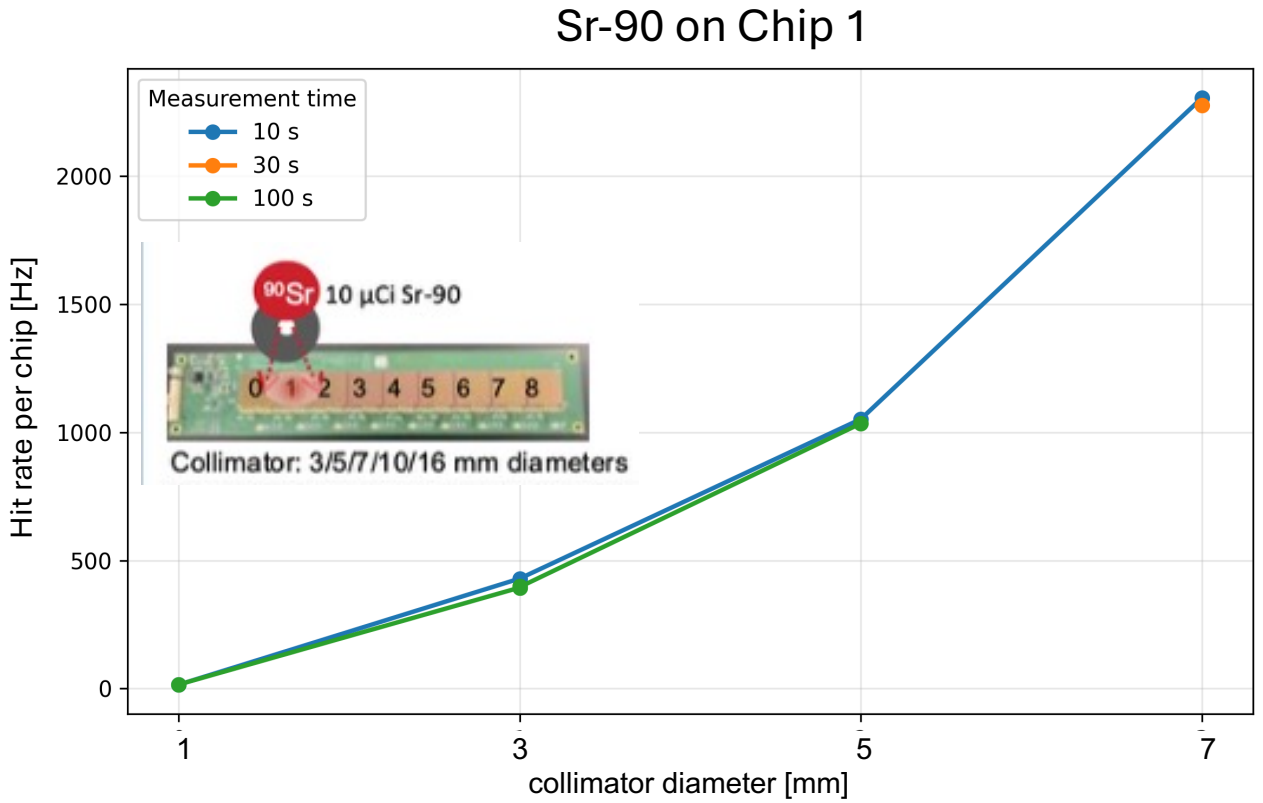
→ Previous results: **3.6 Hz/pixel** for both **5 mm** and **7 mm** collimators.
→ Increasing the **readout FIFO depth** improved the hit rate to **5 Hz/pixel** (7 mm collimator), indicating the previous limitation was due to buffering rather than the AstroPix v3 chip design.

Current Data rate measurement result

clk_ext
↓
PLL/MMCM
↓
80 MHz
100 MHz
10 MHz
20 MHz
2.5 MHz

- Measure for 10 s, 30 s, 100 s using different collimator diameter (**1/3/5/7**/10/15 mm) → hit rate = #.hits/times
- Max. hit rate per chip and per pixel
- Used sw/fw = A-STEP (ext-clock_260225 based on Richard's branch, uploaded Feb. 5, 2026. (a90645d))
  - AstroPix3 Timestamp clk = 10 MHz, AstroPix3 sample clk = 100 MHz





Used sw/fw

1. Hall D beam test using two-layer of quad-chips + ASTEP
    - A-STEP (ext-clock_260225 based on Richard's branch, uploaded Feb. 5, 2026. (a90645d))
        - AstroPix3 Timestamp clk = 10 MHz
        - AstroPix3 sample clk = 100 MHz
2. KEK beam test using 9-chip PCB prototype module + ASTEP (May.2026)
    - A-STEP (ext-clock based on main branch uploaded Aug. 6, 2025. (ac972e0))
        - AstroPix3 Timestamp clk = 5 MHz
        - AstroPix3 sample clk = 100 MHz
3. KEK beam test using three-layer of quad-chips + ASTEP (Dec.2025)
    - A-STEP (quad-9chip-datareview based on main branch uploaded Jun. 6, 2025. (b9d9722))
        - AstroPix3 Timestamp clk = 5 MHz
        - AstroPix3 sample clk = 100 MHz
4. KEK beam test using v4 chip (Dec.2025) and three-layer of single chips + GECCO (by Korea team)
    - astropix-python-v3
        - AstroPix3 Timestamp clk = 2.5 MHz
        - AstroPix3 sample clk = 200 MHz
        - AstroPix4 Timestamp clk = 2.5 MHz
        - AstroPix4 sample clk = 20 MHz