Inner MPGD CyMBaL Status

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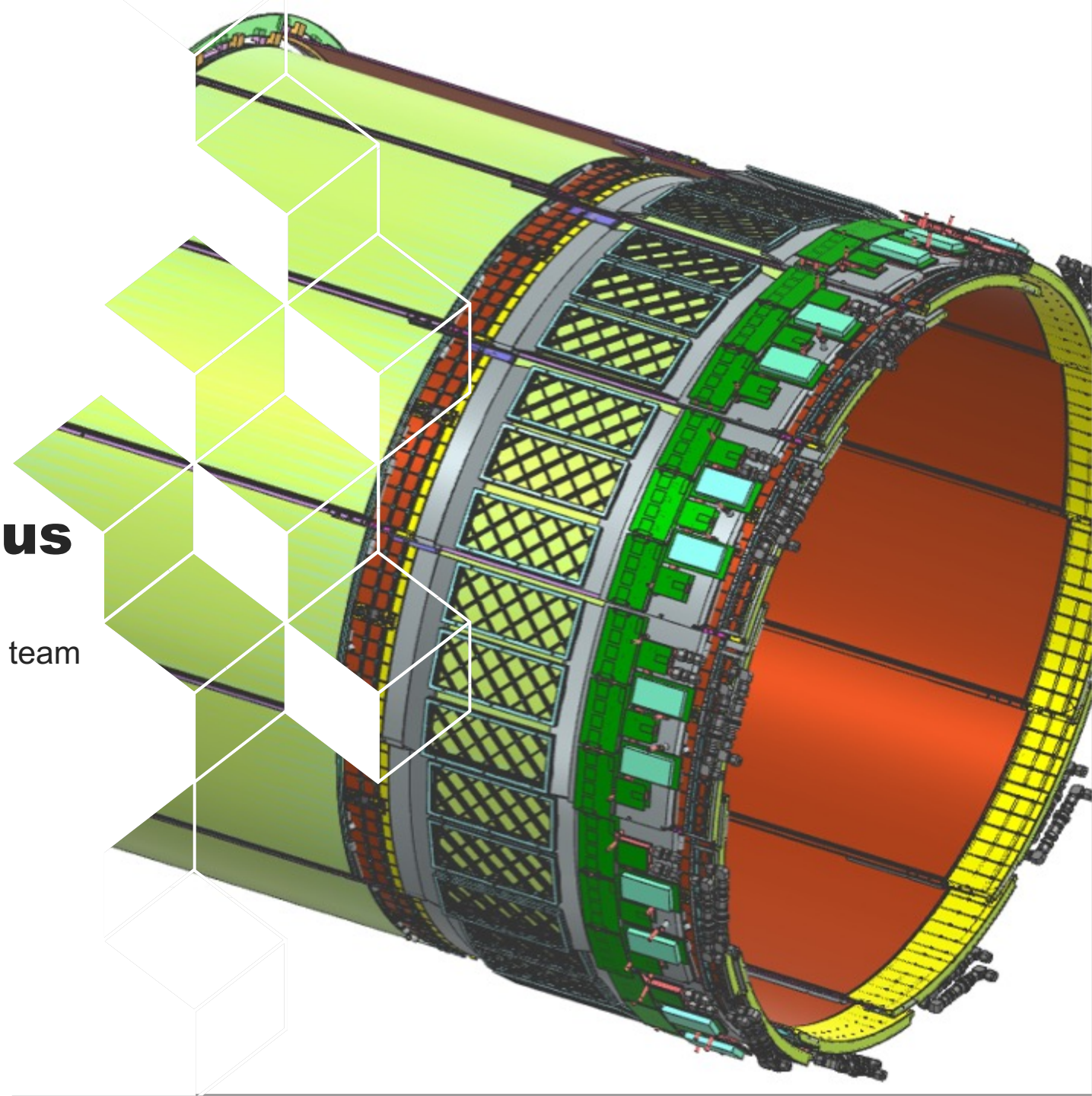
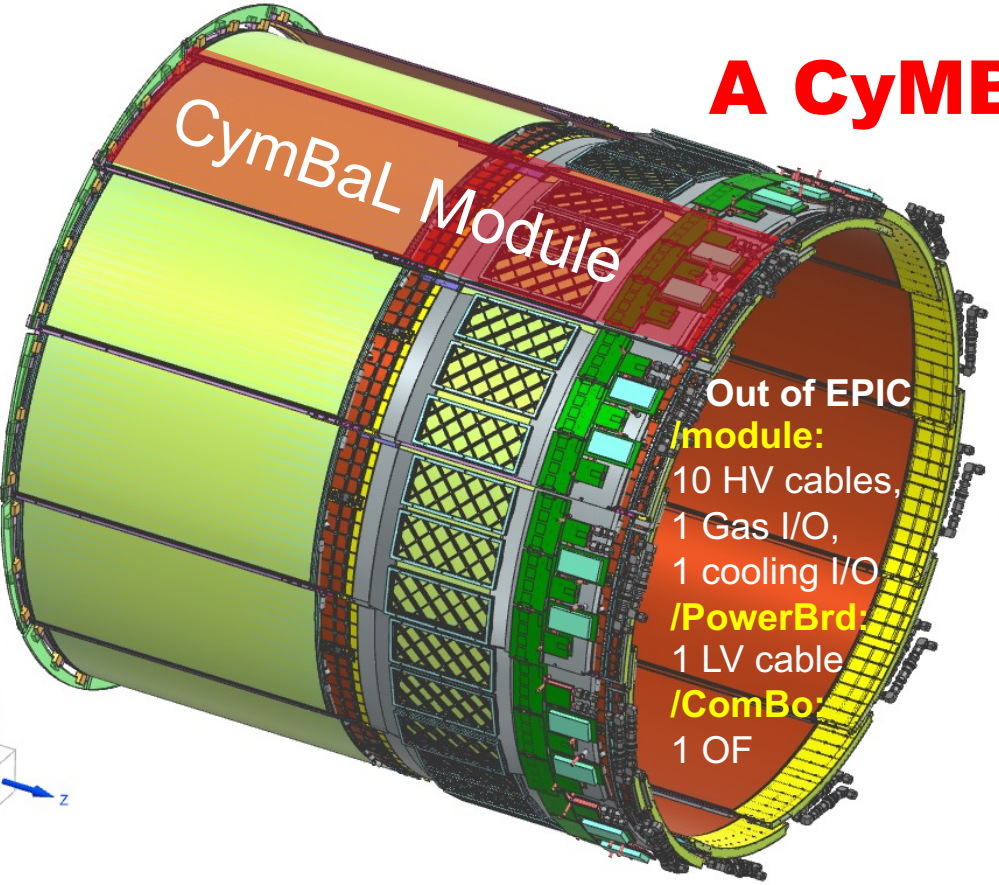
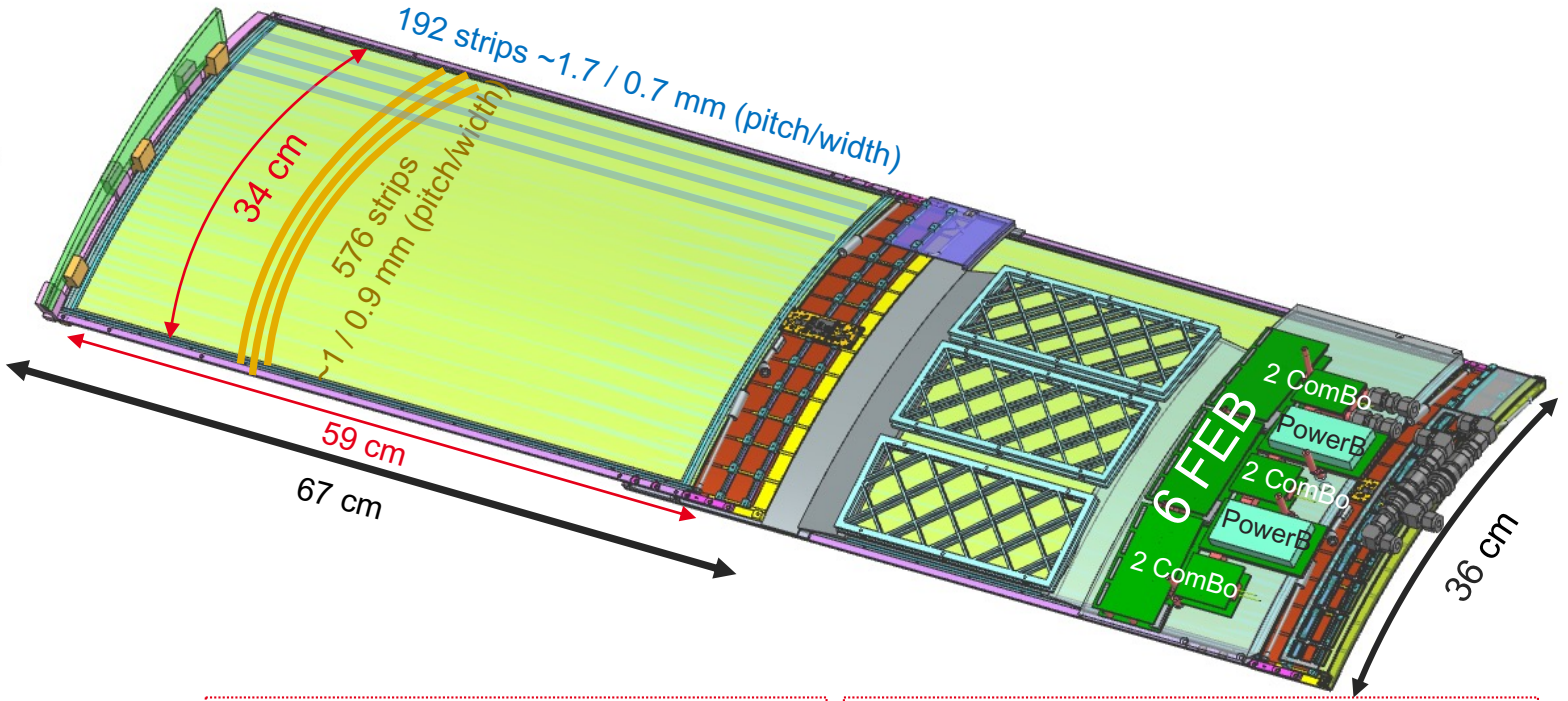


EIC/EPIC 3I meeting, 27 July 2026

A CyMBaL Module (a tray of 2 tiles)





48 tiles: 12 in ϕ × 4 in z (integration in GST in "fish scale")

- R_{min} = 55.5 cm; R_{max} = 61.5 cm **(6 cm thick envelop)**
- Overlaps in ϕ and in z for hermeticity (~2-4 cm)
- 768 readout channels/module
- **36K readout channels in 3 FEBs/tile (144 FEB with spares)**
- 18-20°C water cooling : ~19W/FEB, 58W/tile, 2.8 kW total

Module dimensions

Z = 67.3 cm / R*phi = 36.6 cm

Active zone dimensions

Z = 59 cm / R*phi = 34 cm

Weigh estimates

~1 kg/tile + ~1 kg (Al)-2kg(Cu)/6FEB.

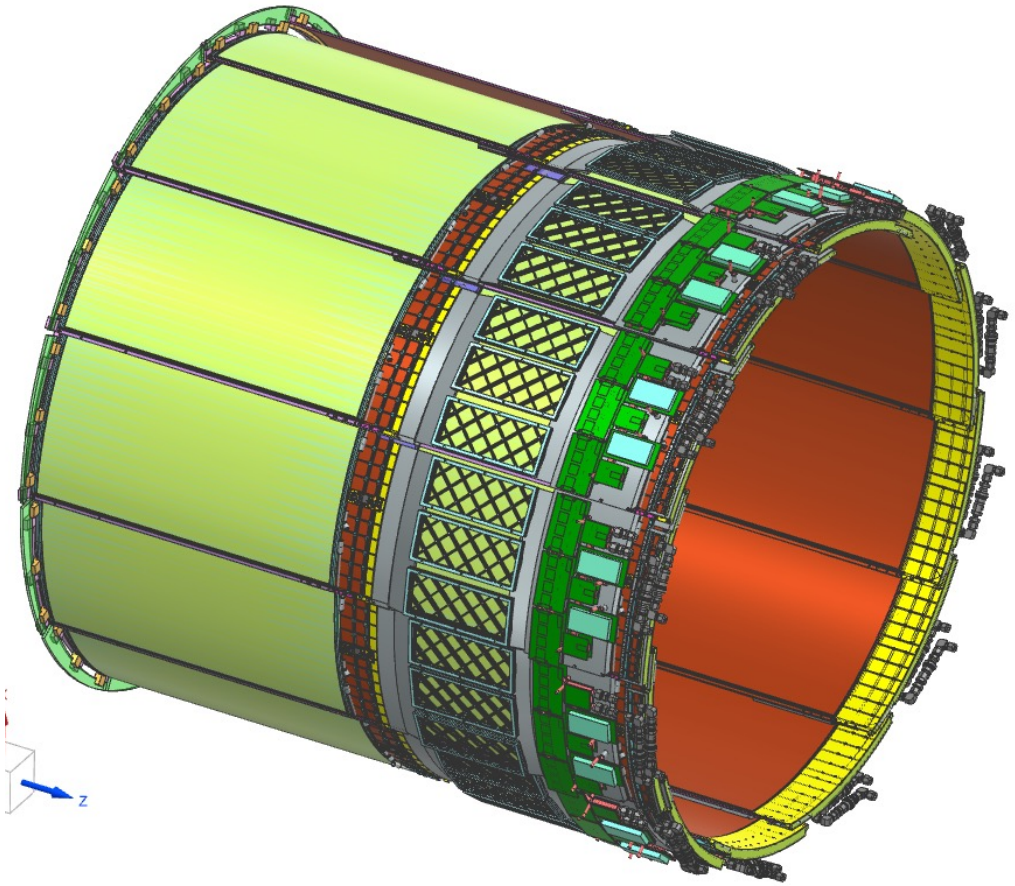
2 tiles tray: 5kg / 120 kg total

Expected performances

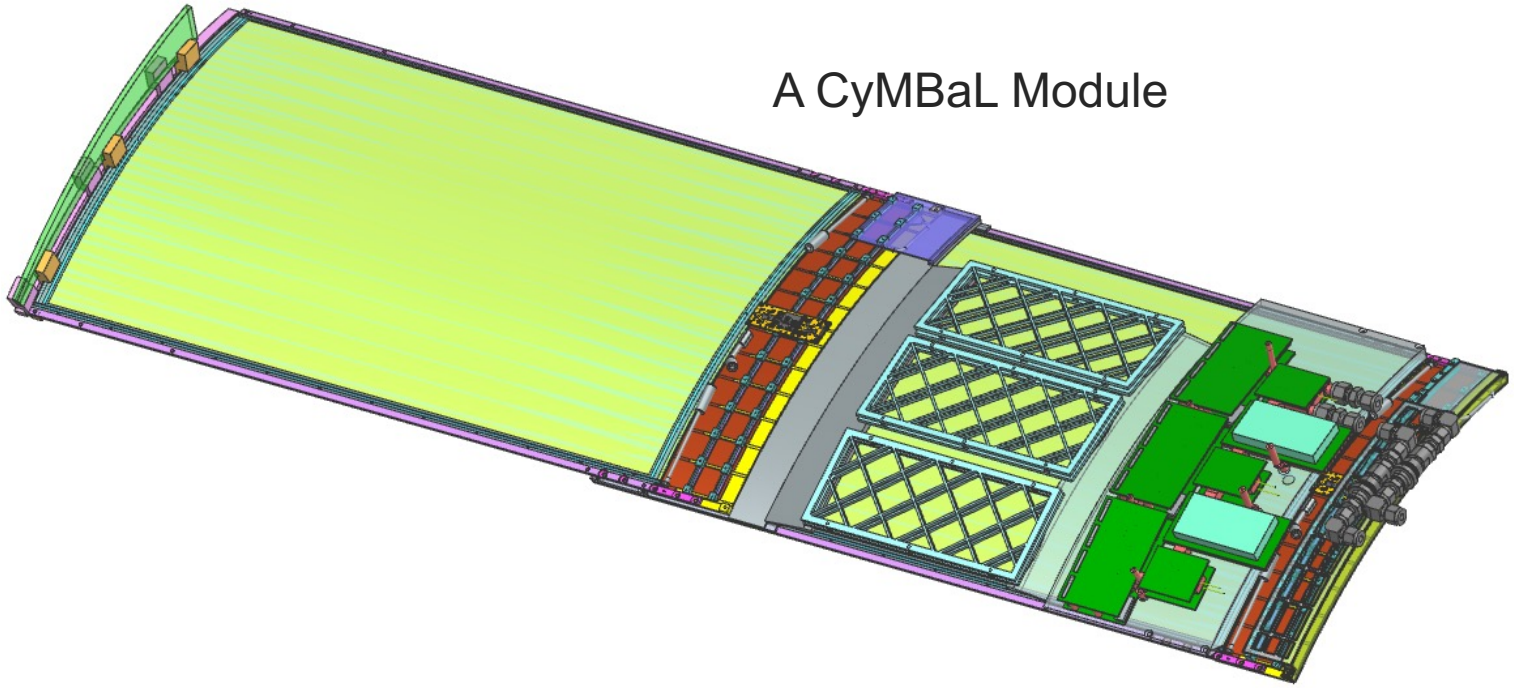
- Spatial resolution: < 300 (500) µm in Z (r*phi)
- ~1 mm (z) /~1.7 mm (phi) pitch
- Time resolution ~20ns
- Efficiency ≥ 98%
- Material budget ~0.5% X0

Current design of CyMBaL inner MPGD barrel

Half CyMBaL barrel

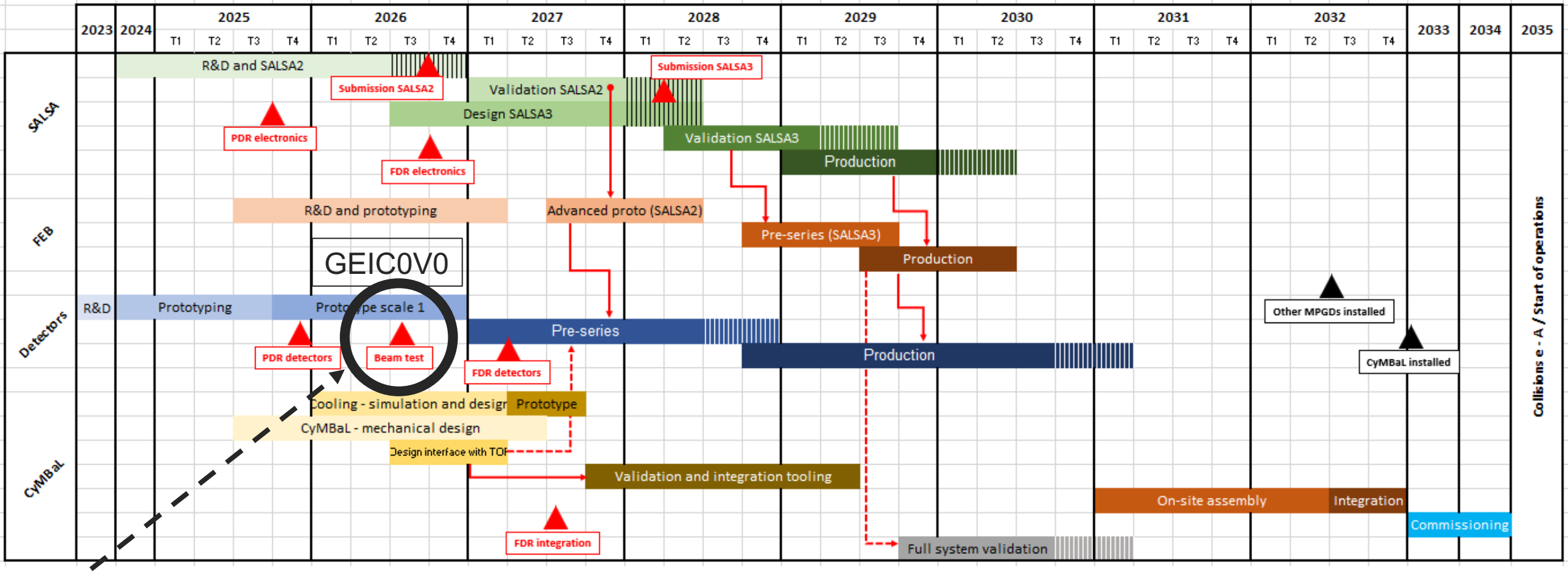


A CyMBaL Module



- **Reference design** from **march 2026** for the scale 1 test article of a CyMBaL Tile (called **GEIC0V0**), and integrated in the current global CAD model of EPIC.
- Module design to be updated for **integration in a « TOF-CyMBaL super-tray »** as soon as a CAD model of a TOF tray is available to work with.

CyMBaL development+production Timeline



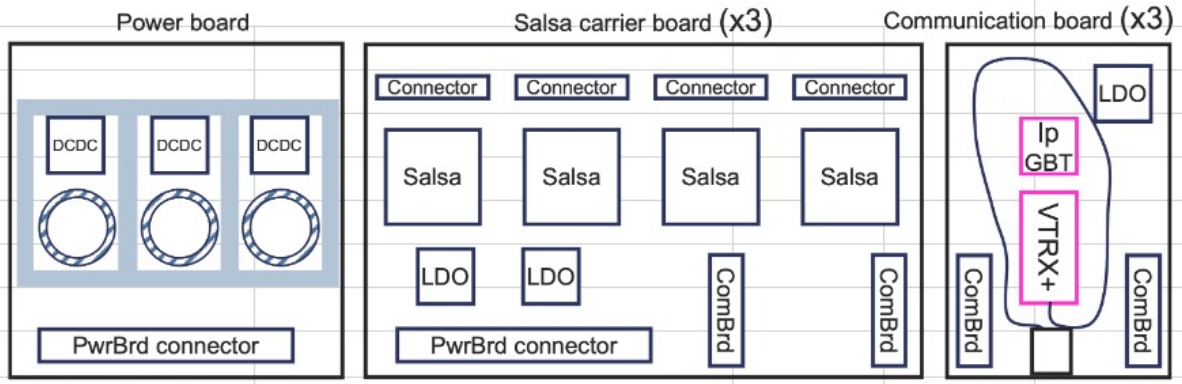
- Production of the 2x5 GEIC0 PCB **delayed from 7 to 15 weeks → new expected delivery mid august.**
- 07/15 – 08/02 GEIC0V0 test beam at CERN was therefore canceled.
- Should be able to have a GEIC0V0 tile to test **with cosmics** ~end of september.

A CyMBaL Module = 2 CyMBaL tiles = 6 (FEB/SALSA Carrier + ComBo) + 2 Power Boards = 2 * 768 ch. (2026/07/06 update)

Cooling Scope of Work			
			Unit
Cooling media		Water	
Inlet Temperature		22	°C
Ambient Temperature		23	°C
Cooling Block equivalent Inner Diameter		4	mm
Cooling Block Material		Copper	
Operating Temperatures of components			
	SALSA	25	°C
	DC/DC	?	°C
	LDO	?	°C
	lpGBT	?	°C
	VTRX	?	°C
Maximum Temperature of components			
	SALSA	35	°C
	DC/DC	?	°C
	LDO	?	°C
	lpGBT	?	°C
	VTRX	?	°C
Temperature Rise		0.5	°C
Temperature Stability (+/-)		2	°C
Flow Rate of a single Module		3	l/min
Pressure drop of a single Module		0.04	bar
Heat Dissipation to ambient		3	W
Total Heat Dissipation to ambient		72	W
Cooling loops		24	
Insulation requirement		NO	
Neighboring detectors		SVT, TOF	

Detailed Power Estimates (1 Module)				
		Power (W)	Qty	Total Power (W)
Power Board				**26,4**
	DCDC (1,5V/8,5A) 70%	4,4	6	26,4
FEB (SALSA Carrier)				***72***
	SALSA (1.2V/2A)	2,4	24	57,6
	LDO (1.5V/2A)	0,6	24	14,4
Communication Board				**13,40**
	LDO lpGBT (1.2V/0.5A)	0,6	6	3,6
	LDO VTRX+ (2,5V/0.07A)	0,175	6	1,05
	LDO VTRX+ (1.5V/0,44A)	0,66	6	3,96
	lpGBT (1.2V/0.5A)	0,6	6	3,6
	VTRX+ (2.5V/0.07A & 1,2V/0,02A)	0,199	6	1,194
Total (1 Module)				**111,80**
Total (24 Modules)				**2683,30**

1 tile R/O (for illustration only : just to show component types)



Simulation of Module R/O electronics cooling

22degC Water

3 l/min

PSalsa = 2.4W

Max TSalsa = 35 degC

Including:

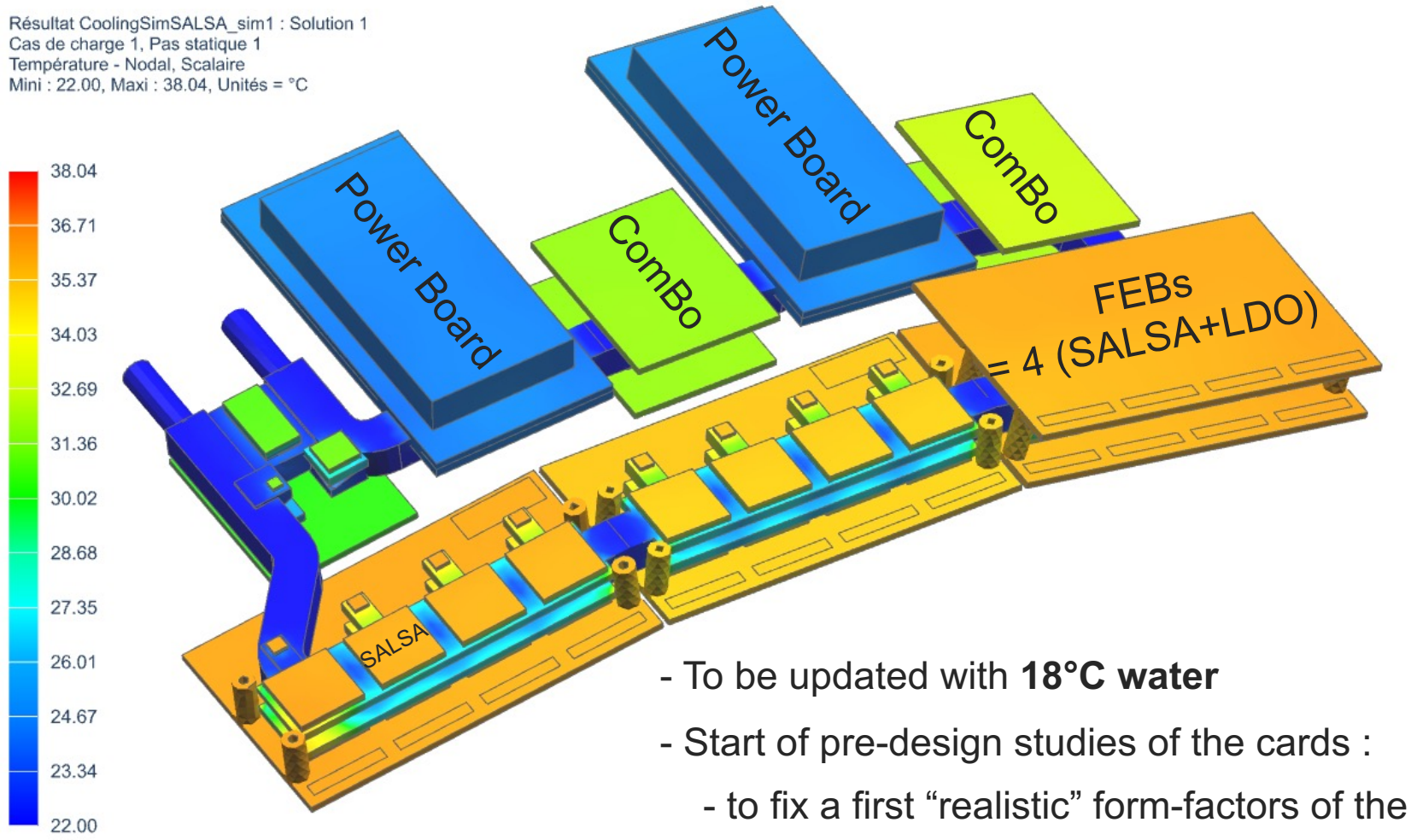
Gap Pads 2W/mK

Chip encapsulation 1W/mK

FR4 Boards 0.3W/mK

deltaT = ca. 0.5 degC

deltaP = 0.04 bar (without any connectors to specify)



- To be updated with **18°C water**
- Start of pre-design studies of the cards :
  - to fix a first “realistic” form-factors of the cards
  - to develop “mechanical” prototypes of (card + heatsink) test their integration with the GEIC0 tile

Cooling Block

3D printed Copper Block

Integrated cooling channels

Minimal Material usage

Integrate all possible features

Aim to produce a “cooling” prototype made of heatsink block and “mechanical” mockup cards in Q1/2027