EICROC2 digital architecture status

16th July 2026

Readout architecture

1) Periphery

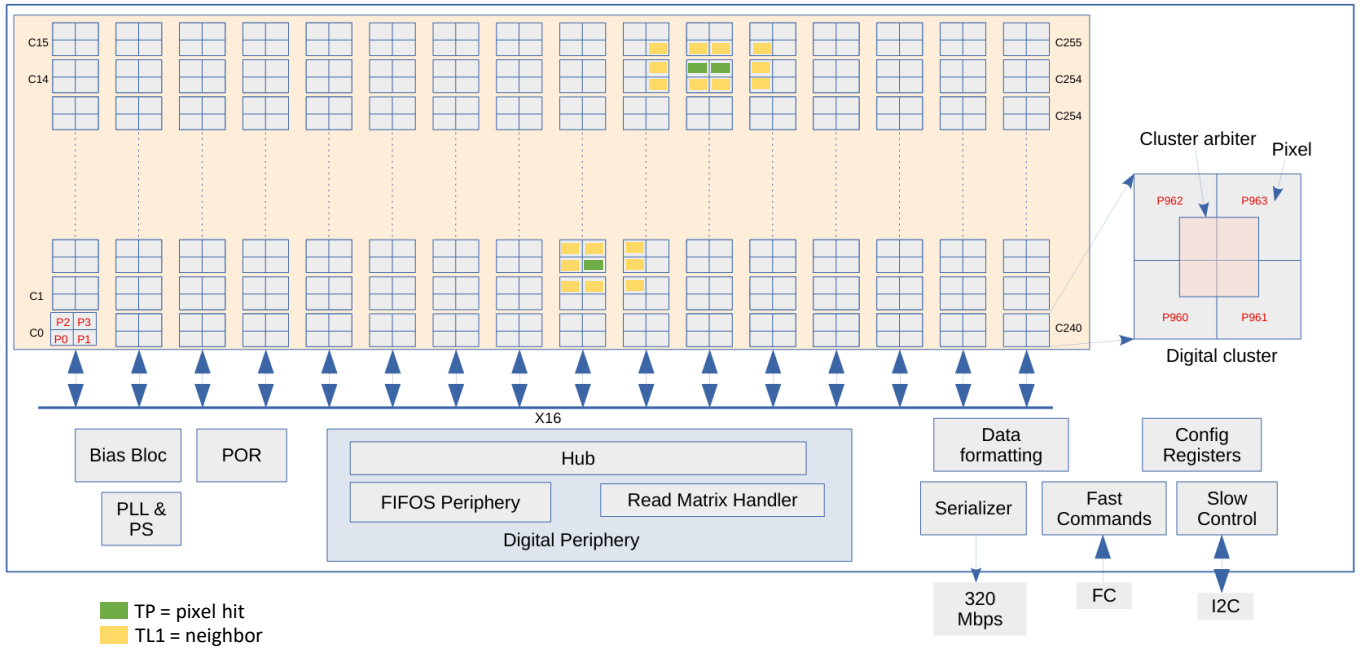
Handle zero suppression, data formatting, serialization, control the pixels..

2) In-pixel logic

Based on clusters of 4 pixels,

Data transmission using ready/valid protocol

- Logic shared at cluster level
- Shared data bus between 2 columns



Constraints :

- Minimize digital logic inside pixel/matrix
- Minimize signals between matrix and periphery
- Triplication of sensitive circuits
  - **No triplication on data path**

Architecture status

In-pixel logic

- Use of ADC SAR instead of ramp ADC inside pixels, providing 4 ADC values per pixel (instead of 1 value)
- Need to implement buffer to store 1 (or 2?) ADC value before the hit for pedestal evaluation
- Clock gating on ADC in discussion

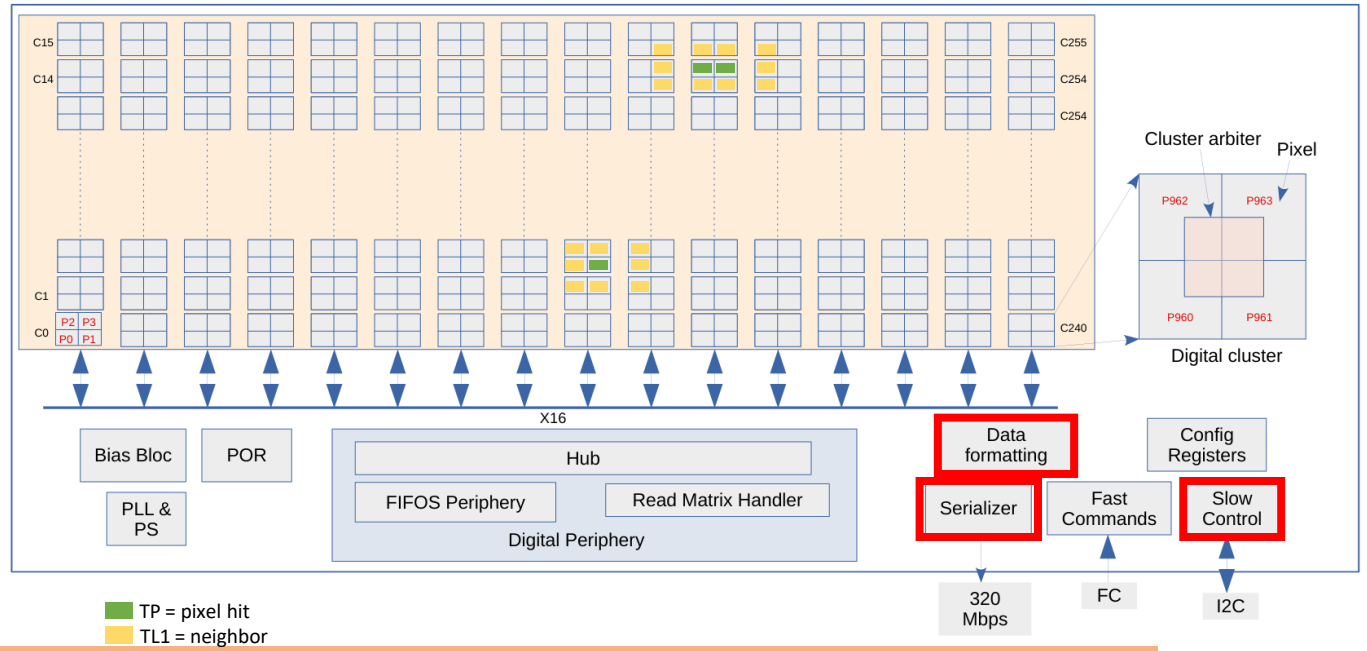
➔ RTL updated, simulations on-going

- Digital in cluster is now taking too much area (optimizations necessary)

Periphery digital blocks design has started :

- DataProcessing (encoding 8b/10b, frame formatting, zero suppress)
- Serializer 320Mbps
- I2C slave

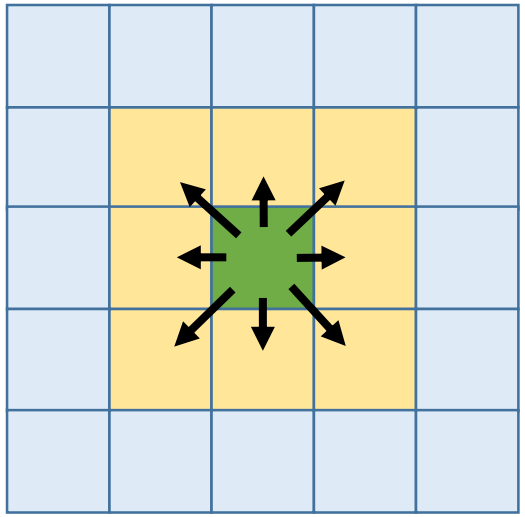
➔ First version of these blocks is under simulations



Open question 1 : Triggers for neighboring pixels

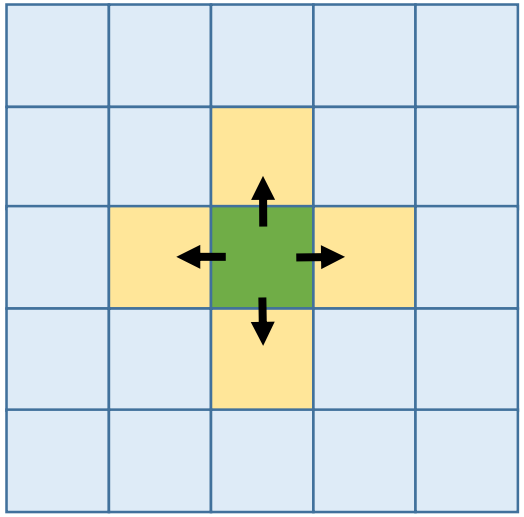
TP : pixel receiving a hit, provide TDC and ADC data

TL1 : pixel receiving a trigger order from a TP, provide ADC data only



Case A : 1 hit, read 8 neighbors

Complex routing, hard to implement



Case B : 1 hit, read 4 neighbors

Automatic routing by abutting, easy to implement

- Trigger scheme is an important choice for the design, impact complexity of the chip
- Need to know which trigger scheme is the baseline

Open question 2 : Frame Format

Header : 32b					Payload : 64b per pixel								Trailer : 32b			
SOF	Type	Error	BCID	Parity	Pad	pixAddr	Hit	TDC	ADC0	ADC0	ADC0	ADC0	EOF	N_pix	CRC	Pad
12b	2b	5b	12b	1b	11b	10b	1b	10b	8b	8b	8b	8b	8b	8b	8b	8b

- Header
  - SOF (StartOfFrame)
  - Type : Data acquisition mode / Serializer sending fixed pattern, etc ..
  - Error : Flags for FIFO levels, etc..
  - BCID : BCID value associated to this hit
  - Parity : Calculated as the XOR of the other 31 bits composing header

- Payload :
  - pixAddr : 10b
  - Hit bit
  - TDC : 10b
  - ADC0/1/2/3 : 4 x 8b

- Trailer :
  - EOF (EndOfFrame)
  - N_pix : Number of hits in this frame 8b
  - CRC : Standard CRC-8 AUTOSAR calculated on payload

- Encoding 8b10b (optional) : K28.5 outside frames for resynchro. MSB first

Maximum Hit rate

A hit corresponds to a triggered pixel : noise, particle interacting with AC-LGAD sensor
One hit is composed of several pixels to read, for example 9 pixels for the 8 neighbors case

Performances	8 neighbors 4 ADC values per pixel	4 neighbors 4 ADC values per pixel	8 neighbors 1 ADC val per pixel	4 neighbors 1 ADC val per pixel
Number of bits per frame (with 8b/10b encoding)	800 bits	480 bits	440 bits	280 bits
Output period for one hit (320MHz serialization)	2.5 µs	1.5 µs	1.37 µs	0.88 µs
Maximum hit rate per pixel	**390 Hz**	**650 Hz**	**710 Hz**	**1116 Hz**

This table do not take into account that a particle intercation may lead to several triggered pixel

- **Bottleneck is from serialization at 320MHz**
- A FIFO in the periphery allows to cope with several hits : Must know how many hits we need to store
  - Need an accurate simulation (burst of events, noise rate)
  - FIFO size cost large area and increase power consumption

Physical implementation status

- Layout of a cluster using pixel analog front end dummy
- Assembly of clusters into a full column

Recent changes on ADC impacted the area, digital do not fit in the in pixel-logic anymore

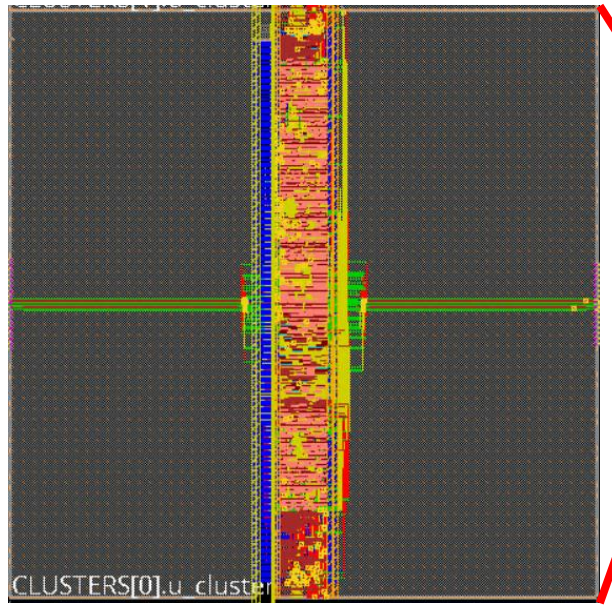
➔ Improvements to reduce area are needed

➔ Issue linked to any technology change

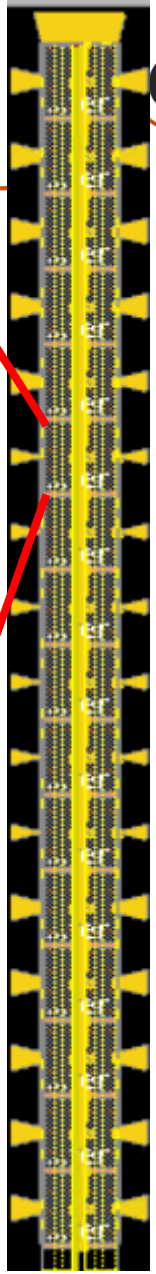
➔ Triplicated registers account for ~60% of the digital area

➔ A possible solution would be to ‘reduce’ the triplication of config registers

Depend on the radiation specs for SEE



Cluster of 4 pixels



Column

Summary

- Digital design status
  - Periphy blocks design has started
  - Investigation needed at cluster level to fix area issues

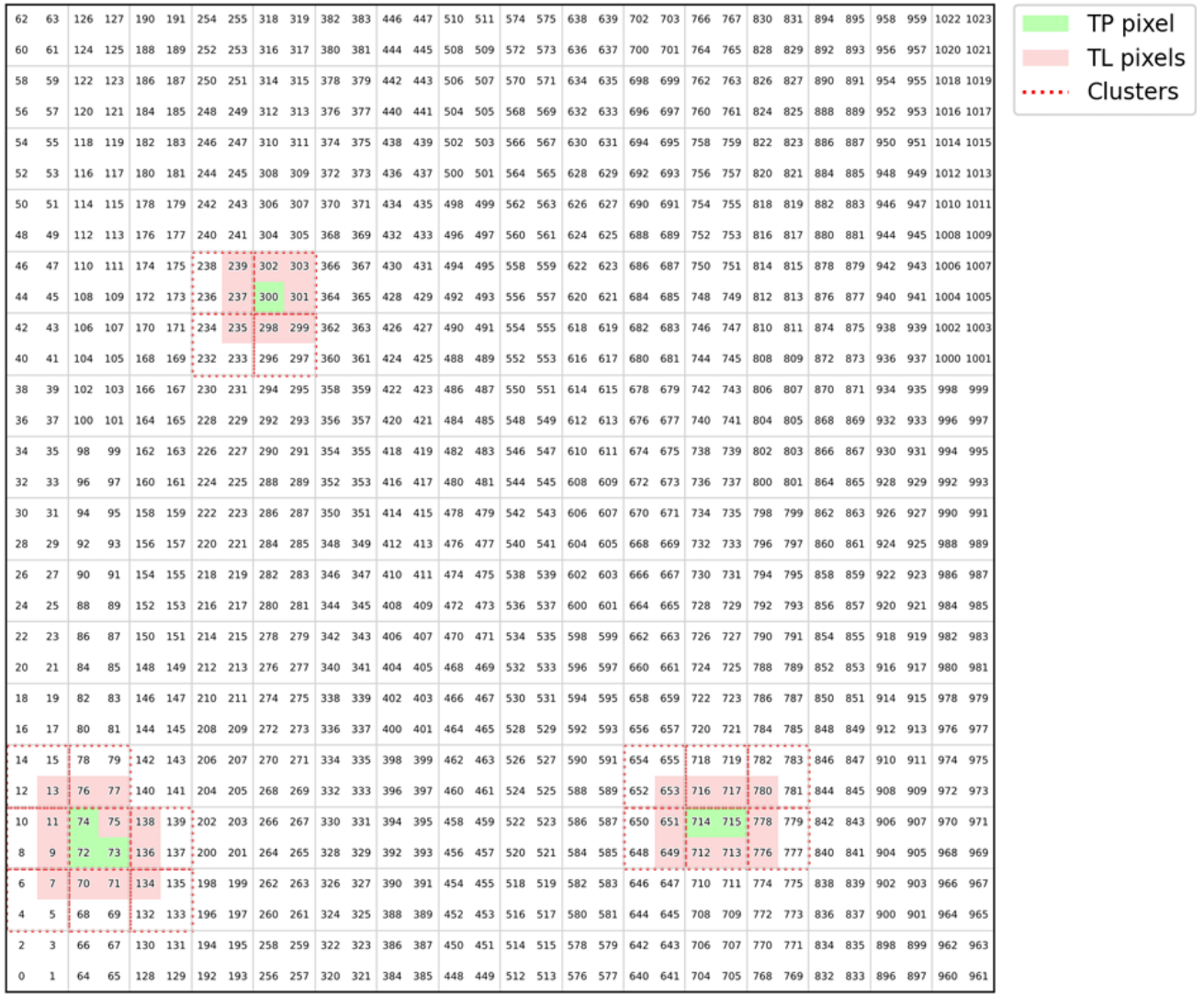
- Next steps:
  - **Technology change ?** (What techno ? What design kit available ?)
  - Analog Front End final choices
  - Clear specifications on trigger scheme (4 or 8 neighbors to read?)
  - Specification on radiation hardness (SEE)

Backup

Architecture overview

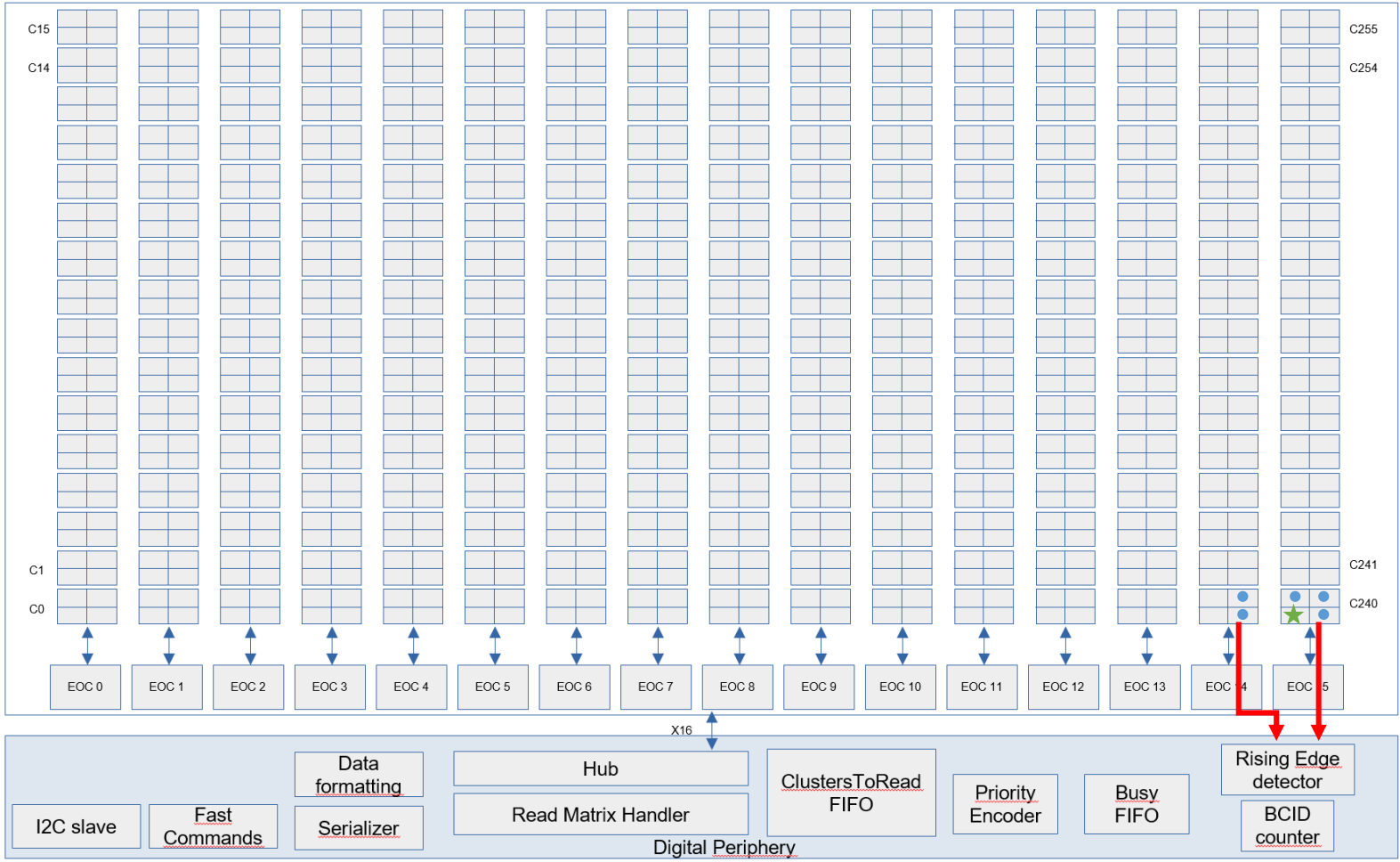
- One hit can have multiple TP

➔ Not an issue for this readout architecture



Architecture overview

1. Clusters send a busy signal to periphery when one of their pixels is hit



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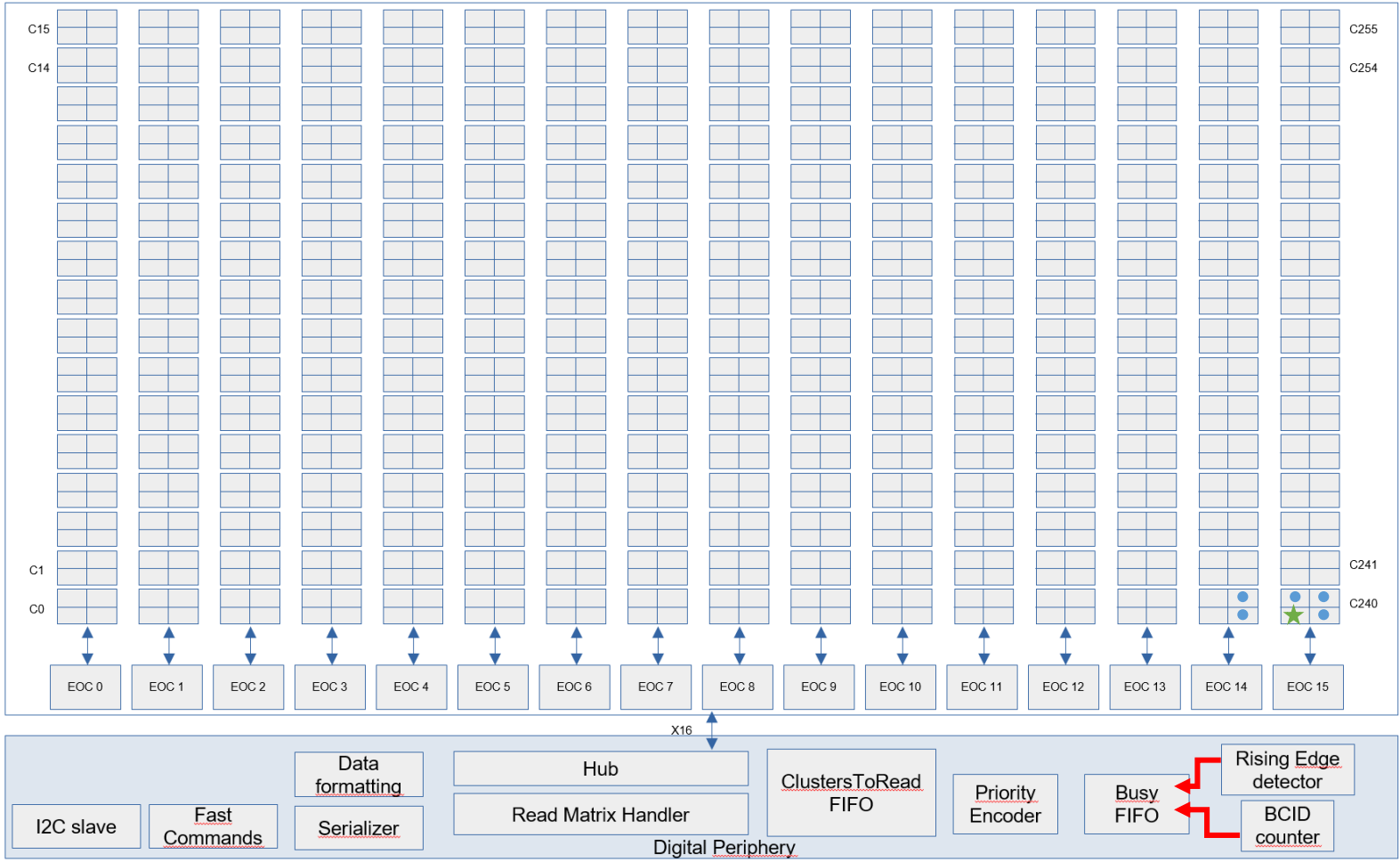

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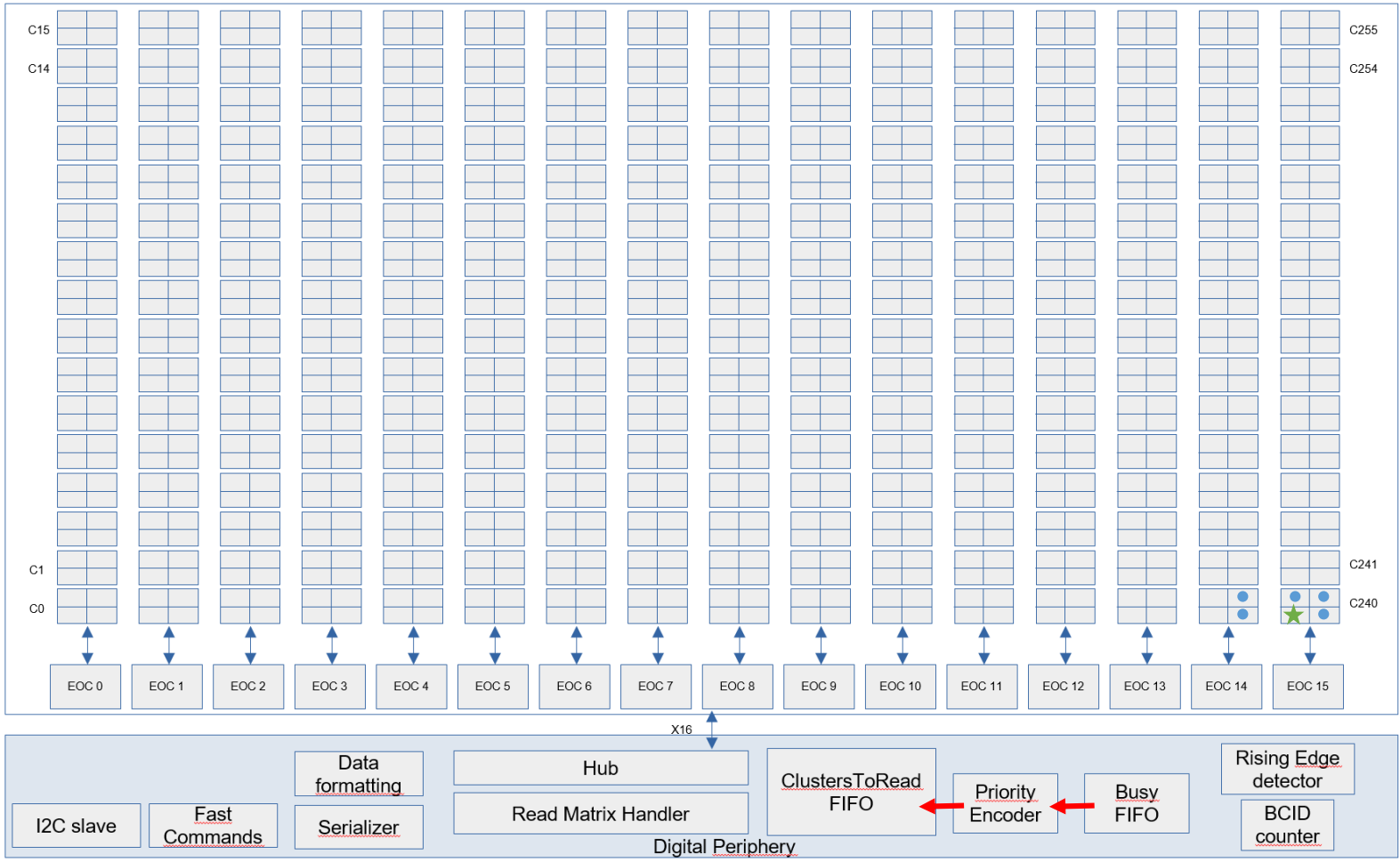

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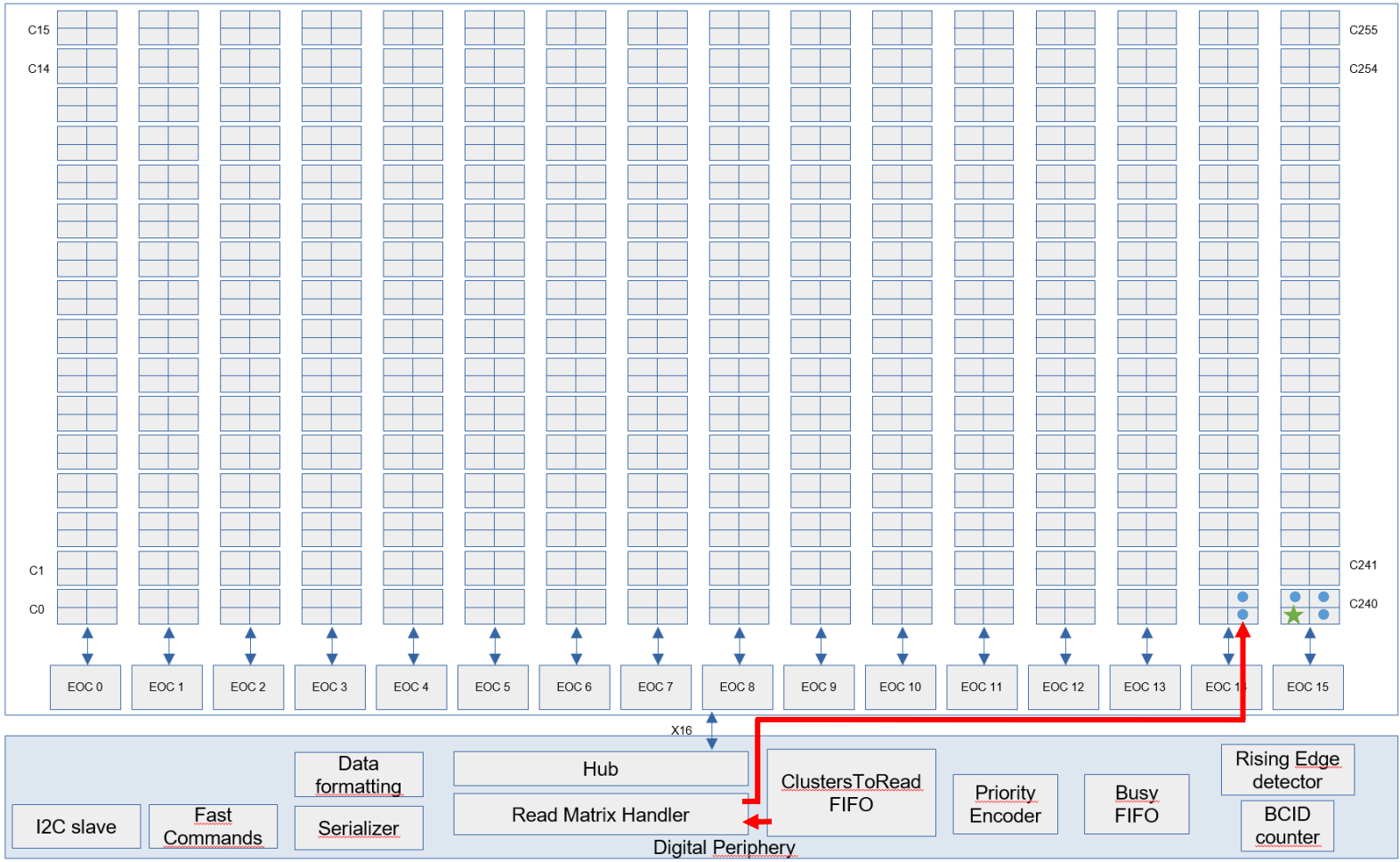

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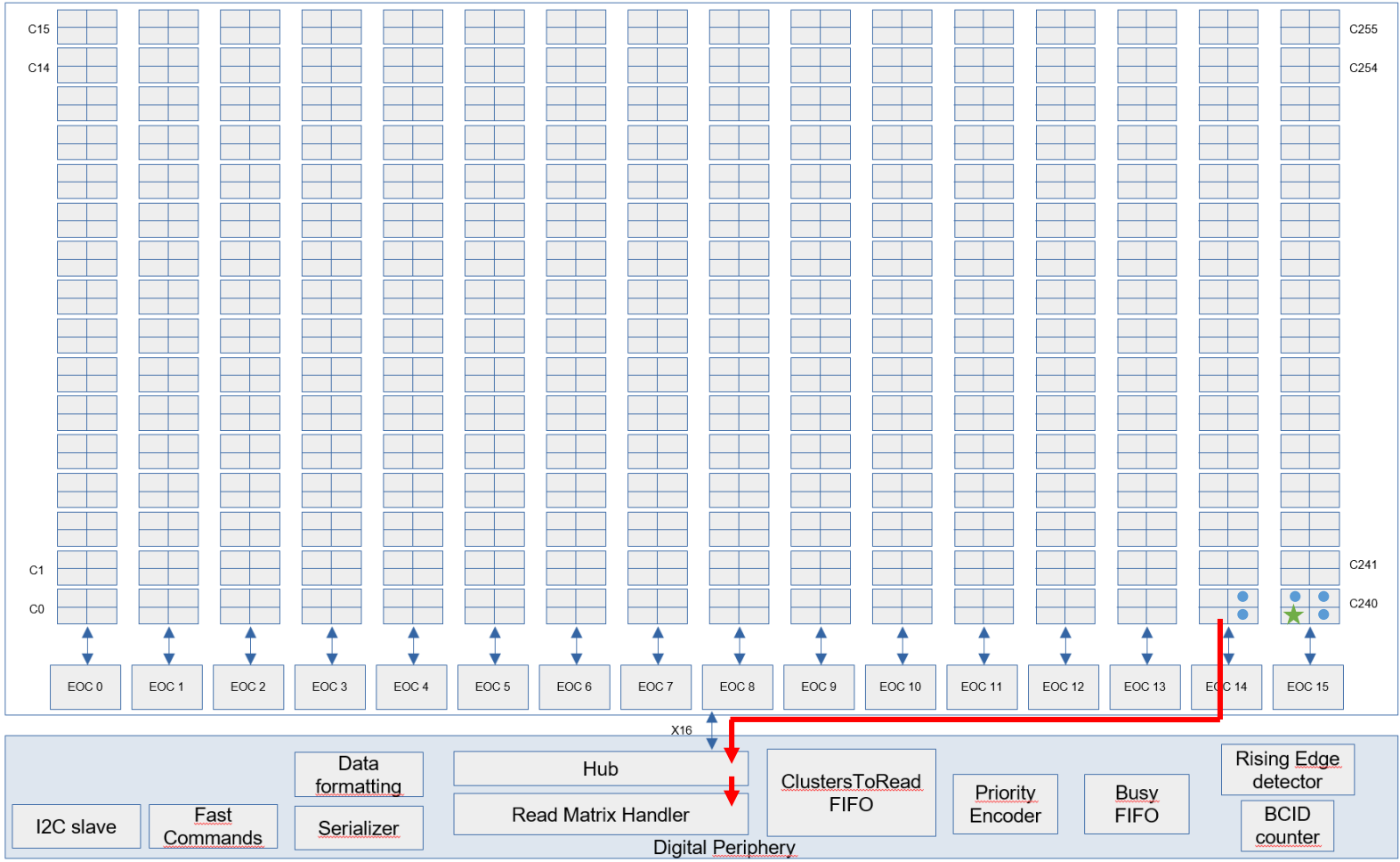

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5. Cluster send pixels data (ADC+TDC) when it is adressed
6. Data are formatted then serialized before being output of the chip (BCID, pixID, TDCdata, ADCdata)