SVT Disk FPC Design — Progress Update —

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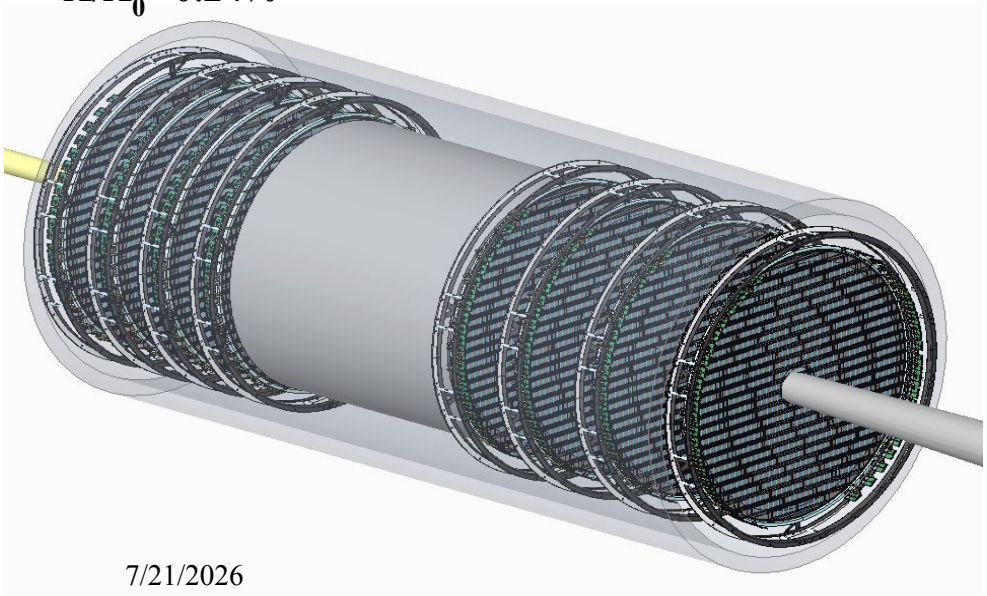
Previous report: ePIC SVT DSC meeting (April 14, 2026) · Indico

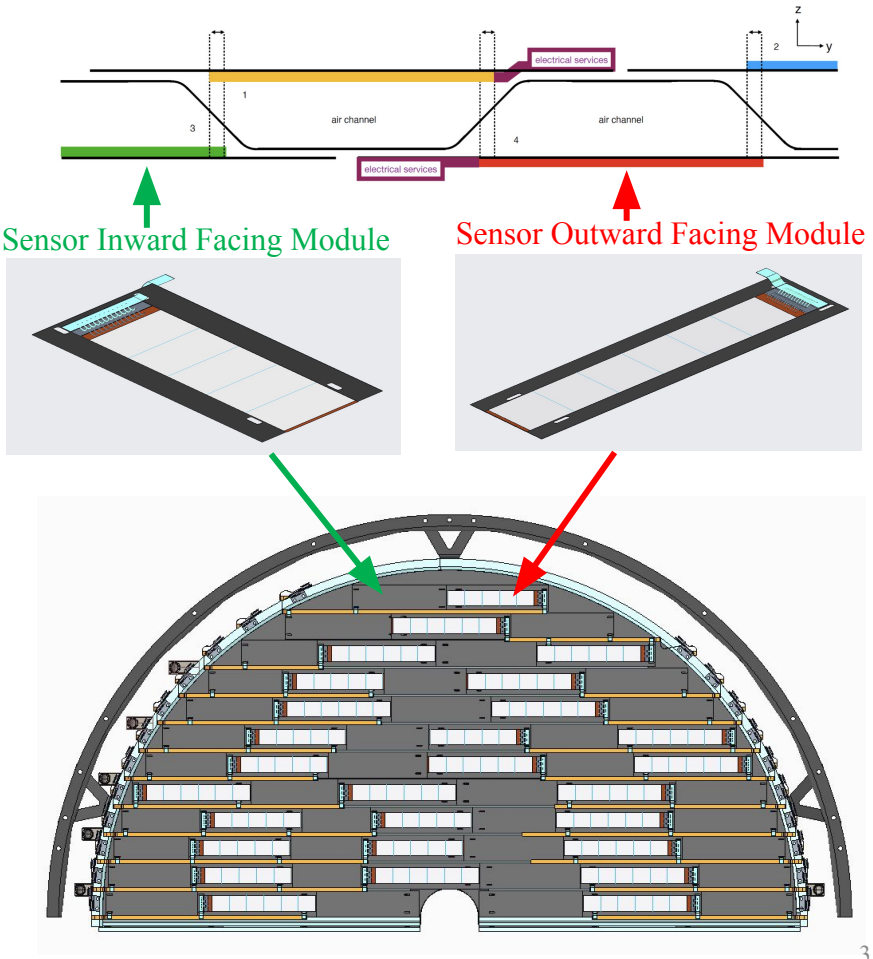
Summary and Outlook from 04/09/2026

- **A first layout design has been completed for SVT disk FPCs:**
  - This design include MFPC and BFPCs for outward facing modules.
    - takes into account the requirements of power and data transmission.
    - provides electrical interfaces between EIC-LAS, AncASIC and FIB (lpGBT and VTRX+).
  - Plan to produce a first batch of Cu-based mechanical prototypes to check FPC dimensions and inter-connection, with the main goal to facilitate disk module development.
- **Outlook**
  - Once the first version of the FPC is received, we will perform the following test:
    - Visual Inspection;
    - Soldering SMD components onto BFPC;
    - Cutting BFPCs;
    - Soldering BFPCs onto MFPC;
    - Mount and wire-bond between dummy EIC-LASs, AncASICs and BFPCs;
  - Design BFPCs for inward facing modules.

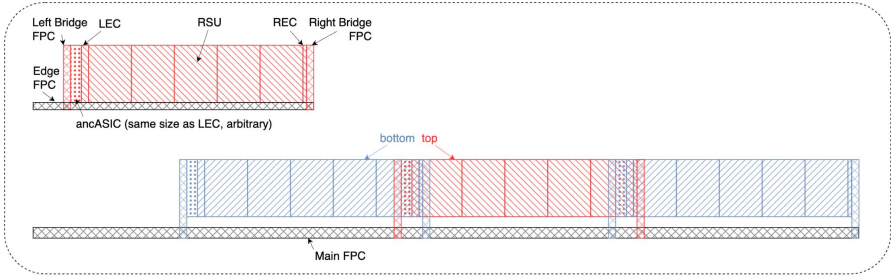
ePIC SVT Disks

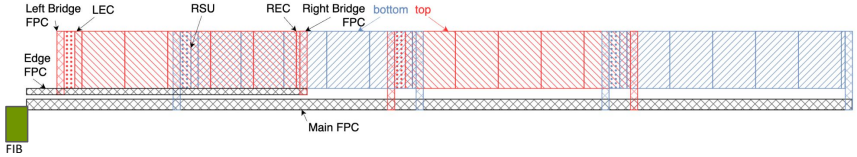
- **EIC Large-Area Sensor** with design based on ITS3 MOSAIX, mounted on low-mass CF support structure with integrated air cooling
- **AncASIC** provide negative sensor bias voltage, serial power and slow control
- **Outer radius** ranging from 24 to 40 cm
- **X/X_0** ~0.24%

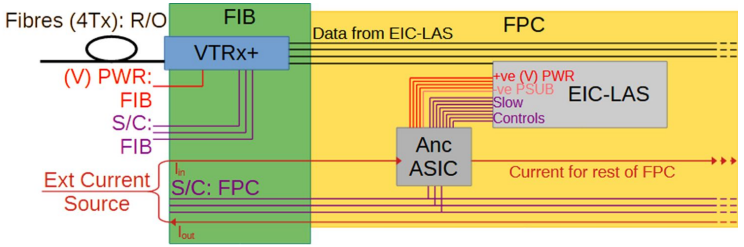




Electrical Interfaces for SVT Disks



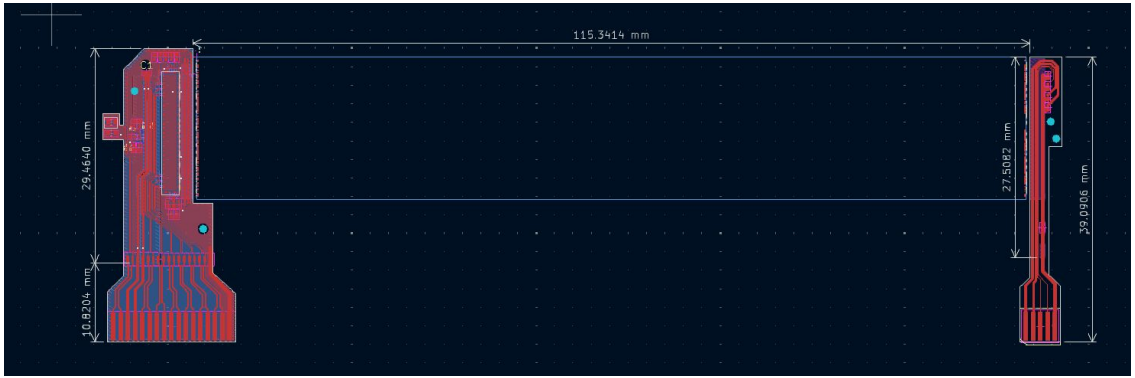




bold: preferred option

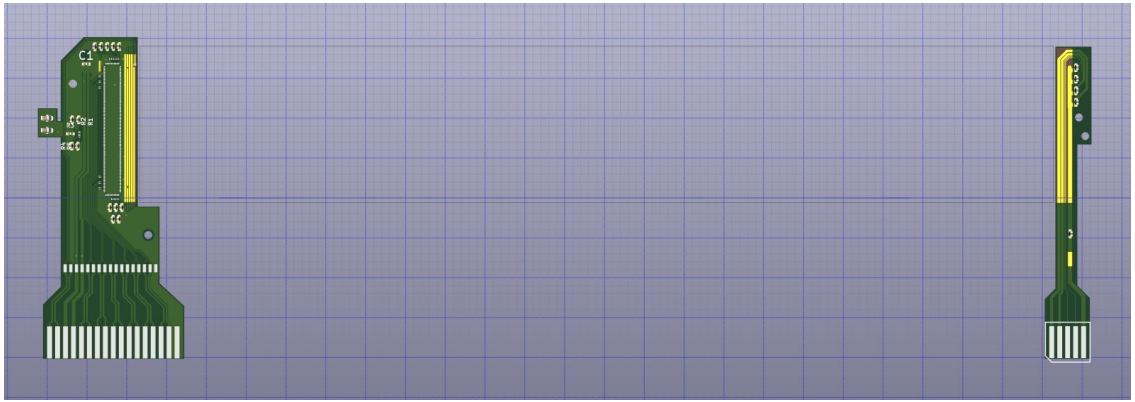
	FIB	Main/Edge FPC	Bridge FPC	AncASIC	EIC-LAS
FIB					
Main/Edge FPC	**Connector**, Soldering				
Bridge FPC	N/A	**soldering**, wire/TAB-bonding			
AncASIC	N/A	N/A	**wire-bonding**, TAB-bonding		
EIC-LAS	N/A	N/A	**wire-bonding,** TAB-bonding	**wire-bonding**	

BFPC_V1 - Overview



- **Left bridge FPC** with **AncASIC** will handle **EIC-LAS LEC** power, slow control, high-speed data transmission.

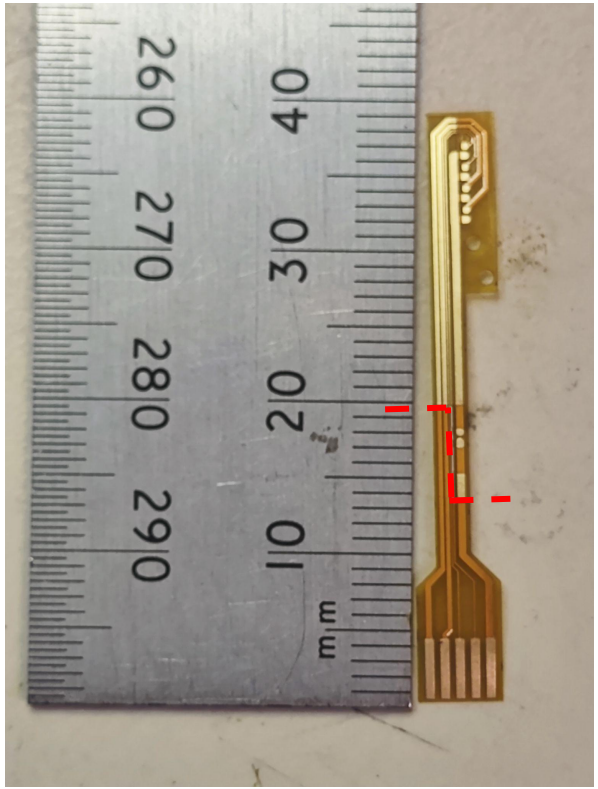
	Area (mm^2)	Copper area (mm^2)	Fill factor
Top Layer	278.2	190	0.69
Bottom Layer	278.2	260	0.94



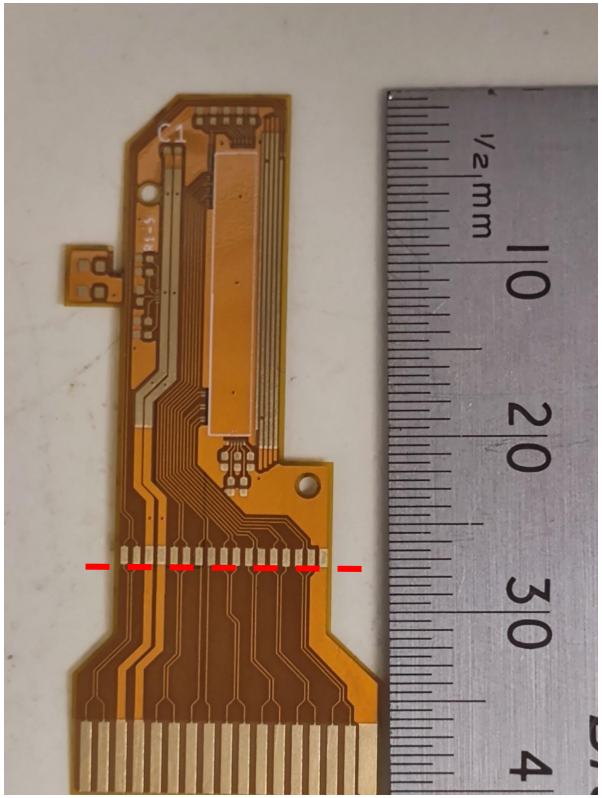
- **Right bridge FPC** with power buses connected to GND through decoupling capacitors will connect to the **EIC-LAS REC**.

	Area (mm^2)	Copper area (mm^2)	Fill factor
Top Layer	78.9	32.9	0.42
Bottom Layer	78.9	0	0

BFPC-Visual Inspection

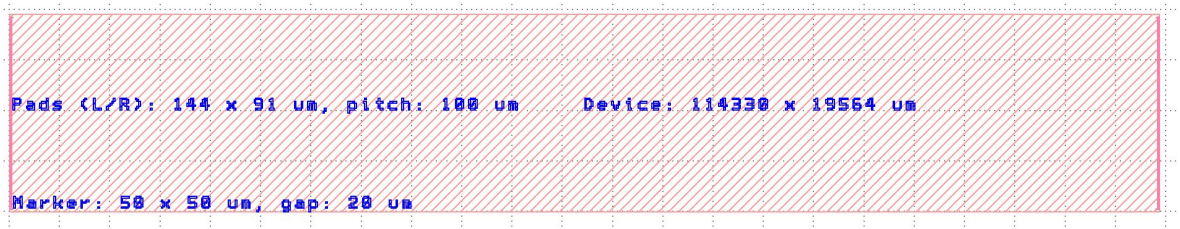


Cut lines

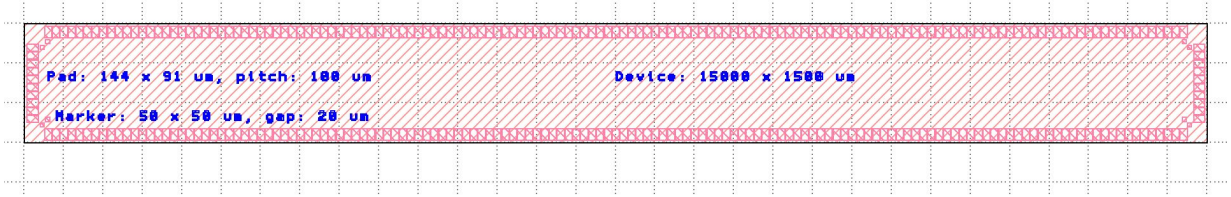


Disk Module with Dummy Chips and BFPCs

Dummy EIC-LAS and AncASIC (UK)



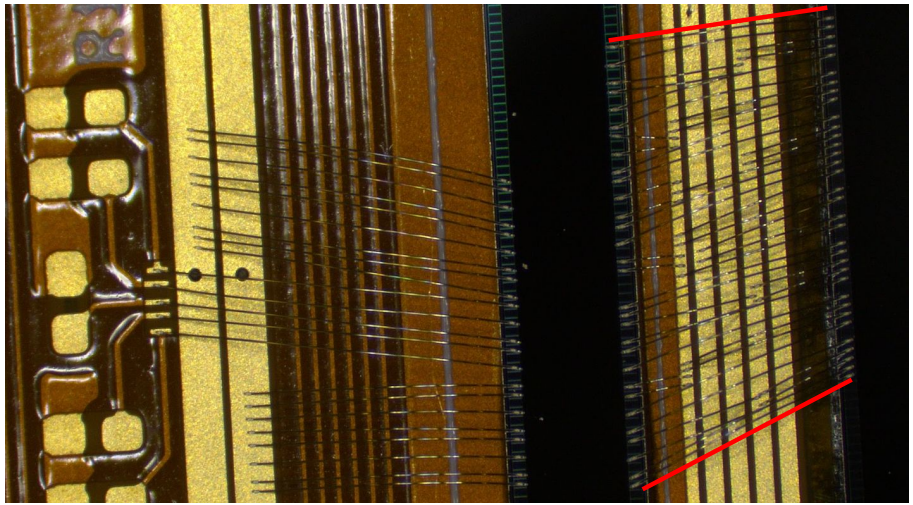
Dummy EIC-LAS: 191 pads on left/right edge

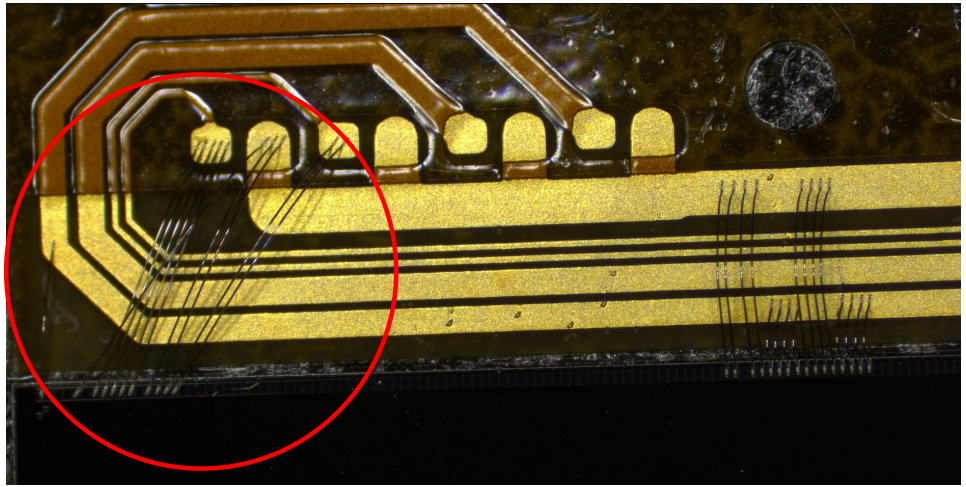


Dummy AncAISC: 145 pads on left/right edge
10 pads on the top/bottom edge

Since the dummy chip's pad positions differ from those on the real chips, we chose the dummy pads closest to the real pad locations for wire bonding test.

Wire-bonds between BFPC and Dummy Chips

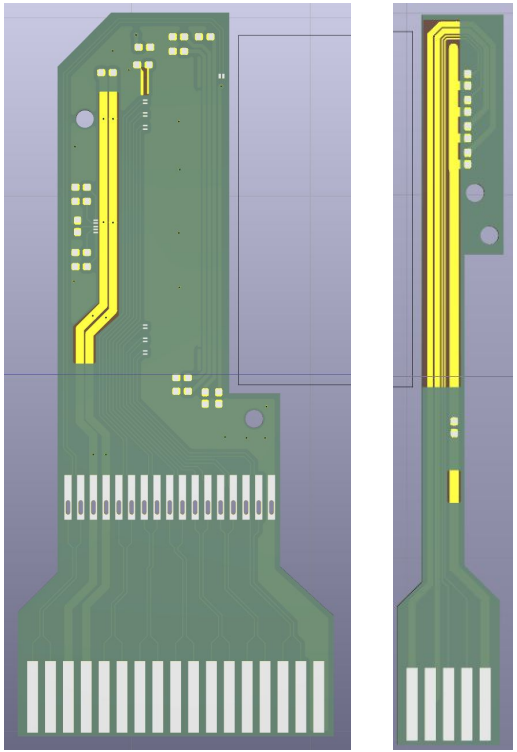




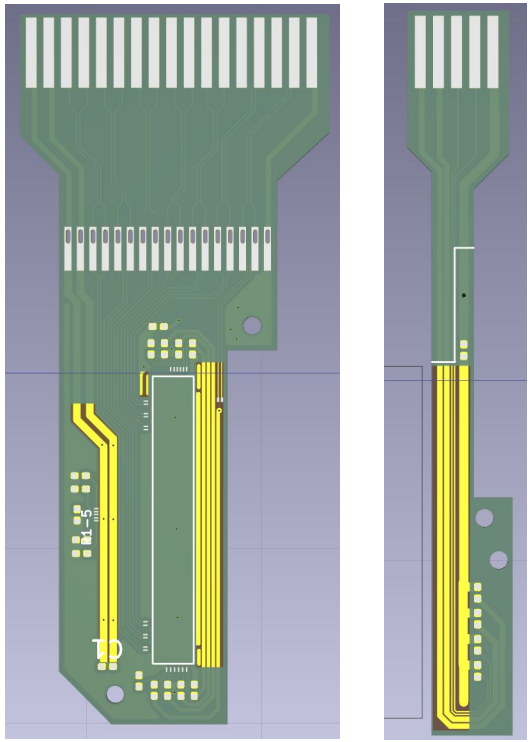
Wire bonding on selected regions has been completed, with no major issues overall. The wire bonding tech provided the following recommendations:

- **Left side**: The position of the AncASIC and its bonding pads should be positioned to facilitate straight wire-bonds, especially for those directly connecting between the AncASIC and LAS.
- **Right side**: the power bus lines aren't long enough, which makes wire bonding of the top pads of the LAS to BFPC somewhat difficult.

New BFPC Overview



Top view of outward facing module BFPCs



Bottom view of inward facing module BFPCs

Main modifications:

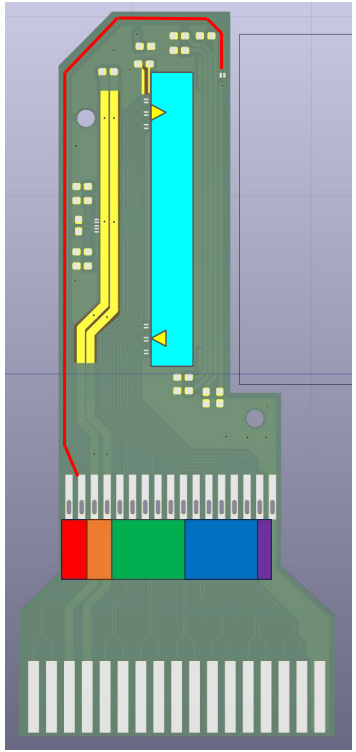
BFPC on left side:

1. Design the Inward version.
2. connected the decoupling capacitors to the power buses.
3. Optimizing the soldering pads to solder on MFPC

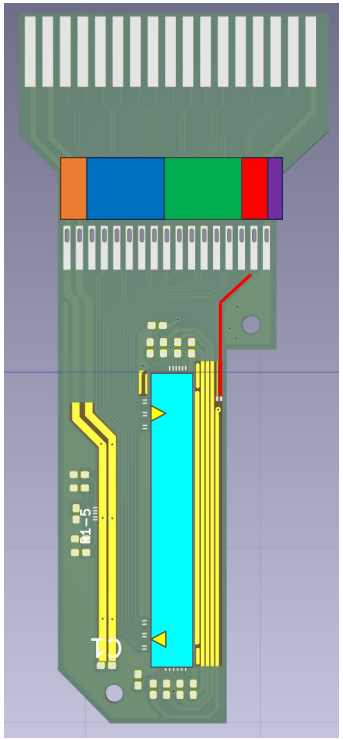
BFPC on right side:

1. Design the Inward version.
2. Increased the length of power buses for better wire bonding.

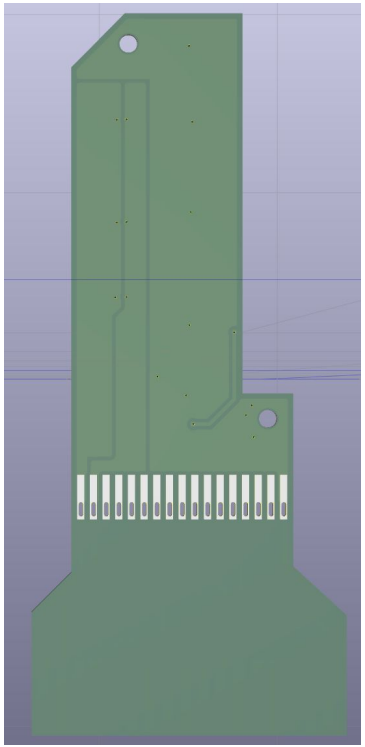
Outward vs Inward facing module BFPC



Top view of outward facing module BFPCs



Bottom view of inward facing module BFPCs



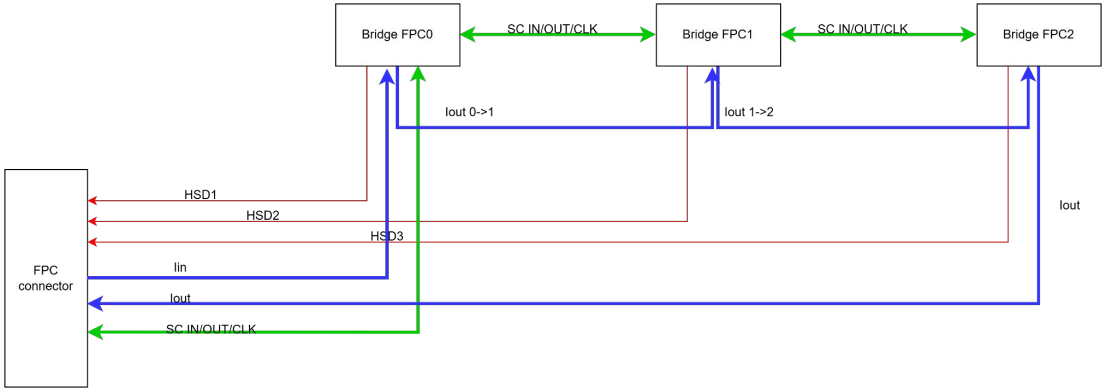
Top view of inward facing module BFPCs

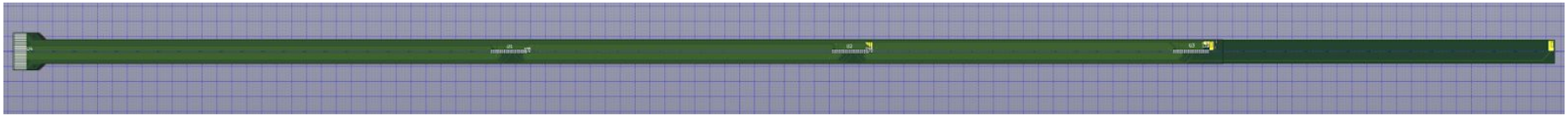
To convert the outward-facing module BFPC into an inward-facing module BFPC:

1. the soldering pad assignment at the interface between the BFPC and the MFPC was adjusted.
2. the connection scheme for the HSD and slow-control signals was modified.
3. In addition, after moving the entire main circuit to the bottom layer, the structures used for connecting to the MFPC were retained on the front side.

HSD
Iin/Iout
Slow-control from previous board
Slow-control to next board
GND

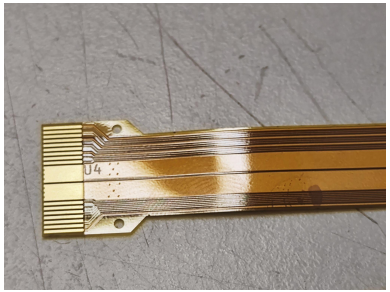
MFPC_V1 Overview

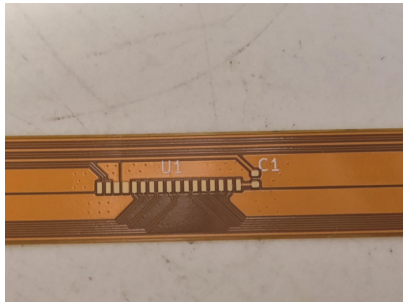


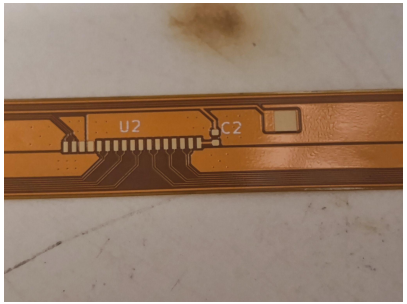


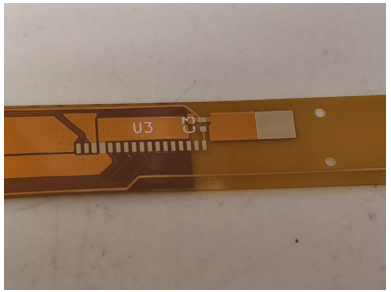
	Area (mm^2)	Trace Area (mm^2)	Power net area (mm^2)	Fill factor
Top Layer	4747.6	221.5	1875.6	0.45
Bottom Layer	4747.6	0	3202.2	0.68

MFPC_v1 - Visual Inspection

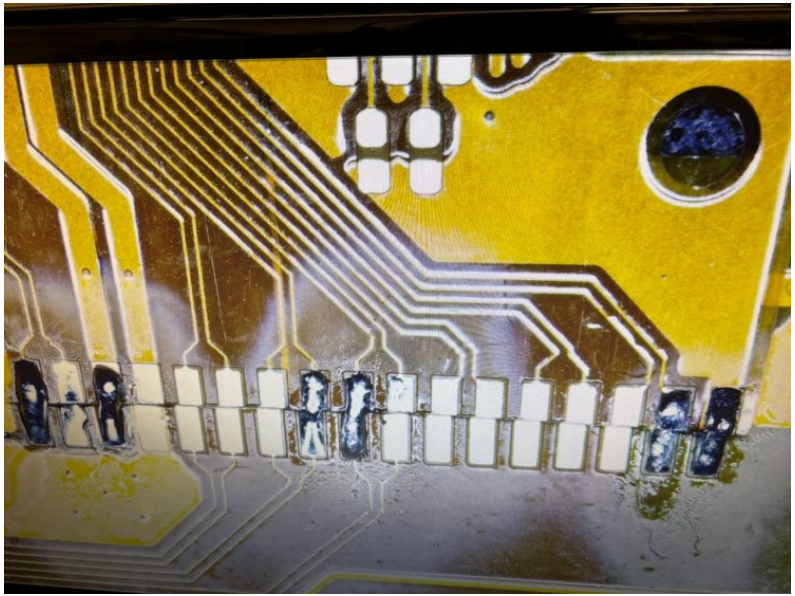




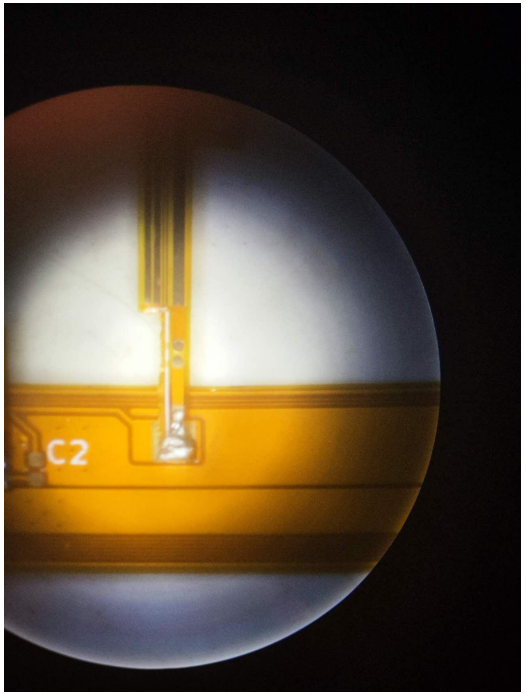




Soldering BFPCs onto MFPC

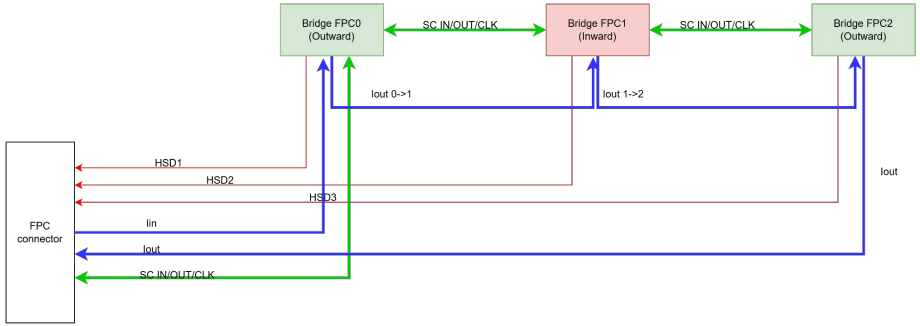


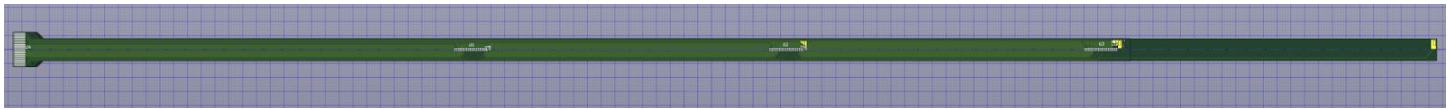
Solder the left BFPC to MFPC: It's doable, but it takes a bit of effort and some cleanup.
Design need to be improved.

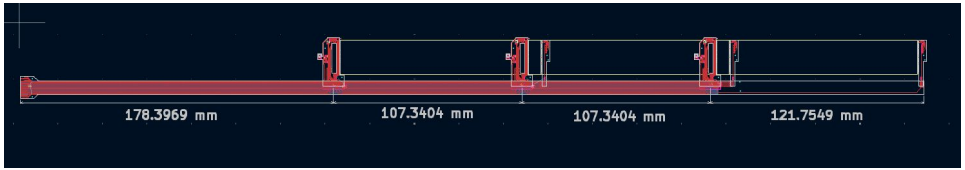


Solder the right BFPC to MFPC: Easy, Stable.

New MFPC v2 Overview



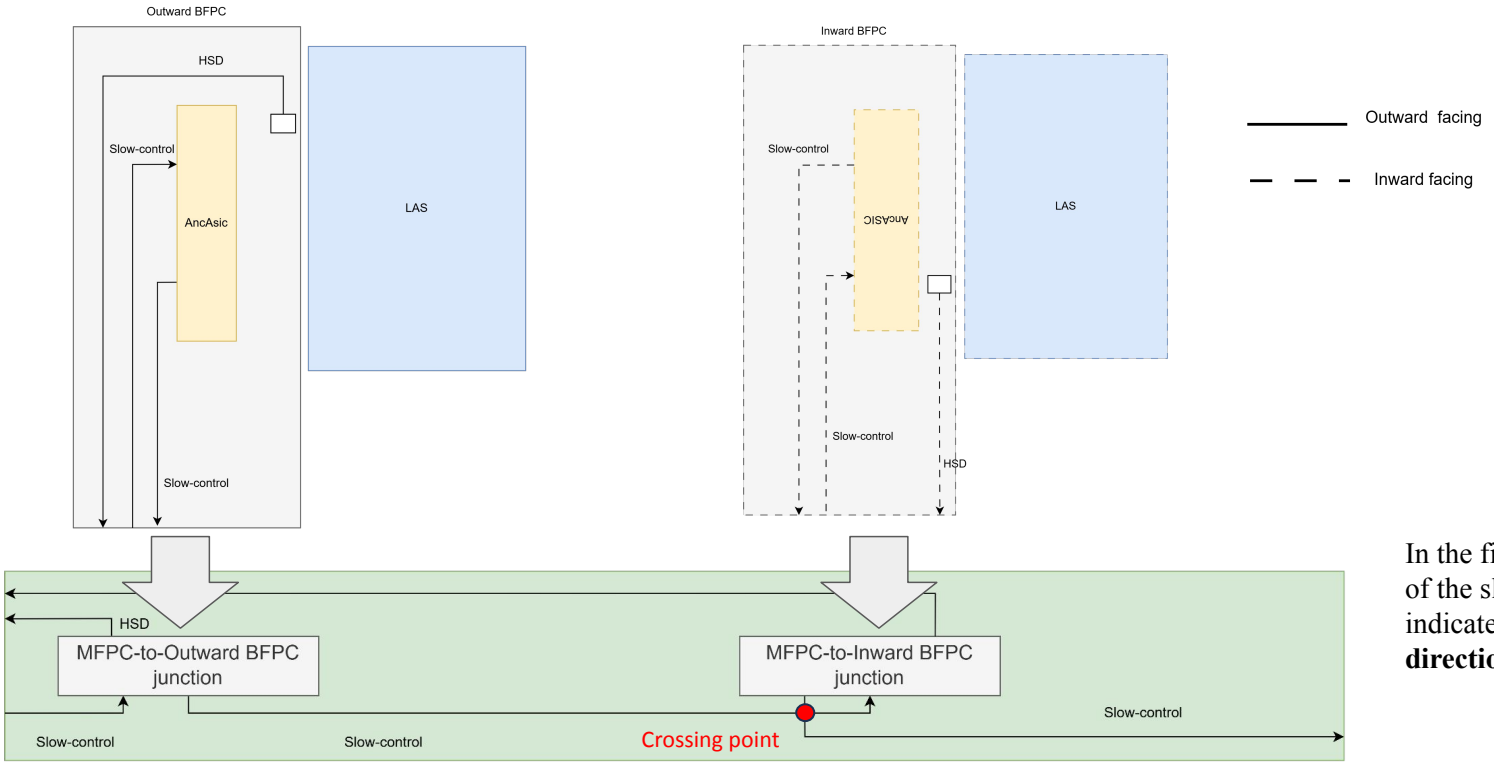




	Area (mm^2)	Trace Area (mm^2)	Power net area (mm^2)	Fill factor
Top Layer	4747.6	221.5	1875.6	0.45
Bottom Layer	4747.6	0 → 3	3202.2 → 3177.5	0.68 → 0.67

Compared to the previous version, the new MFPC has no major changes. Only the connection to BFPC1 was partially modified to accommodate the inward facing module. See page 9 for more details.

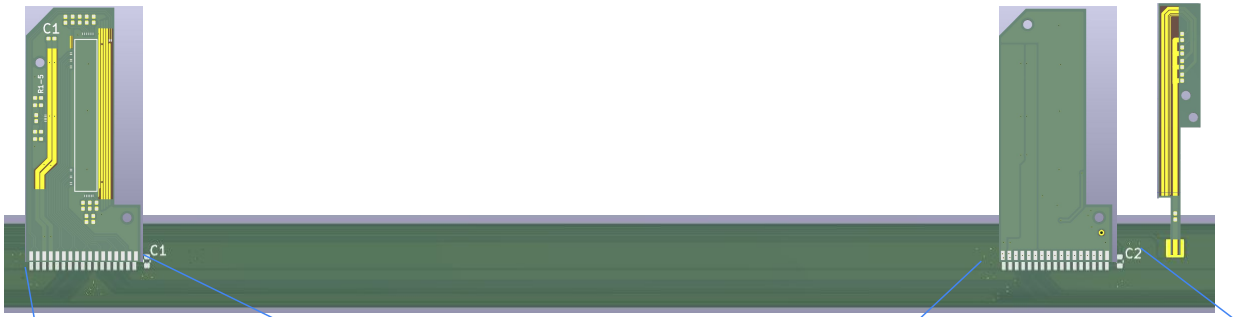
HSD and slow-control connections



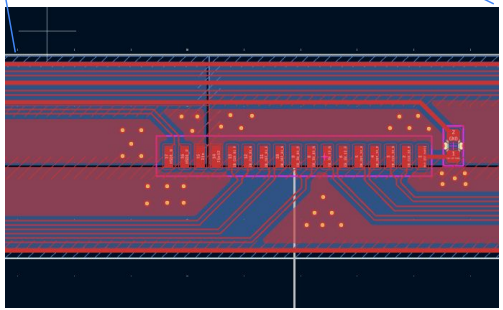
In the figure, the direction of the slow-control arrows indicates the **downlink direction.**

Inward/Outward FPC assembly

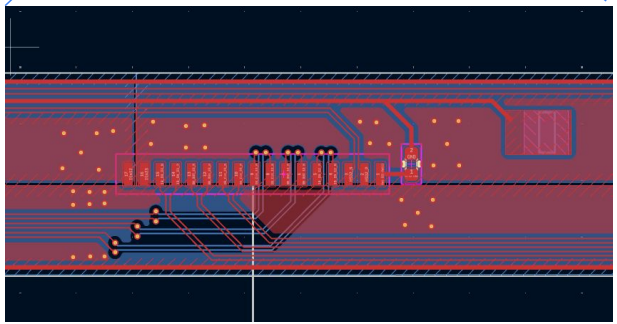
Outward facing module right BFPC



The layout of the solder pads on the Main FPC for the **second** Bridge FPC has been adjusted. To resolve the trace crossing issue, part of the Iout net width on the MFPC was sacrificed.
As a result, the power consumption of Iin/Iout on the Main FPC is expected to increase slightly compared to the first version (473 mW → 479 mW).

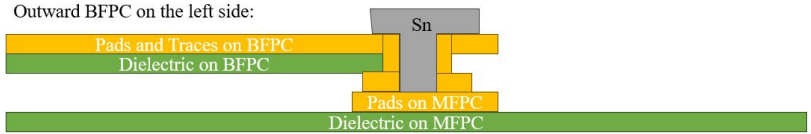


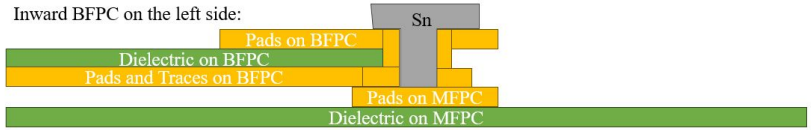
Outward facing module left BFPC

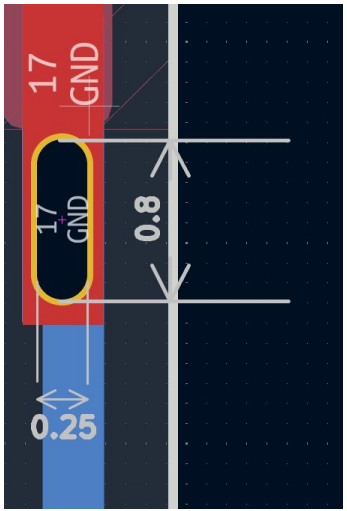


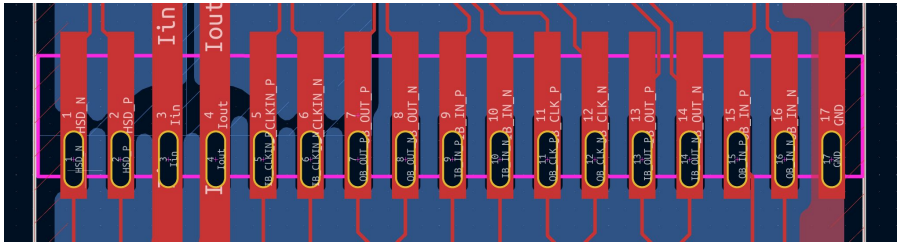
Inward facing module left BFPC

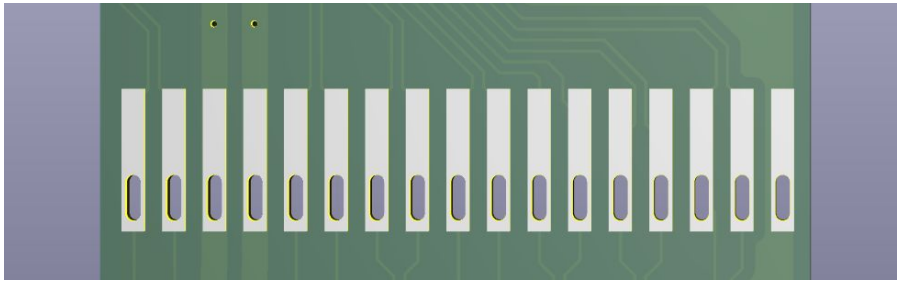
BFPC-to-MFPC Interconnection: Through-hole





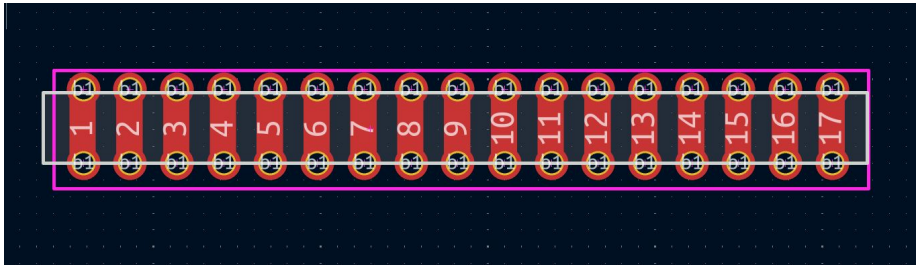


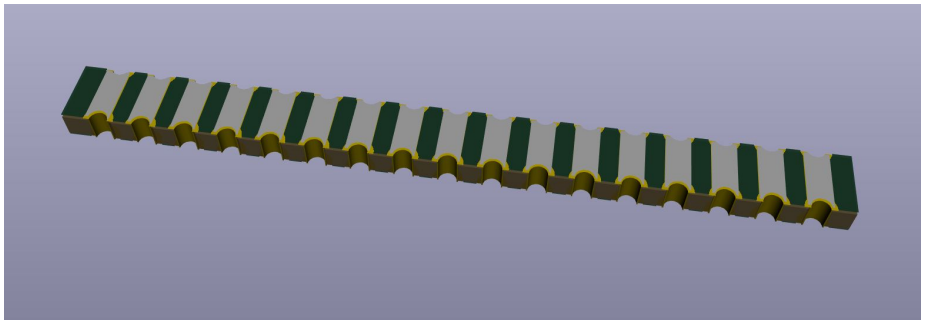


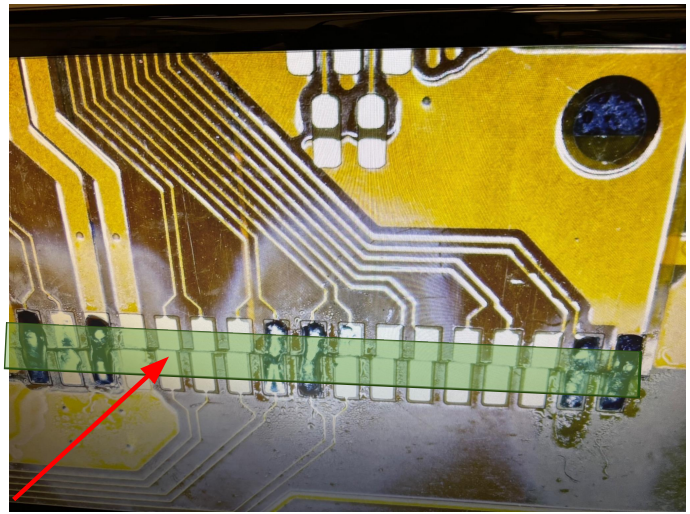


Another method to assemble the BFPC to the Main FPC is through oblong-shaped through-holes, as shown in the figure. The through-hole has a length of 0.8 mm and a width of 0.25 mm, and the soldering pads on the BFPC have been extended to a length of 2.5 mm.

BFPC-to-MFPC Interconnection: Bridge PCB







Bridge PCB

A Bridge PCB with **castellated holes** could be helpful.

Considerations based on ITS3 FPCs and Carrier Board

There are several differences between the current FPC design and ITS3 FPCs and carrier card:

- **Reference ground for HSD**: On the ITS3 FPCs and sensor carrier board, the HSD reference ground is isolated from the rest of the ground planes.
- **Independent power/ground planes**: Each power domain on the ITS3 FPCs and sensor carrier board has its own dedicated power and ground planes. This is achieved using a 3x2-layer FPCs or 12-layer PCB stack-up, which is not feasible to replicate on our 2-layer FPC.
- **Coupling capacitors**: The sensor carrier board includes coupling capacitors between the HSD/slow control lines on the board and the sensor (the slow control path uses 0-Ω resistors as placeholders).

Question to be addressed through system test: To what extent do we have to adopt similar ground and coupling strategy as ITS3

Antoine Junique (CERN) on ITS3 FPCs at TWEPP 2025 link

Summary & Outlook

Summary

- **Cu-based FPC prototypes were designed and produced to check FPC dimensions and inter-connections, with the main goal to facilitate disk module development**
  - Dummy EIC-LAS and AncASIC (UK) and FPCs mounted on CF flat sheet
- **Wire-bonding between the FPC and dummy chips**
  - Both chip-to-power-bus bonding and chip-to-chip wire bonding were verified as feasible.
  - To make the wire bonding easier, recommendation: adjust the chip positions and pad assignments to have straight wire bonds, and extend the right BFPC.
- **Updated version of the FPC design is largely complete.**
  - Designed the BFPCs for inward-facing modules.
  - Connected the decoupling capacitors to the power buses.
  - Extended the power buses on the right BFPC.
  - Discussion with chip designers on-going.
- **Two approaches will be explored to improve BFPC-to-MFPC soldering.**
  - Through-holes on the BFPC and/or bridge PCB

Outlook

- Design testing boards for the new FPCs to test signal transmission quality, power consumption, and measure characteristic impedance.
- FPC simulation in Ansys.

Material Budgets

	Size (mm²)	X_0(%) Al-based	X_0(%) Cu-based
MFPC	4747.6	0.049	0.122
BFPC on the left side	289.7	0.055	0.152
BFPC on the right side	83.1	0.037	0.063

Normalized by the EIC-LAS active area, the material budget (X_0) contribution to a SVT disk by the FPCs will be 0.044% Al vs 0.11% Cu.

Stiffener

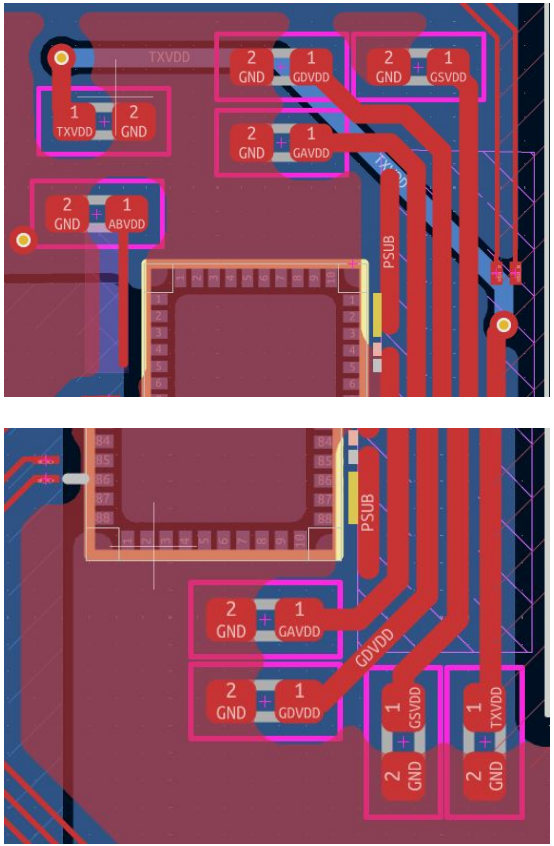
With stiffener

Without stiffener

JLC suggested the FPC designer place a stiffer beneath the device that needs to be soldered.

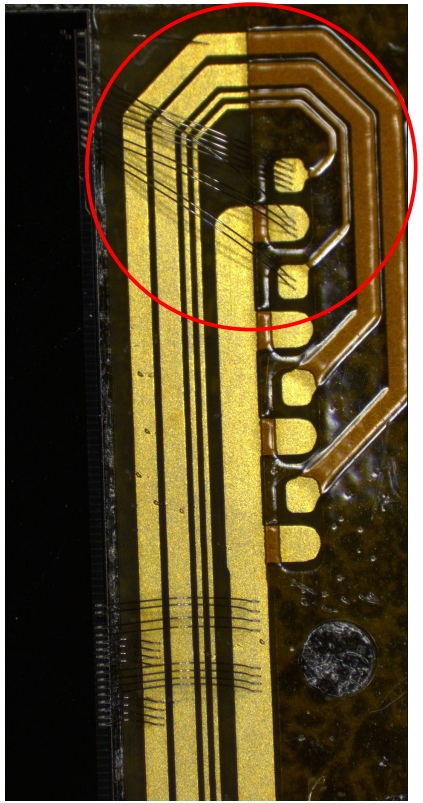
Both capacitors were successfully soldered with no significant difference observed. Therefore, it can be concluded that:
The stiffener is not necessary.

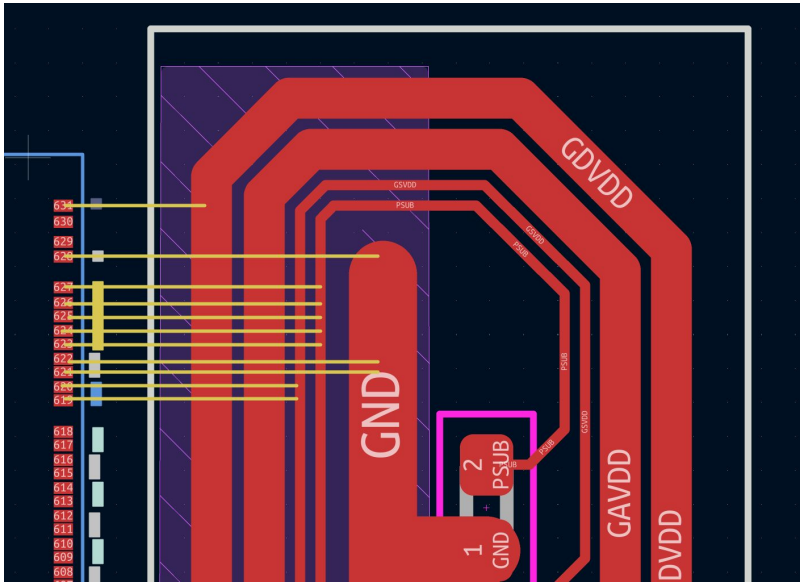
Decoupling capacitors on the left BFPC



Following the suggestion from AncASIC designer, the power buses on the left BFPC are connected to the decoupling capacitor now.
We are still discussing whether the pads on the top/bottom edge of the AncASIC can be left floating. If so, the capacitors can be placed closer to the chip.

Extended the power buses on the right BFPC





Wire bonding diagram for the new right BFPC

To allow the pads on the right side of the LAS to be straight-bonded to the power buses, the length of the right-side BFPC was extended by approximately 0.96 mm.

Material budget estimated

MFPC:
4747.6mm2

Layer	Material	Thickness [um]	X0 [cm]	Fraction	X0(%)
Soldermask	Not sure	30	28.6	1	0.01044802
Aluminum	Aluminum	15	8.9	0.45	0.00758683
Dielectric	Polyamide	45	28.6	1	0.01575079
Aluminum	Aluminum	15	8.9	0.67	0.01129594
soldermask	Polyamide	10	28.6	1	0.00348267
Total		115			0.04856425

BFPC:
289.7mm2
+

Layer	Material	Thickness [um]	X0 [cm]	Fraction	X0(%)
Soldermask + Glue	Not sure	30	28.6	1	0.01044802
Aluminum	Aluminum	15	8.9	0.91	0.01534225
Dielectric	Polymid	45	28.6	1	0.01575079
Aluminum	Aluminum	15	8.9	0.58	0.00977858
soldermask	Polymid	10	28.6	1	0.00348267
		115			0.05480231

Material budget estimated

BFPC_right:
83.1 mm2

Layer	Material	Thickness [um]	X0 [cm]	Fraction	X0(%)
Soldermask	Not sure	30	28.6	1	0.01048951
Aluminum	Aluminum	15	8.9	0.019	0.000320225
Dielectric	Polyamide	45	28.6	1	0.015734266
Aluminum	Aluminum	15	8.9	0.4	0.006741573
soldermask	Polyamide	10	28.6	1	0.003496503
Total		115			0.036782077

Material budget estimated

MFPC:
4747.6mm2

Layer	Material	Thickness [um]	X0 [cm]	Fraction	X0(%)
Soldermask	Not sure	27.5	28.6	1	0.009615385
Aluminum	Aluminum	12	8.9	0.45	0.037604457
Dielectric	Polyamide	25	28.6	1	0.008741259
Aluminum	Aluminum	12	8.9	0.67	0.055988858
soldermask	Polyamide	27.5	28.6	1	0.009615385
Total		104			0.121565343

BFPC:
289.7mm2
+

Layer	Material	Thickness [um]	X0 [cm]	Fraction	X0(%)
Soldermask + Glue	Not sure	27.5	28.6	1	0.009615385
Aluminum	Aluminum	12	8.9	0.91	0.076044568
Dielectric	Polymid	25	28.6	1	0.008741259
Aluminum	Aluminum	12	8.9	0.58	0.048467967
soldermask	Polymid	27.5	28.6	1	0.009615385
		104			0.152484563

Material budget estimated

BFPC_right:
83.1 mm2

Layer	Material	Thickness [um]	X0 [cm]	Fraction	X0(%)
Soldermask	Not sure	27.5	28.6	1	0.009615385
Aluminum	Aluminum	12	8.9	0.019	0.001587744
Dielectric	Polyamide	25	28.6	1	0.008741259
Aluminum	Aluminum	12	8.9	0.4	0.033426184
soldermask	Polyamide	27.5	28.6	1	0.009615385
Total		104			0.062985956