HRPPD Meeting #25 Update

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U.S. DEPARTMENT of ENERGY

Current Status

Tasks:

- Priority tasks
  - BNL visit
    - Meet Tuesday to get an overview of area?
    - Where to meet other days?
    - Testing is in building 510D, room 201 @ 9AM
    - Don’t forget to complete training!
      - Sean for training

Part status

- Interposer
  - Submitted 7/6, req approved 7/20, waiting PO
- HRPPD order status
  - Ordered 6/17, due 10/21
- Sidewall
  - Ordered 6/17, due ~9/1

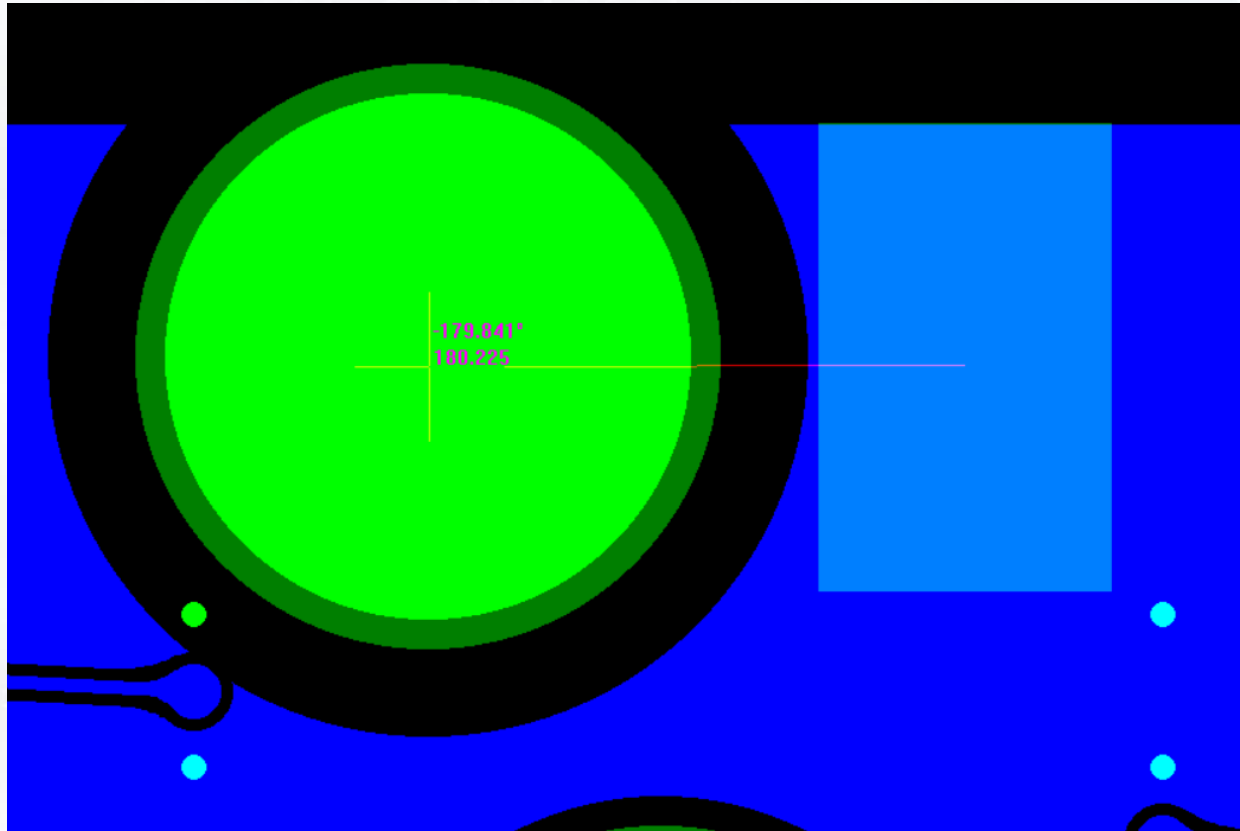
No update

- Open items:
  - N/A
- FCFD Test Board
  - Will resume in July
- Backplane Changes
  - See action item list

Parts for Next Week

- Gerard's LED pulser
- 1210 or 1812 parts will fit on backplane, but might be susceptible to breaking if HV wires move
- Decoupling capacitors
  - Exit MCP to anode capacitance = 44 pF
  - Entry or Exit MCP capacitance = 862 pF
  - Will select 1x, 5x, 10x
- Anti-ringing resistors, if needed
- Can someone overnight these parts to BNL?

Voltage	Max V from 0V
PC	-2500
EnT	-2100
EnB	-1450
ExT	-1250
ExB	-500
GND	0



Appendix

Status Updates

Needed for HRPPDs

- Spacer
  - Thickness selected = 2.8 mm
  - Glue
    - Pull test was performed
    - Is glue finalized, 3M DP460?
  - Helicoils + screws
    - Material: 2-56 stainless steel coil + aluminum screw
      - This will cause corrosion?
    - We previously discussed a screw pull test in the spacer without helicoils to determine if they're even needed
    - Standard length 3/16 or 7/32 should work depending on PCB backplane thickness
- Shims, window
  - Status?
- Interposers
  - MFG drawing provided, req approved, waiting for PO issue
- HV pogo pins
  - Mill-max 0900 SMT pins, readily available for order
- Backplane
  - HV connectors and cables/wiring
  - HV distribution and routing
  - Add MCP bleed and PC current limiting resistors
  - Size bypass caps and anti-ringing resistors
  - How are ASIC cards going to be anchored?
  - Bug fixes – swapped traces

Other priority

- FCFD Testing
  - When, who, and how?
  - Need to settle specifications with hpDIRC team somehow…
  - FNAL starting FCFD Variant v1.2 (analog frontend + digital backend)

Remaining design items

- ASIC card
  - Impedance matching solution – analyzing signal path lengths
    - TBD test on-board terminations
  - Bug fixes – card edge dimensions
  - Maybe preliminary routing can start once FCFDv2 is designed
- Bridge card
  - LV connectors
  - Use a more rugged optical cable for readout rather than included VTRX+ one
- Power distribution
  - Cable lengths from South Platform
  - Account for distribution board. Where located? Tim designed original, will it need to be updated?
- Mechanical (Alex)
  - Preliminary envelope 3D modeled
  - Cooling
  - HRPPD enclosure fit into pfRICH