OAK RIDGE National Laboratory

August 12th, 2026

Insert Rates

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U.S. DEPARTMENT of ENERGY

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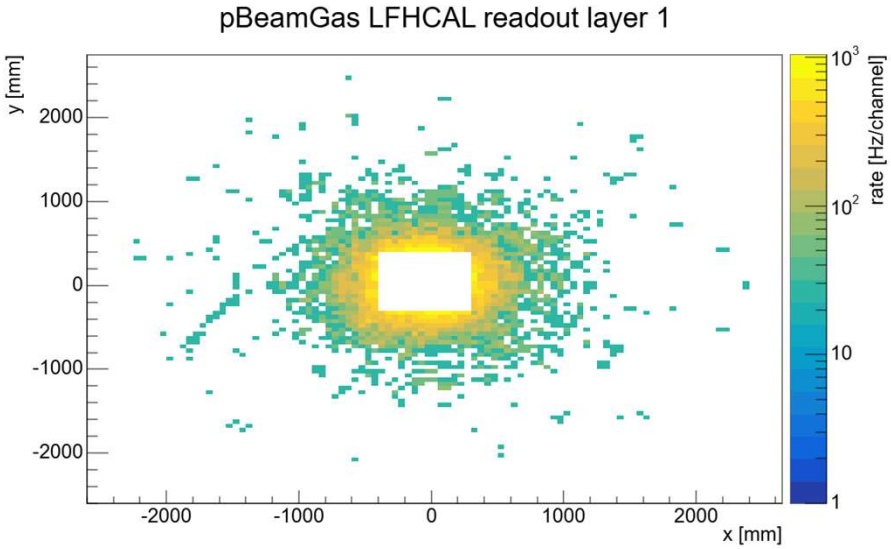
Primary Data Source

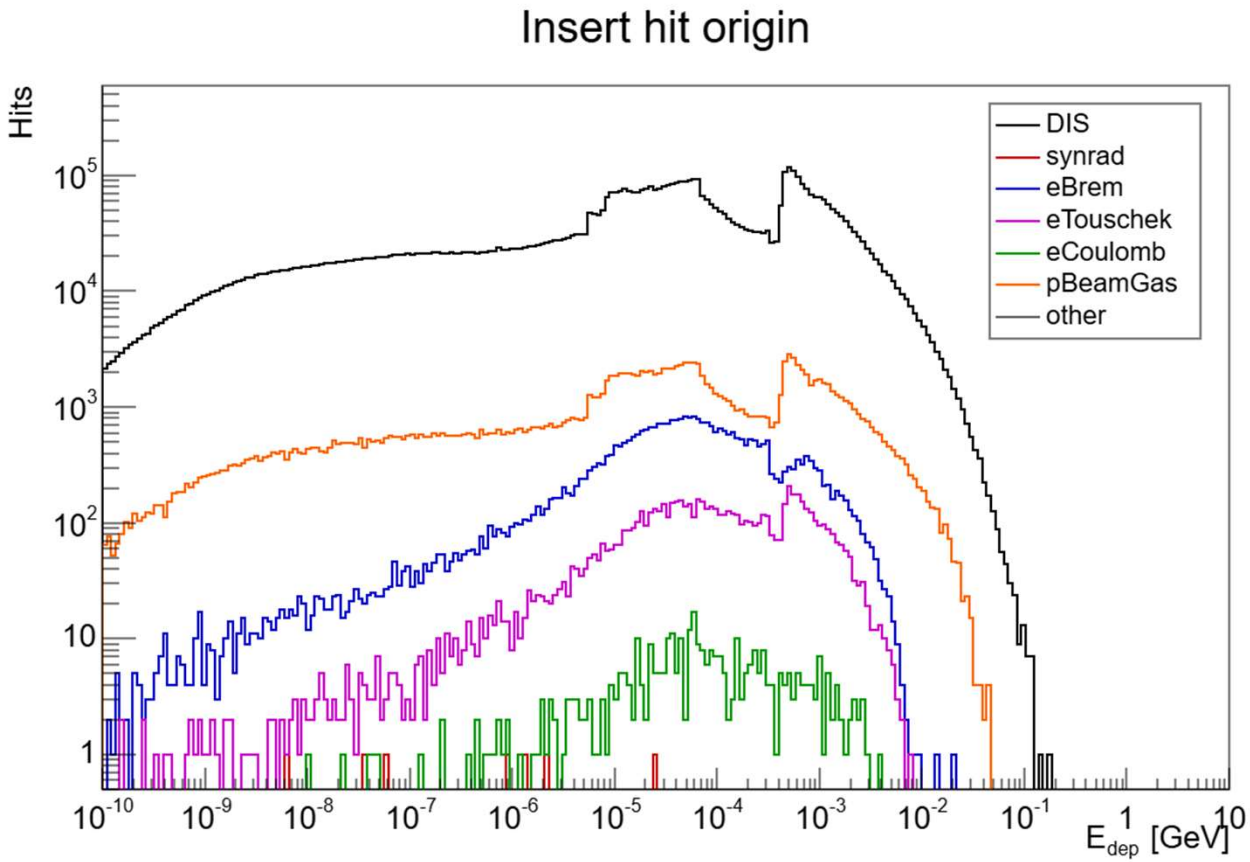
July full background simulation data: NC, DIS, 10x275 GeV, $Q^2 > 1$ GeV^2:

- epic:/FULL/26.07.1/epic_craterlake/Bkg_Exact1S_2us/GoldCt/10um/DIS/NC/10x275/minQ2=1/pythia8NCDIS_10x275_minQ2=1_beamEffects_xAngle=-0.025_hiDiv_1.0000.edm4hep.root

Used the first 200 files, approximately 19k events.



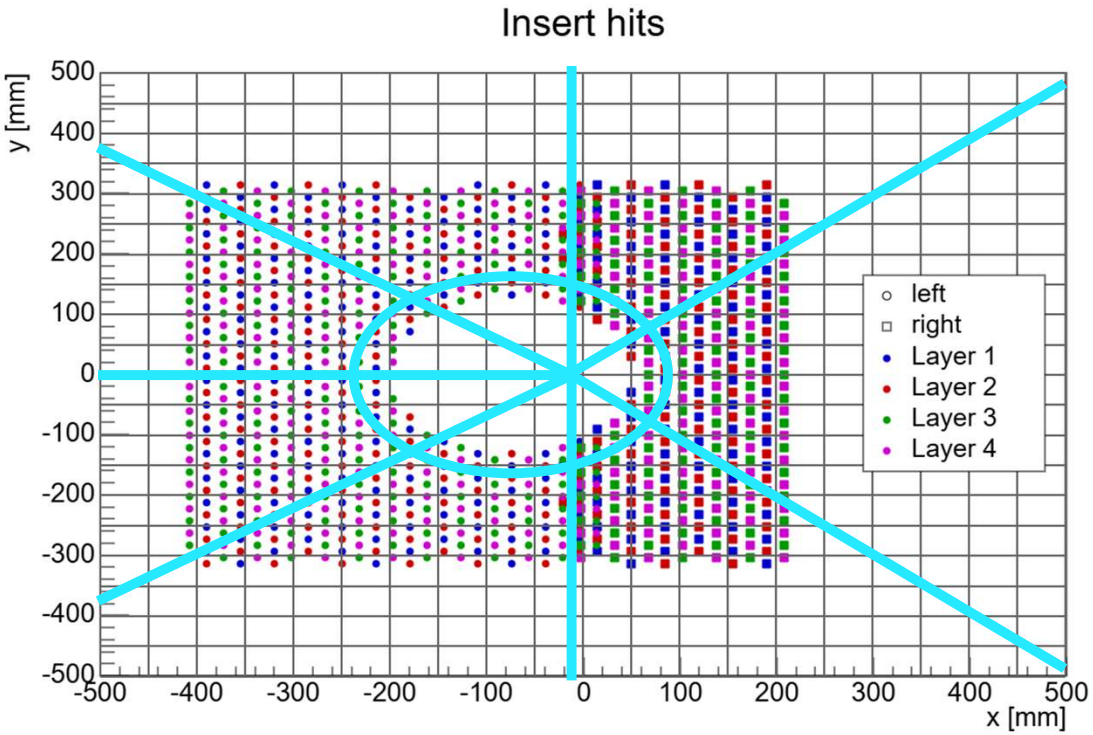
Background composition



The Insert Calorimeter

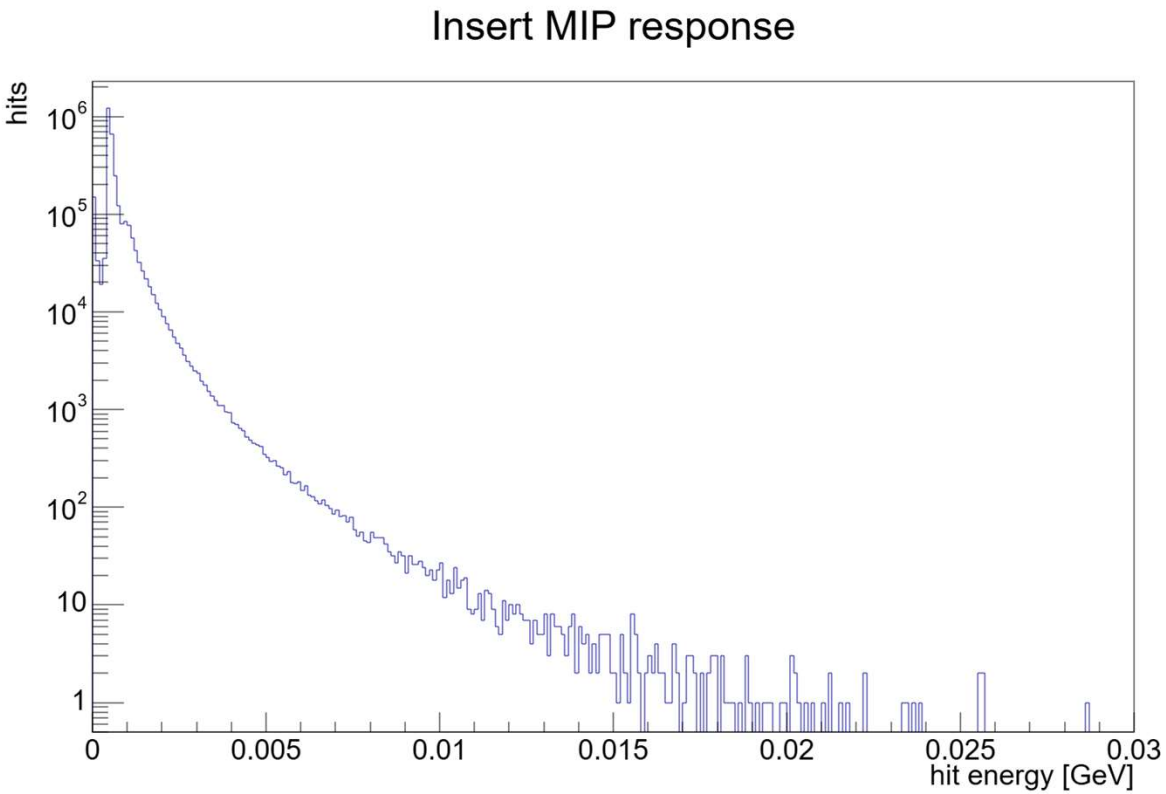
- 60 layers of hexagonal tiles
  - 3 different tile sizes depending on layer
- Each layer is offset from the previous layer
  - Offset pattern repeats every 4 layers
- 2 sides
  - Left side has more tiles than right side

- Alternative designs and data rate estimates?
  - LFHCal-sized tiles
  - Full LFHCal-style readout (includes longitudinal summing)
  - With/without inner radius of channels



Threshold model

- MIP peak for an Insert tile is approximately 4e-4 GeV.
- Thresholds for channels made of one tile = 0.1×MIP, 0.2×MIP, etc.
- Thresholds for channels made of N tiles = 0.1×N×MIP, 0.2×N×MIP, etc.



Rate definitions

For a channel

A channel is counted as fired when its summed hit energy in an event exceeds its MIP-based threshold.

Rate:

$$\frac{\text{Channel fire count}}{\text{Total events} \times 2 \text{ microseconds}}$$

For a readout chip

A chip is counted as fired when any channel on that chip fires in that event.

Rate:

$$\frac{\text{Chip fire count}}{\text{Total events} \times 2 \text{ microseconds}}$$

Data model

For individual channels

- Data per event = (32 bits per channel) × 4 samples if a channel fires

For chips with multiple channels

- Data per event = [128 bits + 32 bits × (number of fired channels)] × 4 samples

Version 1: Insert tiles (with/without inner ring)

HCalEndcapPInsertHits

hit.getPosition() + decode cell ID

Use the physical layer number with that transverse bin to define the tile-channel ID (layer, x, y)

Skip/keep a channel depending on its distance from beampipe

Original insert with/without inner ring

Per-channel and per-chip rate tails (p95/p99) and total side data rates, with the inner ring (top) and without the inner ring (bottom).

	Channel p95	Channel p99	Chip p95	Chip p99	Left	Right
0.1 MIP	19.0 kHz 0.0024 Gb/s	27.7 kHz 0.0035 Gb/s	171 kHz 0.14 Gb/s	189 kHz 0.15 Gb/s	20.1 Gb/s	11.1 Gb/s
0.5 MIP	13.2 kHz 0.0017 Gb/s	20.2 kHz 0.0026 Gb/s	129 kHz 0.098 Gb/s	147 kHz 0.11 Gb/s	13.8 Gb/s	7.28 Gb/s
1.5 MIP	8.36 kHz 0.0011 Gb/s	13.4 kHz 0.0017 Gb/s	91.1 kHz 0.068 Gb/s	103 kHz 0.076 Gb/s	9.20 Gb/s	4.72 Gb/s

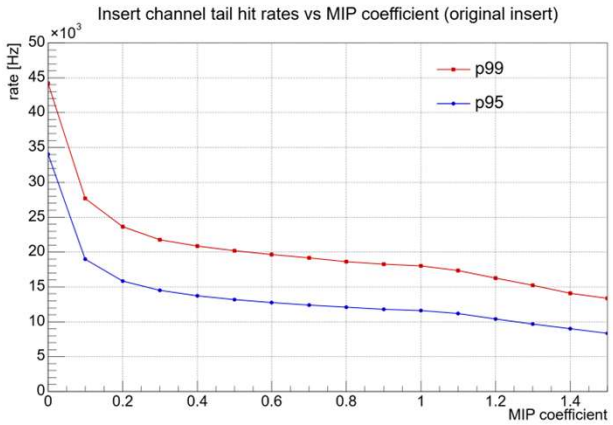
	Channel p95	Channel p99	Chip p95	Chip p99	Left	Right
0.1 MIP	17.5 kHz 0.0022 Gb/s	26.7 kHz 0.0034 Gb/s	149 kHz 0.12 Gb/s	165 kHz 0.13 Gb/s	18.3 Gb/s	8.78 Gb/s
0.5 MIP	11.7 kHz 0.0015 Gb/s	18.9 kHz 0.0024 Gb/s	110 kHz 0.083 Gb/s	125 kHz 0.093 Gb/s	12.3 Gb/s	5.41 Gb/s
1.5 MIP	7.55 kHz 0.00097 Gb/s	12.6 kHz 0.0016 Gb/s	76.3 kHz 0.055 Gb/s	87.2 kHz 0.063 Gb/s	8.22 Gb/s	3.51 Gb/s

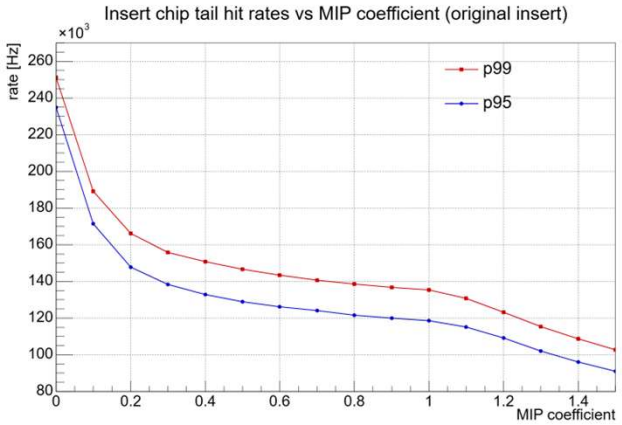
Various rates vs MIP (with inner ring)

Channel

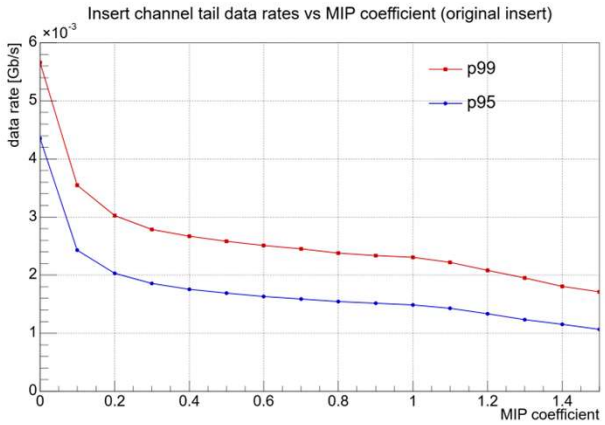
Chip

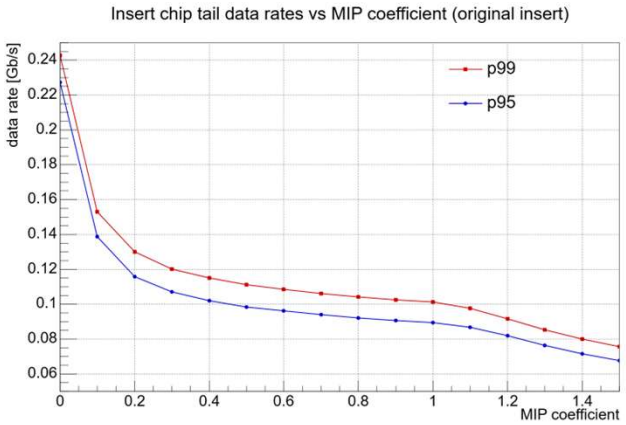
Hit Rate





Data rate



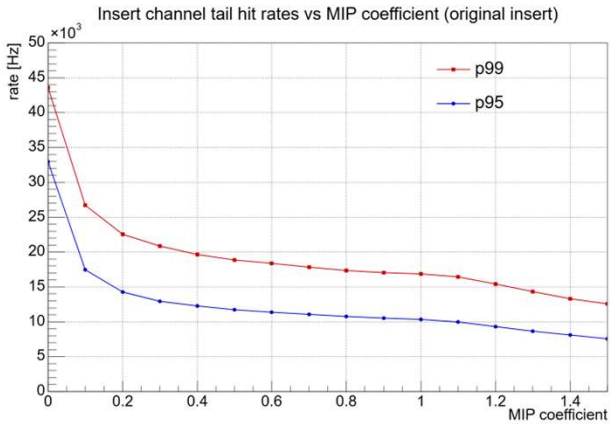


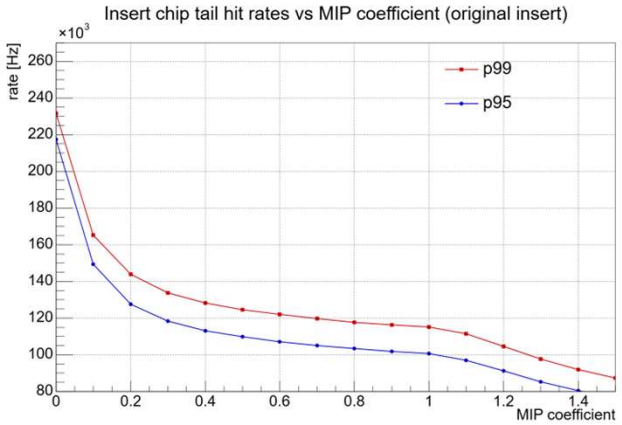
Various rates vs MIP (without inner ring)

Channel

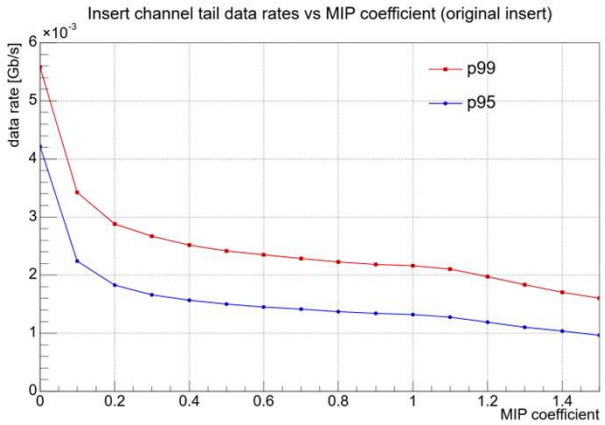
Chip

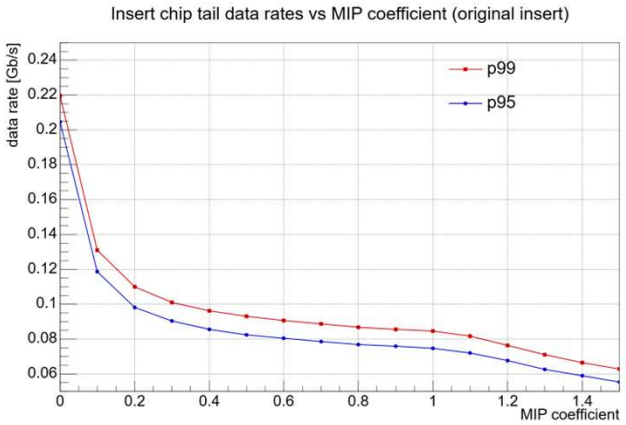
Hit Rate





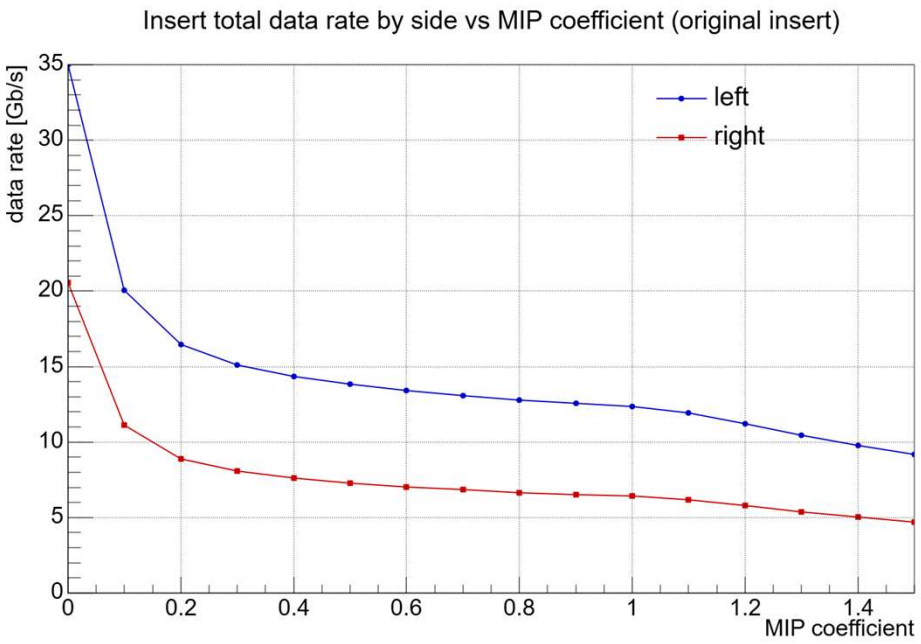
Data rate



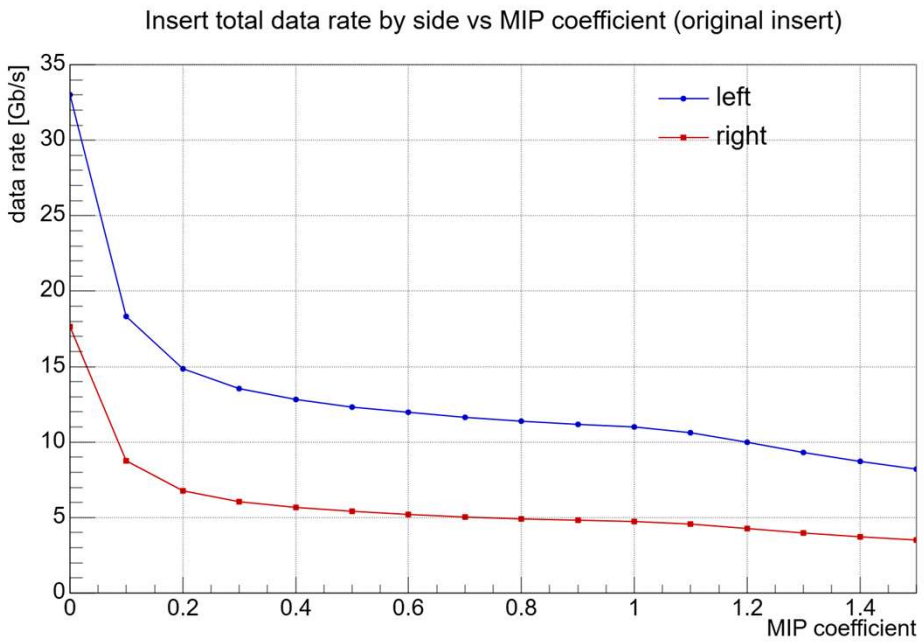


Side data rates with/without inner ring vs MIP

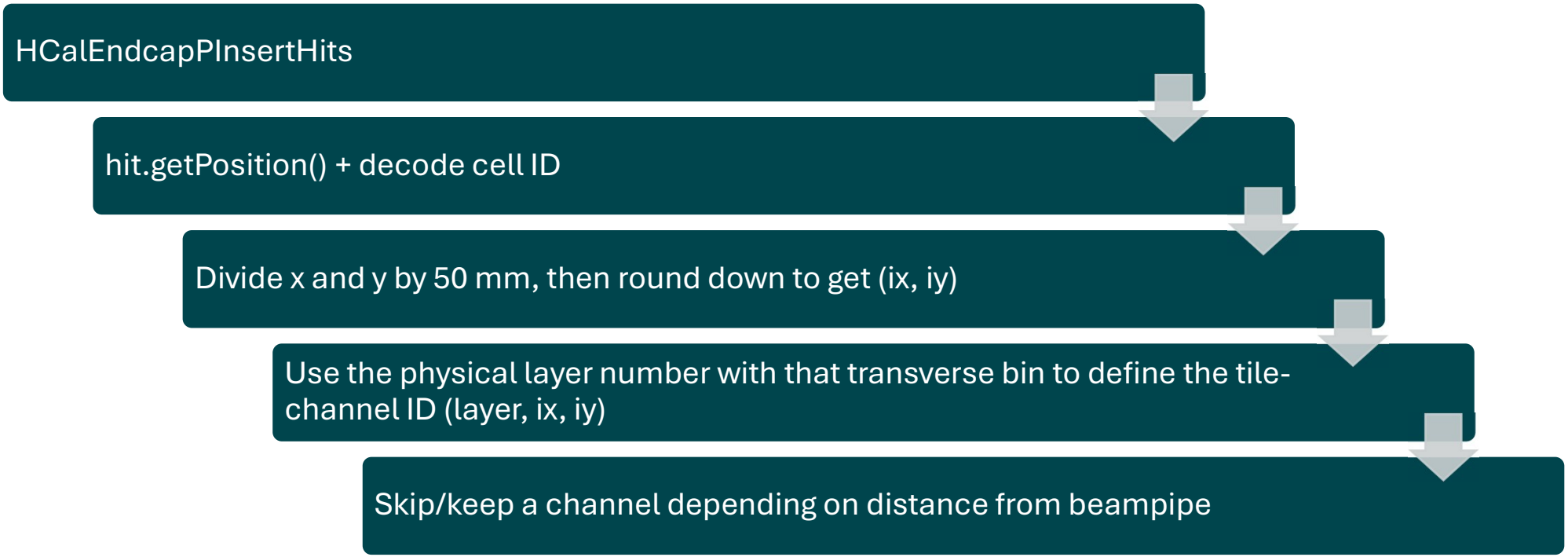
With inner ring



Without inner ring



Version 2: LFHCal-sized tiles (with/without inner ring)



LFHCal tiles with/without inner ring

Per-channel and per-chip rate tails (p95/p99) and total side data rates, with the inner ring (top) and without the inner ring (bottom) for LFHCal sized tiles.

	Channel p95	Channel p99	Chip p95	Chip p99	Left	Right
0.1 MIP	23.9 kHz 0.0031 Gb/s	38.4 kHz 0.0049 Gb/s	174 kHz 0.14 Gb/s	188 kHz 0.15 Gb/s	19.9 Gb/s	11.0 Gb/s
0.5 MIP	16.1 kHz 0.0021 Gb/s	26.8 kHz 0.0034 Gb/s	133 kHz 0.099 Gb/s	147 kHz 0.11 Gb/s	13.7 Gb/s	7.24 Gb/s
1.5 MIP	10.3 kHz 0.0013 Gb/s	18.2 kHz 0.0023 Gb/s	94.4 kHz 0.068 Gb/s	107 kHz 0.076 Gb/s	9.20 Gb/s	4.71 Gb/s

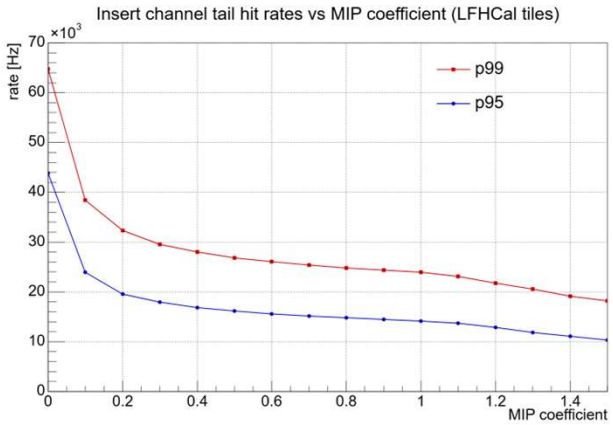
	Channel p95	Channel p99	Chip p95	Chip p99	Left	Right
0.1 MIP	21.6 kHz 0.0028 Gb/s	35.3 kHz 0.0045 Gb/s	152 kHz 0.12 Gb/s	174 kHz 0.13 Gb/s	17.7 Gb/s	8.21 Gb/s
0.5 MIP	14.4 kHz 0.0018 Gb/s	23.8 kHz 0.0030 Gb/s	110 kHz 0.079 Gb/s	130 kHz 0.095 Gb/s	11.9 Gb/s	5.04 Gb/s
1.5 MIP	9.29 kHz 0.0012 Gb/s	15.7 kHz 0.0020 Gb/s	76.6 kHz 0.054 Gb/s	90.9 kHz 0.065 Gb/s	7.93 Gb/s	3.28 Gb/s

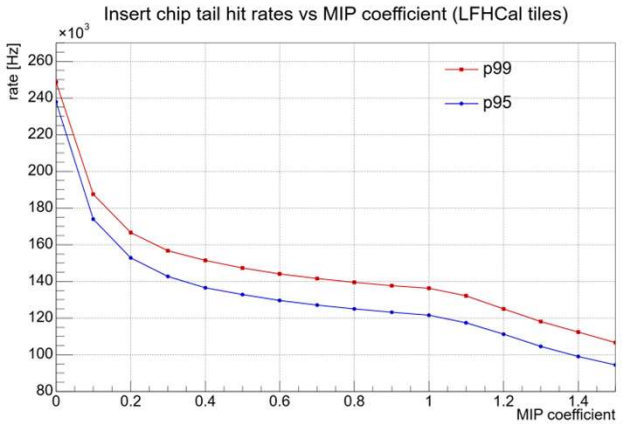
Various rates vs MIP (with inner ring)

Channel

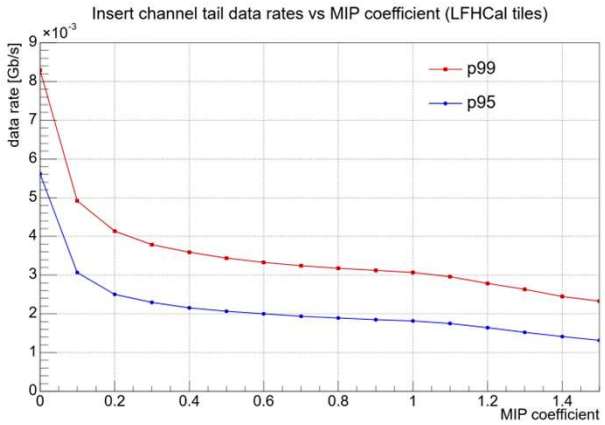
Chip

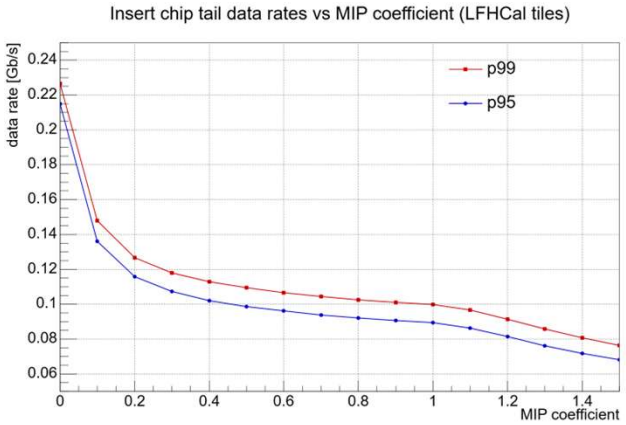
Hit Rate





Data rate



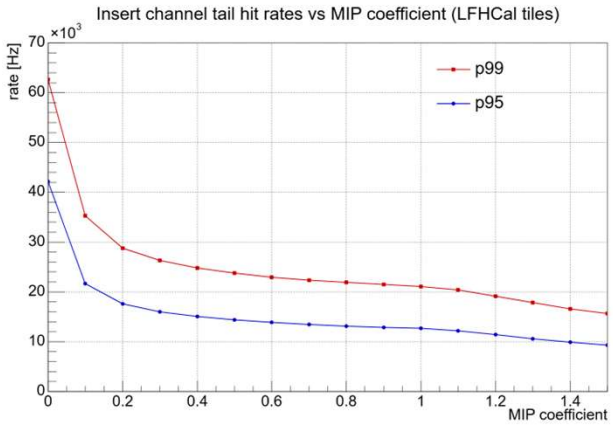


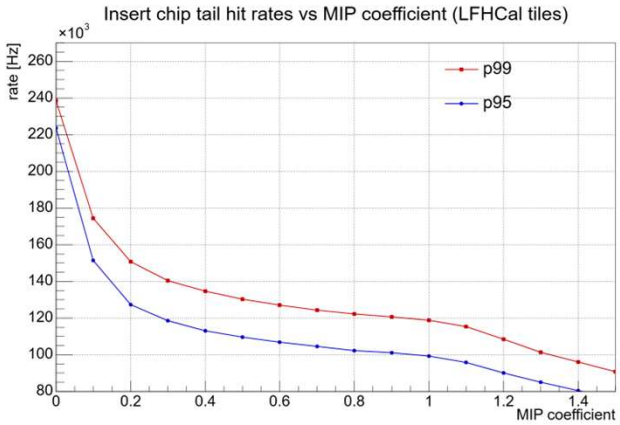
Various rates vs MIP (without inner ring)

Channel

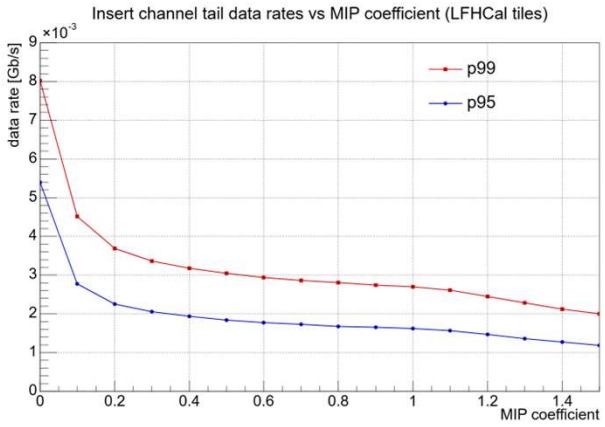
Chip

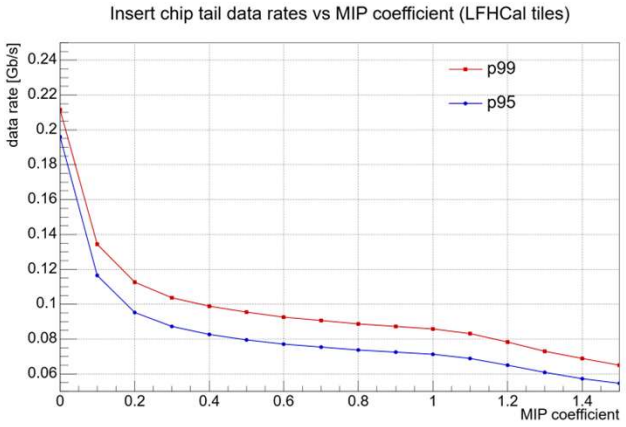
Hit Rate





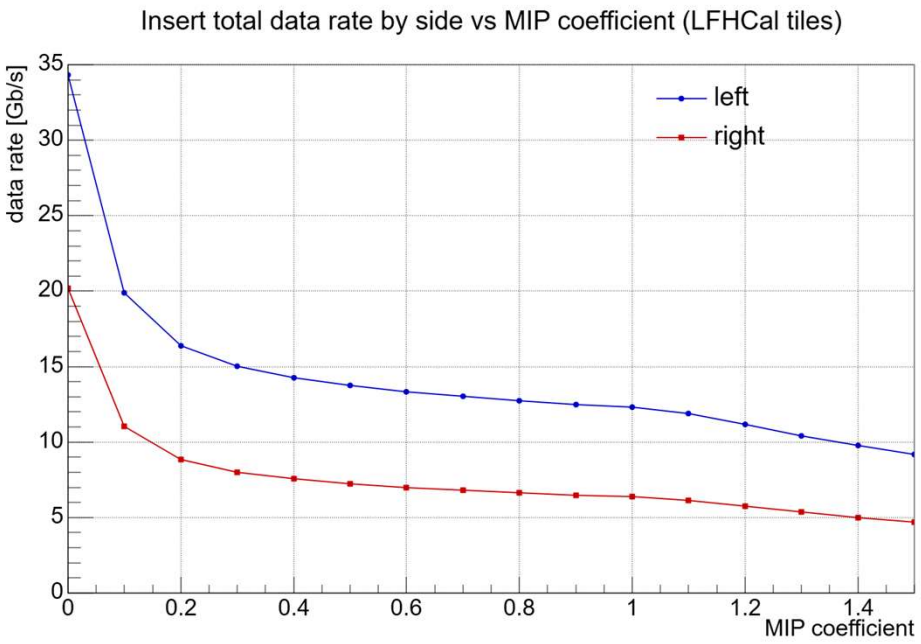
Data rate



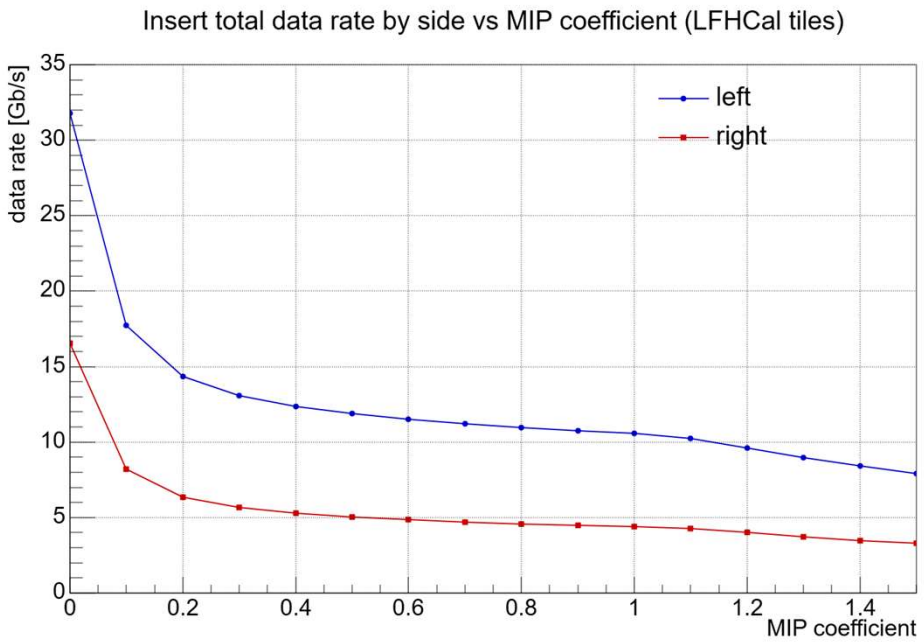


Side data rates with/without inner ring vs MIP

With inner ring



Without inner ring



Version 3: Full LFHCal readout format

Longitudinal segmentation

- Layer values from 1 to 5 get grouped into one segment, then 6–10, and 11–20, 21–30, 31–40, 41–50, 51–60
- 7 virtually segmented readout layers

Channel segmentation

1. HCalEndcapPInsertHits
2. hit.getPosition()
3. Map the hit layer into a readout segment
4. Divide x and y by 50 mm, then round down to get (ix, iy)
5. Hits in the same readout segment and same 50 mm × 50 mm transverse bin share the same virtual channel
6. Define a virtual channel ID as (segment, ix, iy)

Chip segmentation

1. Virtual channel ID: (ix, iy)
2. Compute virtual chip ID as (ix / 2, iy / 2) with integer division
3. This merges each 2 × 2 block of virtual channels into one virtual chip
    - Example: (0,0), (0,1), (1,0), (1,1) all map to chip (0,0)
4. Repeat for all virtual channels

Full LFHCal readout with/without inner ring

Per-channel and per-chip rate tails (p95/p99) and total side data rates, with the inner ring (top) and without the inner ring (bottom) with the full LFHCal readout scheme.

	Channel p95	Channel p99	Chip p95	Chip p99	Left	Right
0.1 MIP	61.9 kHz 0.0079 Gb/s	78.5 kHz 0.010 Gb/s	286 kHz 0.30 Gb/s	300 kHz 0.33 Gb/s	4.37 Gb/s	2.46 Gb/s
0.5 MIP	29.8 kHz 0.0038 Gb/s	45.7 kHz 0.0059 Gb/s	179 kHz 0.15 Gb/s	199 kHz 0.19 Gb/s	2.23 Gb/s	1.19 Gb/s
1.5 MIP	11.8 kHz 0.0015 Gb/s	21.7 kHz 0.0028 Gb/s	83.3 kHz 0.066 Gb/s	106 kHz 0.091 Gb/s	0.949 Gb/s	0.454 Gb/s

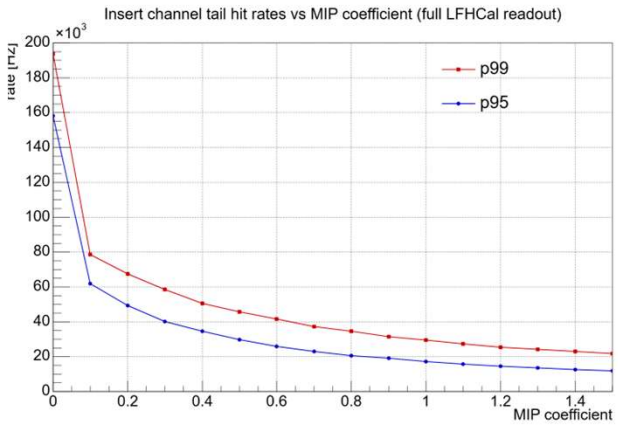
	Channel p95	Channel p99	Chip p95	Chip p99	Left	Right
0.1 MIP	56.7 kHz 0.0073 Gb/s	75.6 kHz 0.0097 Gb/s	265 kHz 0.25 Gb/s	270 kHz 0.25 Gb/s	3.83 Gb/s	1.91 Gb/s
0.5 MIP	27.1 kHz 0.0035 Gb/s	41.3 kHz 0.0053 Gb/s	158 kHz 0.13 Gb/s	162 kHz 0.14 Gb/s	1.97 Gb/s	0.920 Gb/s
1.5 MIP	9.87 kHz 0.0013 Gb/s	17.4 kHz 0.0022 Gb/s	76.4 kHz 0.059 Gb/s	82.2 kHz 0.065 Gb/s	0.838 Gb/s	0.354 Gb/s

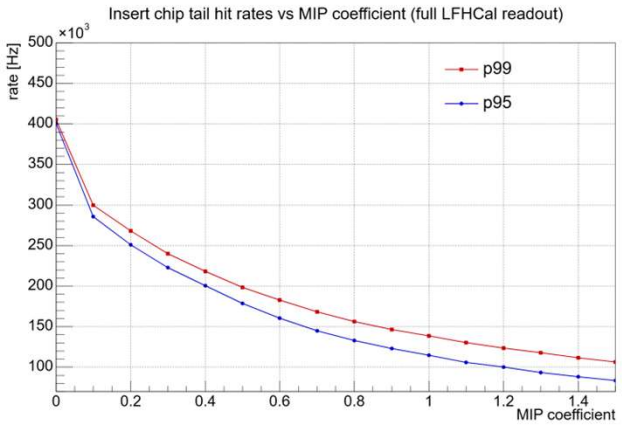
Various rates vs MIP (with inner ring)

Channel

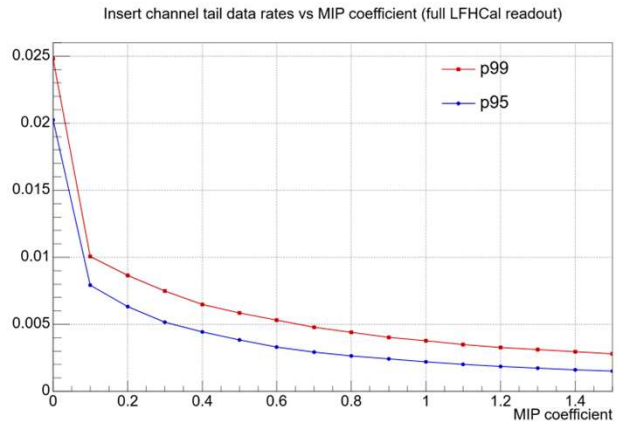
Chip

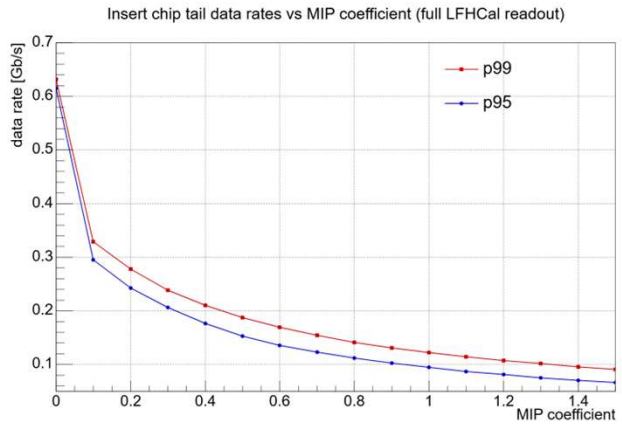
Hit Rate





Data rate



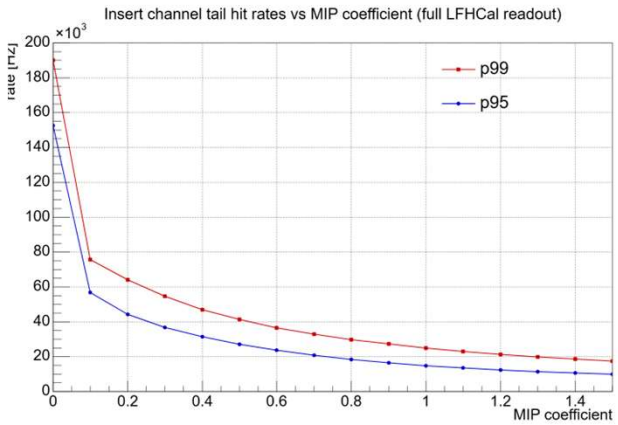


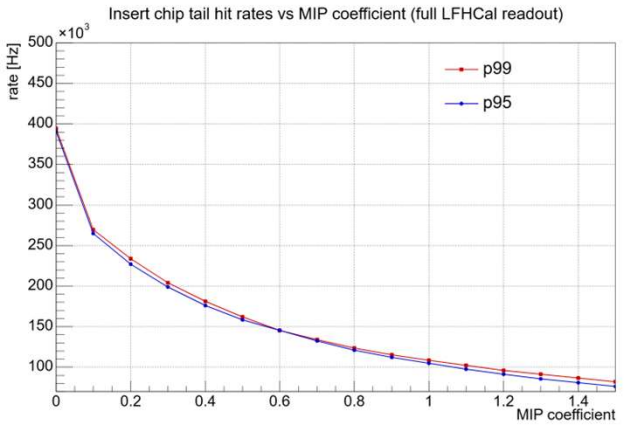
Various rates vs MIP (without inner ring)

Channel

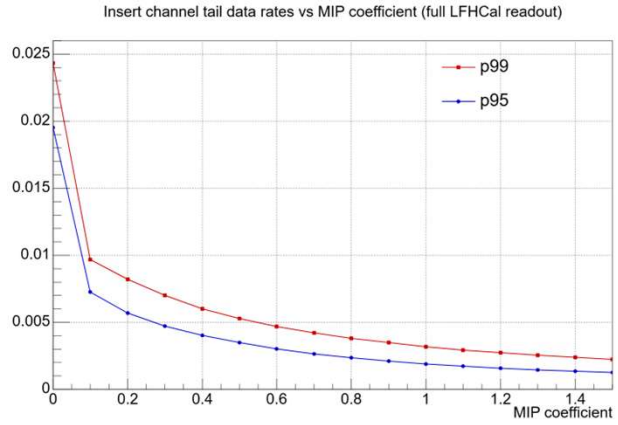
Chip

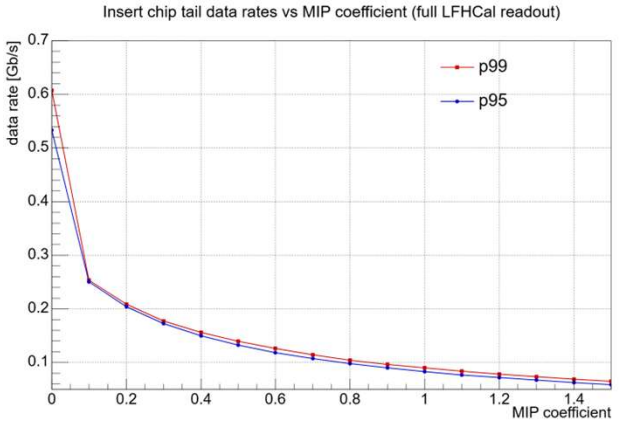
Hit Rate





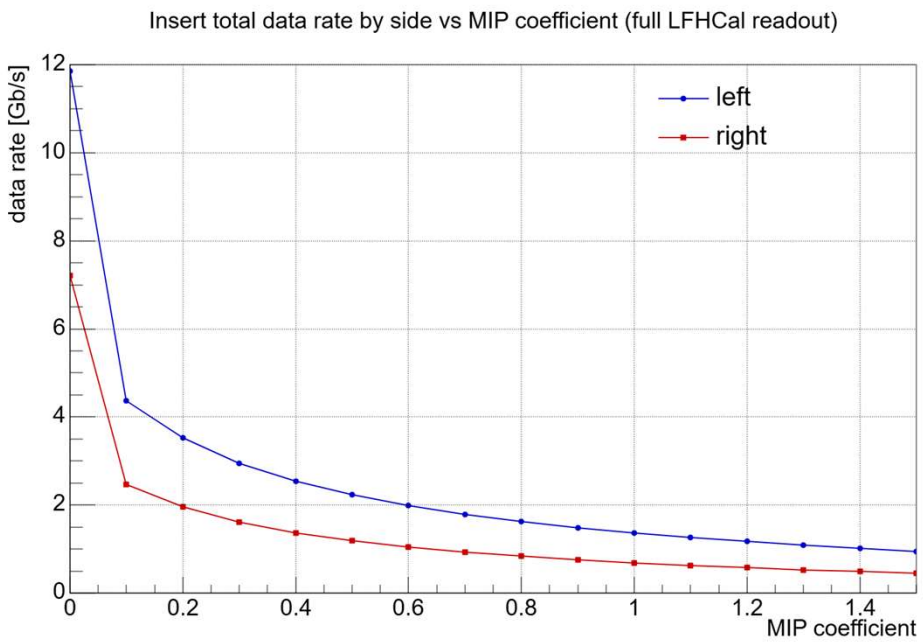
Data rate



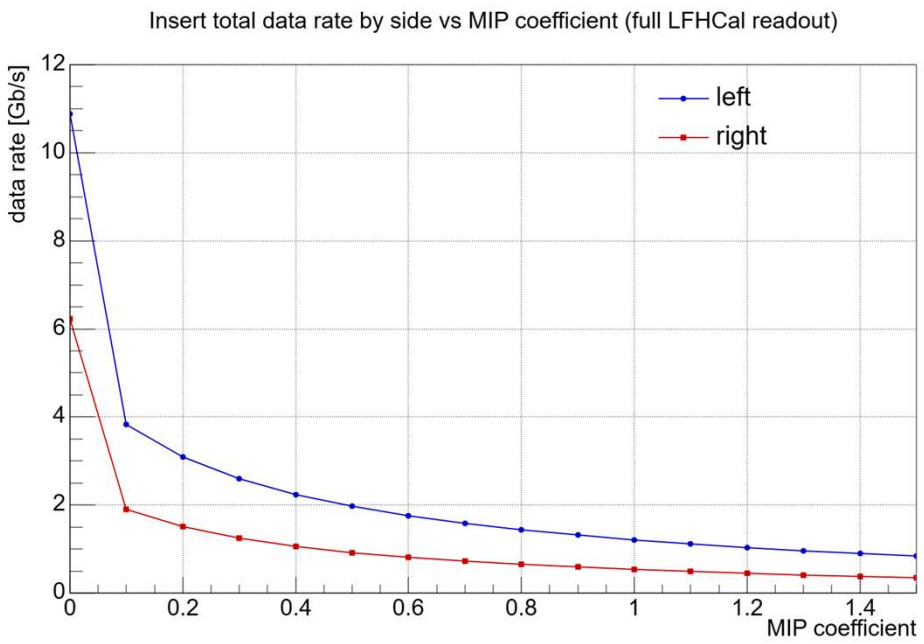


Side data rates with/without inner ring vs MIP

With inner ring



Without inner ring



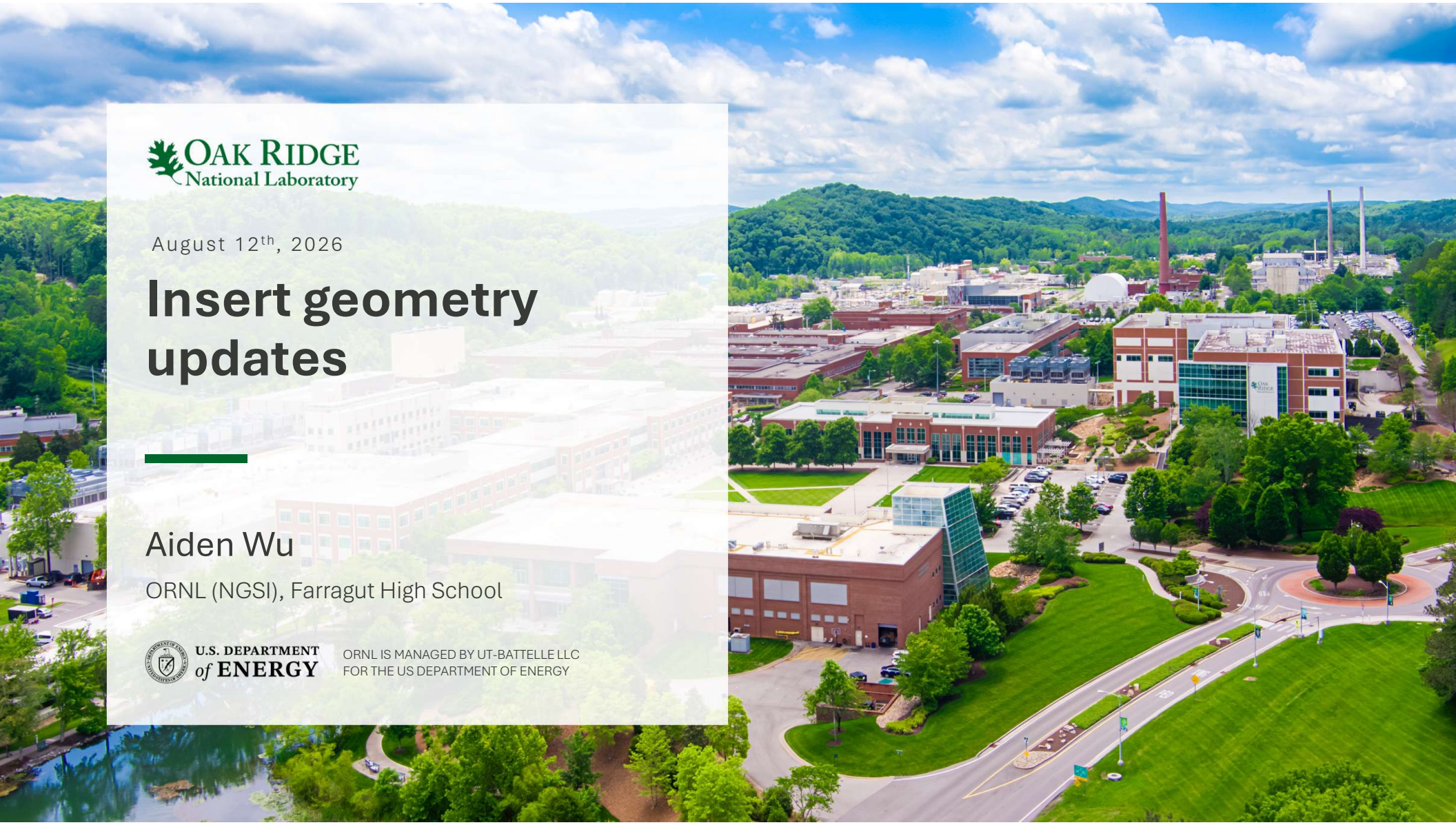
Summary

For the Insert

No inner ring	Channel p95	Channel p99	Chip p95	Chip p99	Left	Right
Original insert (0.5 MIP)	11.7 kHz 0.0015 Gb/s	18.9 kHz 0.0024 Gb/s	110 kHz 0.083 Gb/s	125 kHz 0.093 Gb/s	12.3 Gb/s	5.41 Gb/s
LFHCal tiles (0.5 MIP)	14.4 kHz 0.0018 Gb/s	23.8 kHz 0.0030 Gb/s	110 kHz 0.079 Gb/s	130 kHz 0.095 Gb/s	11.9 Gb/s	5.04 Gb/s
Full LFHCal (0.5 MIP)	27.1 kHz 0.0035 Gb/s	41.3 kHz 0.0053 Gb/s	158 kHz 0.13 Gb/s	162 kHz 0.14 Gb/s	1.97 Gb/s	0.920 Gb/s
Full LFHCal (0.1 MIP)	56.7 kHz 0.0073 Gb/s	75.6 kHz 0.0097 Gb/s	265 kHz 0.25 Gb/s	270 kHz 0.25 Gb/s	3.83 Gb/s	1.91 Gb/s

For the LFHCal

	Channel p95	Channel p99	Chip p95	Chip p99	Total
0.1 MIP	1.72 kHz 0.00022 Gb/s	5.81 kHz 0.00074 Gb/s	18.7 kHz 0.013 Gb/s	60.7 kHz 0.046 Gb/s	6.09 Gb/s



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Insert geometry updates

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U.S. DEPARTMENT of ENERGY

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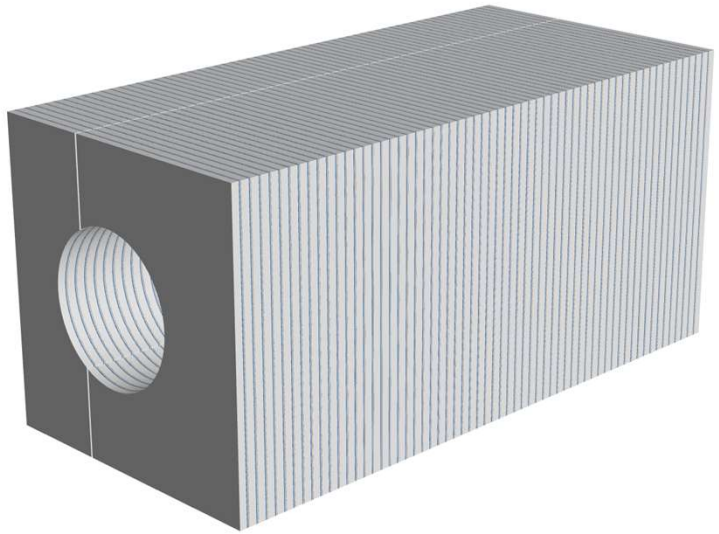
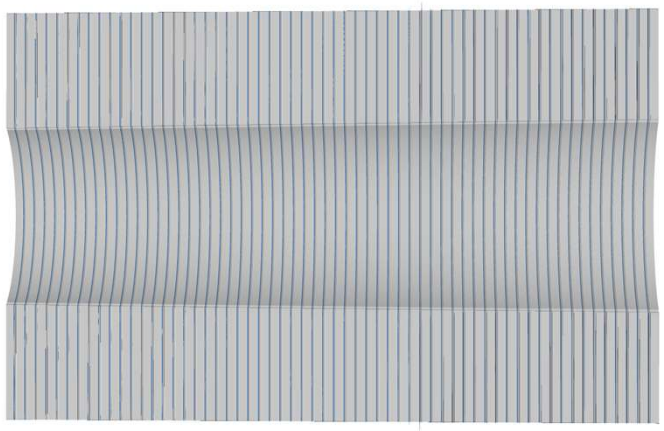
FOR THE US DEPARTMENT OF ENERGY

Original design

- 59.26 × 59.29 × 134.75 cm envelope
- 60 steel/scintillator sampling layers plus 1.52 cm steel backplate
- Layer thickness: 2.05 cm
    - Absorber, foil, scintillator, aluminum, FR4, and air slices
- Two halves separated by a 3.8 mm central gap
- 3 sizes of virtually segmented hexagonal tiles with per layer offsets
- Conical beampipe cutout



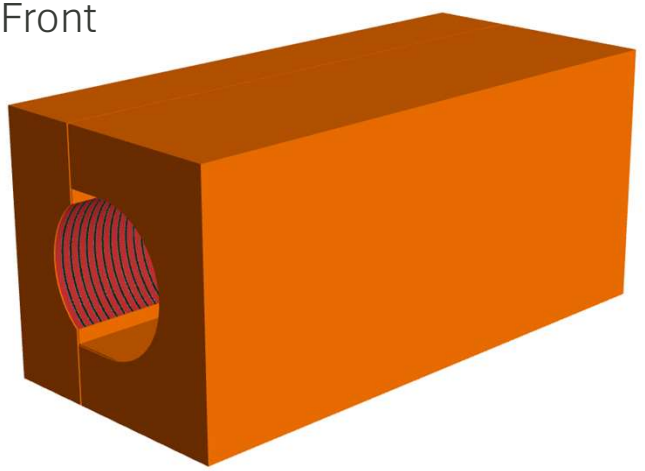


LFHCal-style design

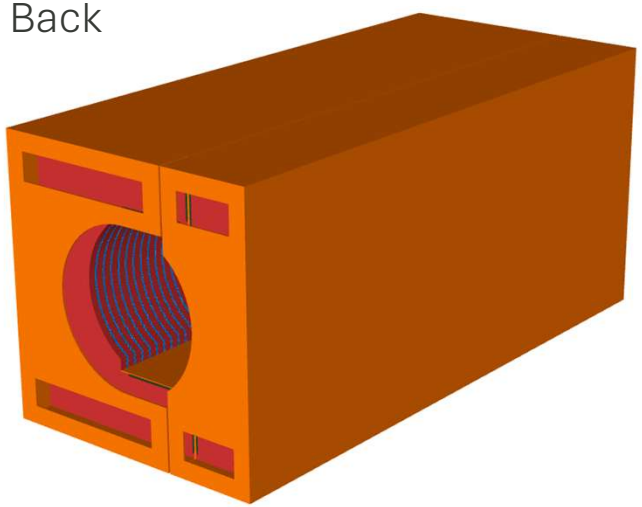
From Elliot Fountain

- 59.26 × 59.29 × 134.75 cm envelope
- 60 steel/scintillator sampling layers plus 1.52 cm steel backplate
- Layer thickness: 2.05 cm
  - Absorber, foil, scintillator, aluminum, FR4, and air slices
- Two halves separated by a 4 mm central gap
- Simplified 4.7 × 4.7 cm square scintillator tiles with 0.2 mm gaps (physically modeled)
- Fixed cylindrical beam-pipe cutout
- Steel casing, PCBs, covers, and rear cutouts

Front

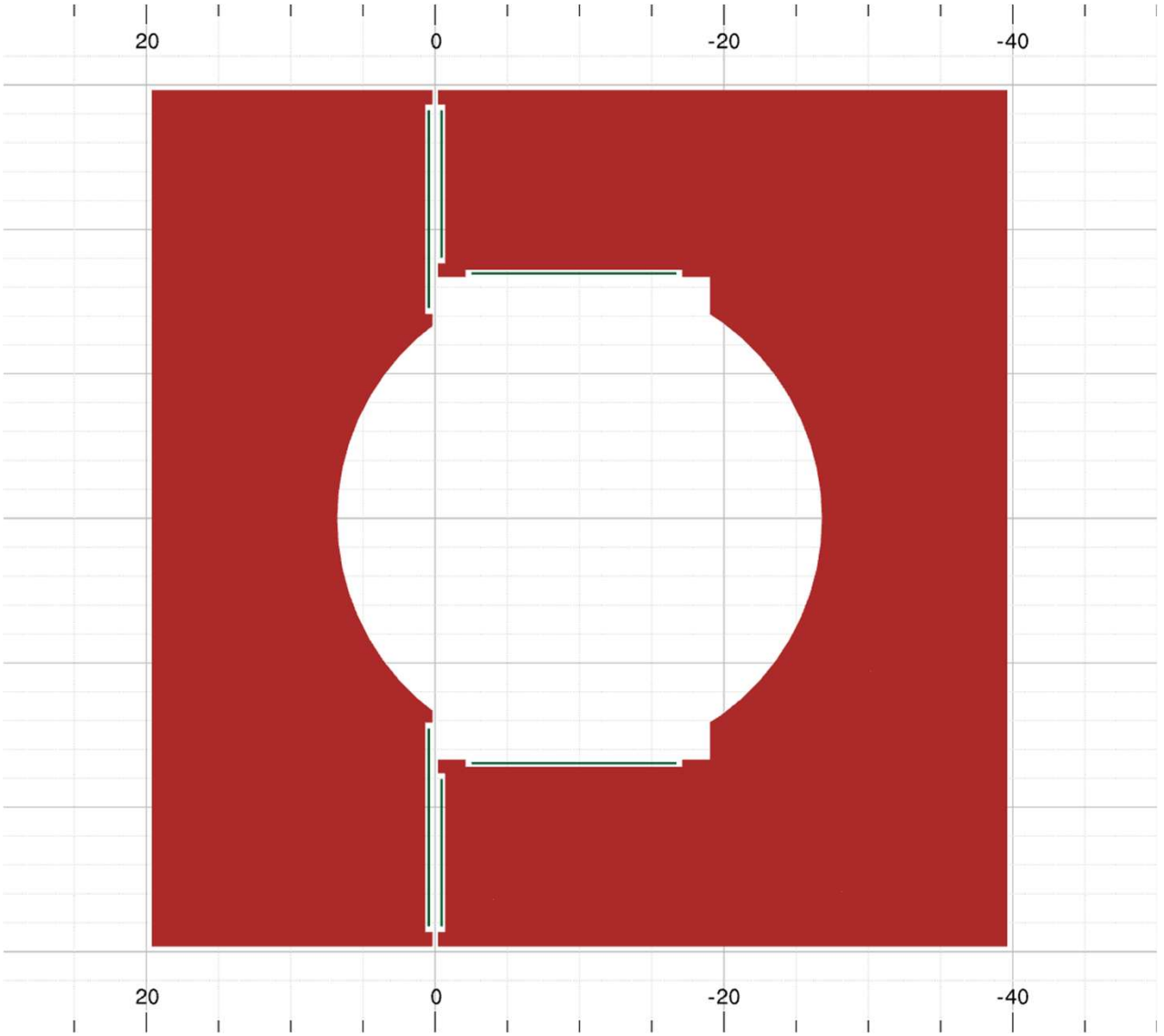


Back



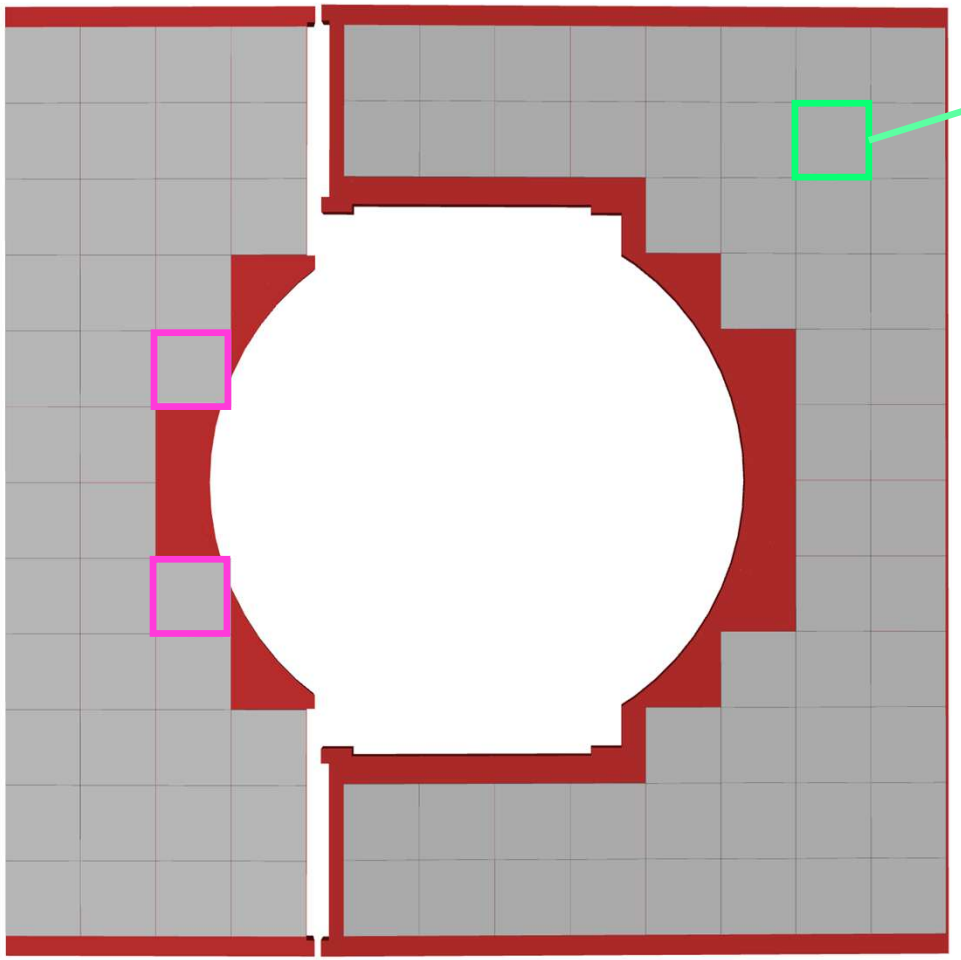
Front face (no casing)

- 1.6 mm PCBs run longitudinally through dedicated slots with constant edge clearance



Tiling

- Two tiles intersect with the beampipe opening
- 40 tiles on the left, 54 tiles on the right



Cell ID decoding/encoding

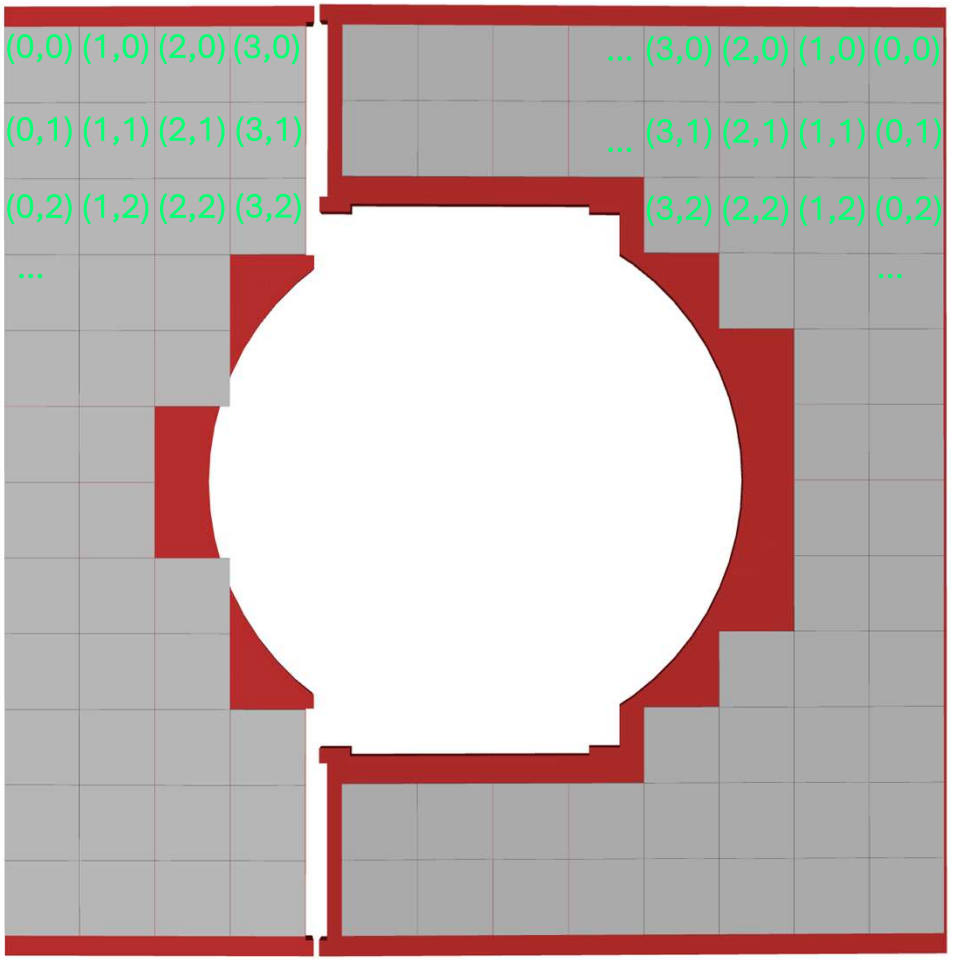
A cell ID consists of:

<id>system:8,side:1,layer:8,slice:7,x:32:-16,y:-16</id>

- system = 115; identifies the insert
- side: 0 for right, 1 for left
- layer ∈ {1, …, 60}: longitudinal sampling layer
- slice = 5; scintillator slice within the layer
- x, y = tile column, tile row; shown on the right

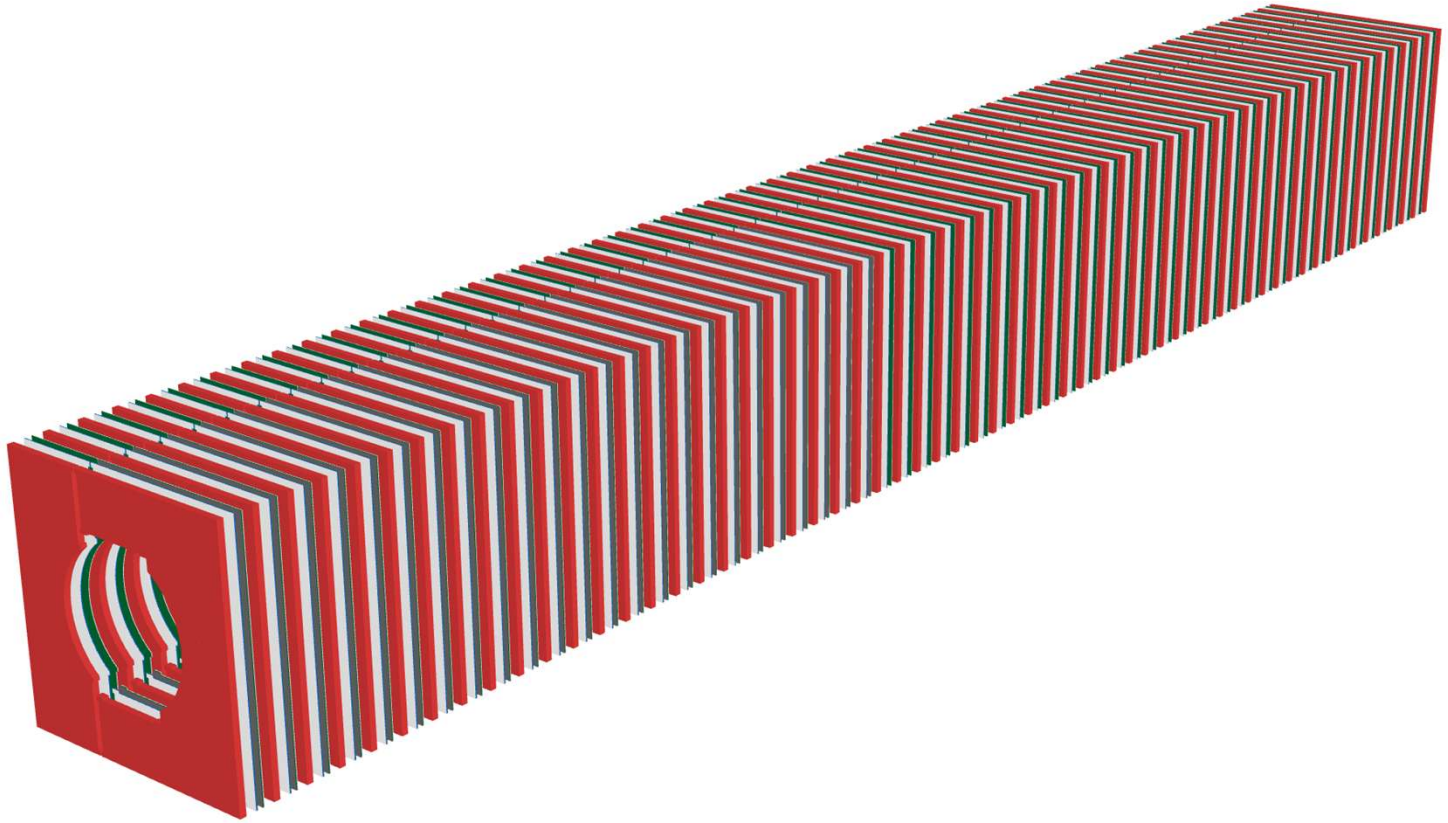
To find the center of a tile in cm using the column, row, and side:

- Left side: (27.26 – 4.72x, 25.96 – 4.72y)
- Right side: (– 27.04 + 4.72x, 25.96 – 4.72y)



Layers

- Layer composition and thicknesses remain unchanged, including the scintillator tiles



Summary

A simplified version of the Insert is available for simulation campaigns

- LFHCal-shaped tiles
- Uniform beampipe cutout
- Space for PCBs

Issues with LFHCal reconstruction in EICrecon, under investigation.