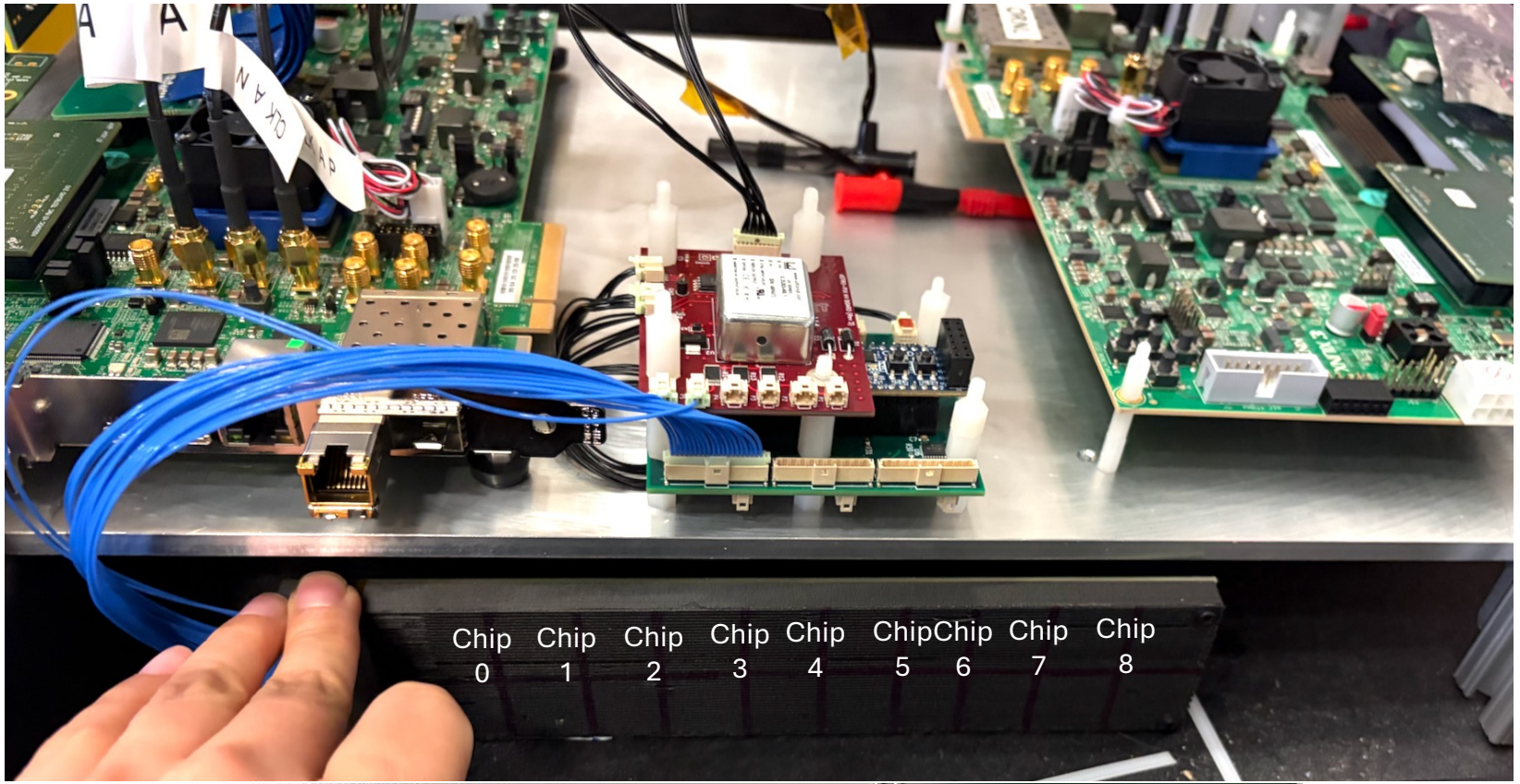
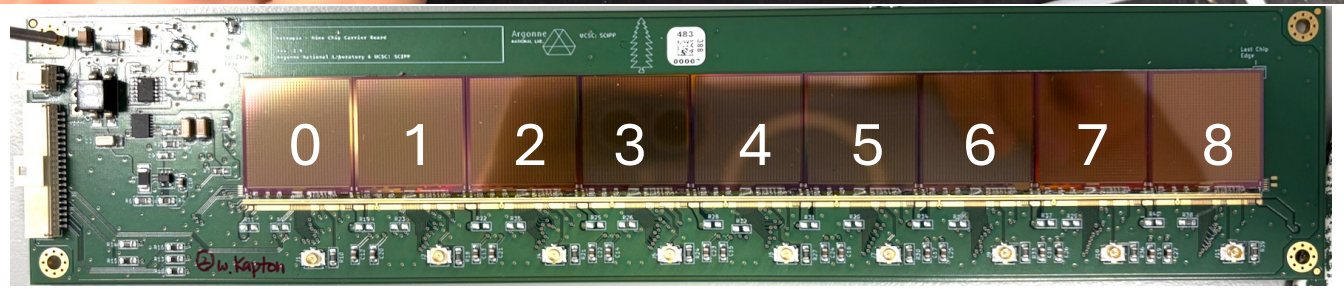
AstroPix Setting





9 chip prototype modules
- Module 4
- Module 8

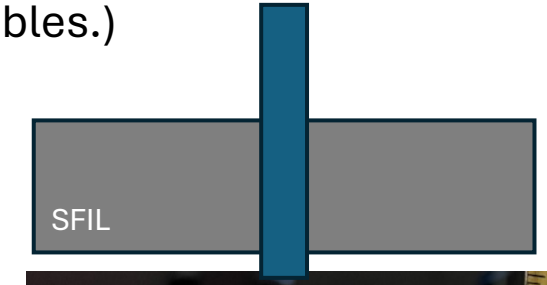
Standalone AstroPix running
: Ok
- Configured up to 9 chips
  : Ok
- Masking noisy pixel
  : Ok
- External clock
  : Ok

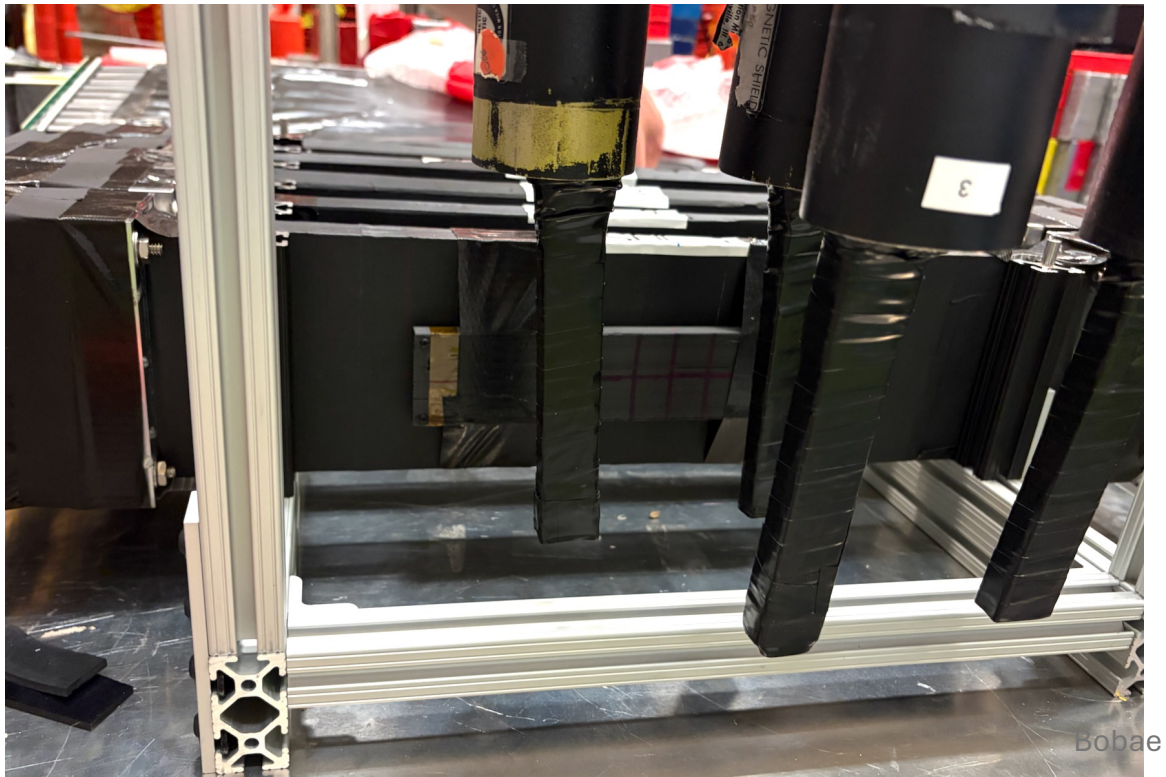
Online monitoring
- On-going
  (4->9 chips)

- AstroPix v3 size: ~2 cm X 2 cm; 9 AstroPix v3 module can cover ~18 cm x 2 cm.

Current Status & Plan

1. Check beam rate and AstroPix readout occupancies with a 9-chip module in front of 1st SFIL
    1. The the center of chip 4 was aligned with the center of 1st SFIL.
2. Two layer of 9-chips
   (if possible, an additional 2 inches of clearance is required above the SFIL.
   More space will be needed to accommodate the cables.)
    1. Use 2 cm X 18 cm instead of 18 cm X 2 cm





AstroPix standalone

```
(base) mep@carbon:~/astropix/astep-fw/sw$ python3.10 main.py -y module8 -c 9 -n test9_m8 -T 10
outputPrefix: '/home/mep/astropix/astep-fw/sw/data/20260805-093757' <class 'str'>
name: 'test9_m8' <class 'str'>
logname: '/home/mep/astropix/astep-fw/sw/data/20260805-093757test9_m8_run.log' <class 'str'>
abspath: '/home/mep/astropix/astep-fw/sw/data/20260805-093757test9_m8_run.log'
2026-08-05 09:37:57,087:87.__main__.INFO:Setup logger
Namespace(name='test9_m8', outputPrefix='/home/mep/astropix/astep-fw/sw/data/20260805-093757', loglevel='I', runTime=10.0, readout=None, yaml
=['module8'], chipsPerRow=[9], confOverride=False, noAutoread=False, threshold=200, analog=None, inject=None, vinj=None)
2026-08-05 09:37:57,108:108.root.INFO:Discovering FSP
2026-08-05 09:37:57,110:110.rfg.io.uart.INFO:Opened Serial port /dev/ttyUSB1 with baud 921600 bps
2026-08-05 09:37:57,110:110.__main__.INFO:Opened FPGA, testing...
2026-08-05 09:37:57,122:122.__main__.INFO:FW ID: 44051
2026-08-05 09:37:57,122:122.__main__.INFO:FPGA test successful.
2026-08-05 09:37:57,138:138.drivers.boards.board_driver.WARNING:Not Enabling External Clock, FW is already running on the external clock
2026-08-05 09:37:57,154:154.__main__.INFO:clock_ctrl=0x0000001e
2026-08-05 09:37:57,154:154.__main__.INFO:FPGA is operating with the external single-ended clock.
2026-08-05 09:37:57,154:154.__main__.INFO:Clock status bits: ext_selected=1, clock_mode_bit=1, enable_req=0
/home/mep/astropix/astep-fw/sw/scripts/config/module8.yml
2026-08-05 09:37:57,269:269.drivers.astropix.asic.INFO:astropix3  Configuration file with 9 chips found!
2026-08-05 09:37:57,269:269.drivers.astropix.asic.INFO:astropix3 Number of chips in chain: 9
2026-08-05 09:37:57,269:269.drivers.astropix.asic.INFO:astropix3 matrix dimensions found!
2026-08-05 09:37:57,269:269.drivers.astropix.asic.INFO:Chain chip_0 config found!
2026-08-05 09:37:57,269:269.drivers.astropix.asic.INFO:Chain chip_1 config found!
2026-08-05 09:37:57,269:269.drivers.astropix.asic.INFO:Chain chip_2 config found!
2026-08-05 09:37:57,269:269.drivers.astropix.asic.INFO:Chain chip_3 config found!
2026-08-05 09:37:57,269:269.drivers.astropix.asic.INFO:Chain chip_4 config found!
2026-08-05 09:37:57,269:269.drivers.astropix.asic.INFO:Chain chip_5 config found!
2026-08-05 09:37:57,269:269.drivers.astropix.asic.INFO:Chain chip_6 config found!
2026-08-05 09:37:57,270:270.drivers.astropix.asic.INFO:Chain chip_7 config found!
2026-08-05 09:37:57,270:270.drivers.astropix.asic.INFO:Chain chip_8 config found!
2026-08-05 09:37:57,270:270.__main__.INFO:1 ASIC drivers instanciated.
2026-08-05 09:37:57,410:410.__main__.INFO:[00.0 s] buff=0000 status: 0=10-010101-0000 1=01-010100-0000 2=01-010100-0000
2026-08-05 09:37:58,100:100.drivers.astropix.asic.INFO:SPI Config bits, tdac False, len=1545
2026-08-05 09:37:58,372:372.drivers.astropix.asic.INFO:SPI Config bits, tdac False, len=1545
2026-08-05 09:37:58,644:644.drivers.astropix.asic.INFO:SPI Config bits, tdac False, len=1545
2026-08-05 09:37:58,916:916.drivers.astropix.asic.INFO:SPI Config bits, tdac False, len=1545
2026-08-05 09:37:59,188:188.drivers.astropix.asic.INFO:SPI Config bits, tdac False, len=1545
2026-08-05 09:37:59,460:460.drivers.astropix.asic.INFO:SPI Config bits, tdac False, len=1545
2026-08-05 09:37:59,732:732.drivers.astropix.asic.INFO:SPI Config bits, tdac False, len=1545
2026-08-05 09:38:00,003:3.drivers.astropix.asic.INFO:SPI Config bits, tdac False, len=1545
2026-08-05 09:38:00,276:276.drivers.astropix.asic.INFO:SPI Config bits, tdac False, len=1545
2026-08-05 09:38:00,530:530.__main__.INFO:Flush chips before data collection
2026-08-05 09:38:00,562:562.__main__.INFO:interrupt low
2026-08-05 09:38:00,658:658.__main__.INFO:interrupt low
2026-08-05 09:38:00,754:754.__main__.INFO:interrupt low
2026-08-05 09:38:00,866:866.__main__.INFO:Flush FPGA buffer before data collection
```

AstroPix standalone