sPHENIX Director's Review: 1.2.5 TPC FEE

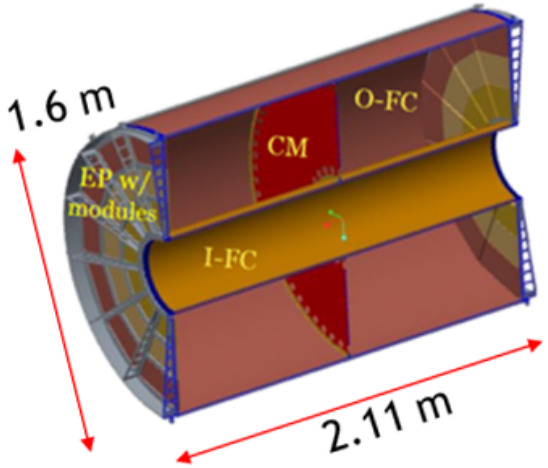
Takao Sakaguchi, BNL Physics

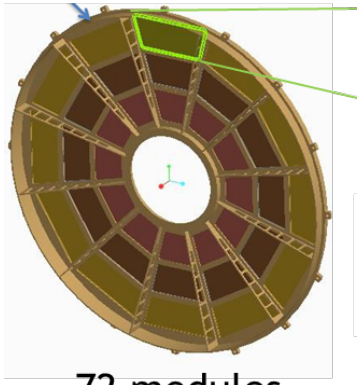
August 2-4, 2017

BNL

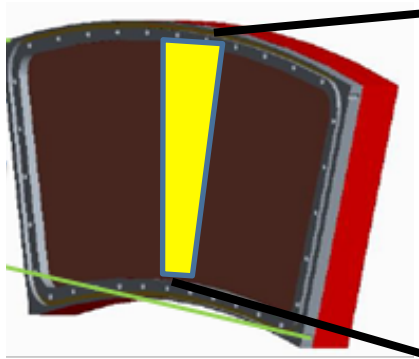
The Subsystem

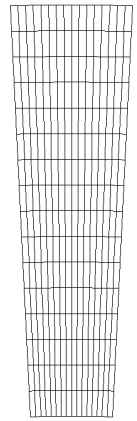
- WBS 1.2.5: Front End Electronics (FEE) for the TPC
  - **Receive analog signal from the padplane on TPC, and send the digitized data out to the backend electronics (DAM) via optical cable**



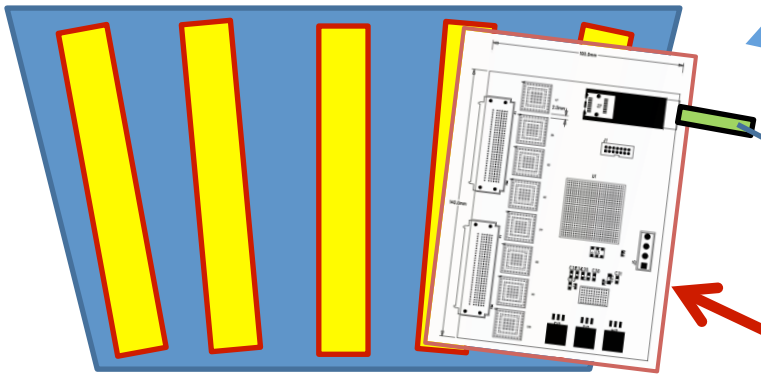


72 modules
2(z), 12(ϕ), 3(r)





16 pads
~2mm



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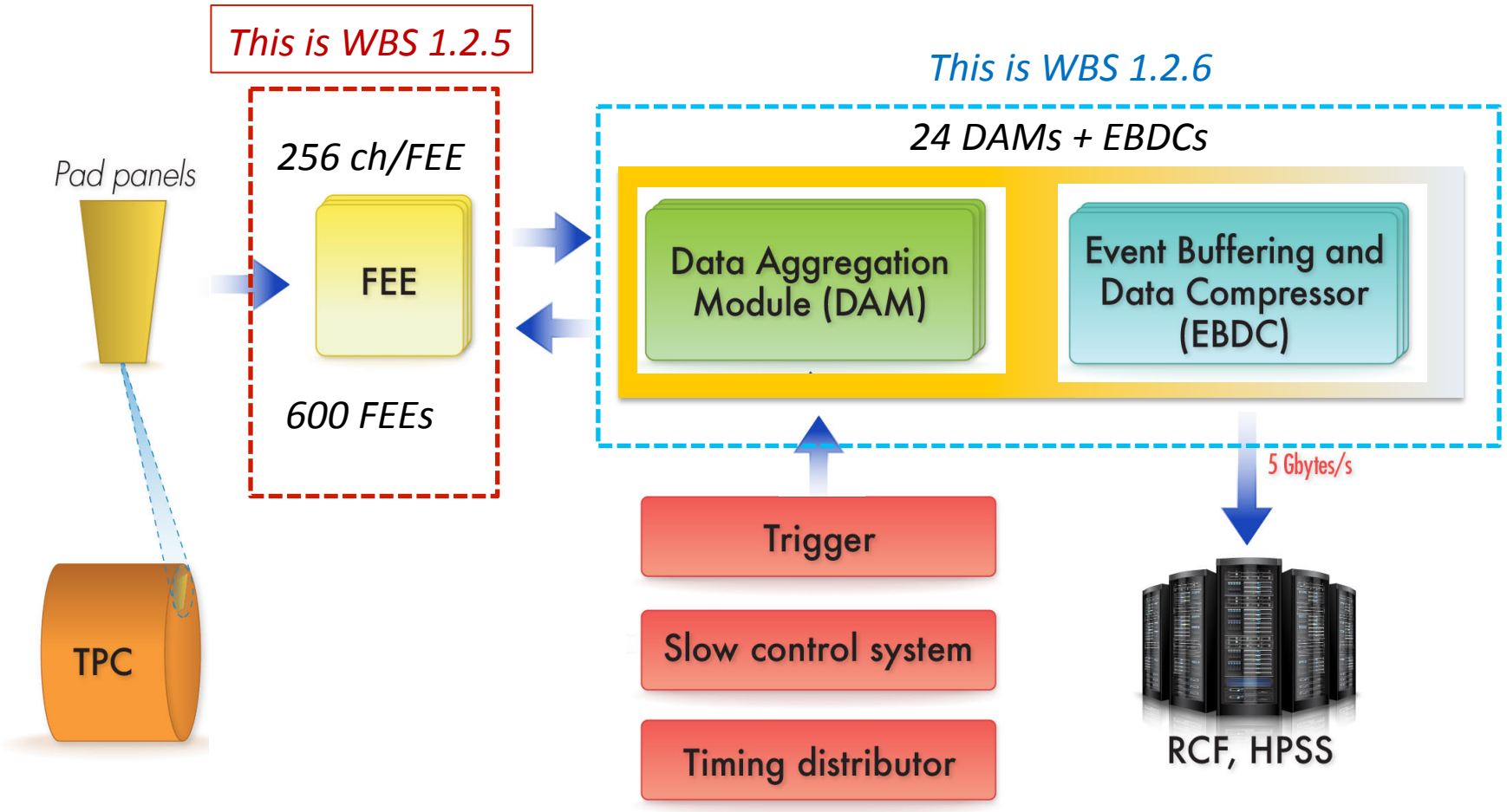
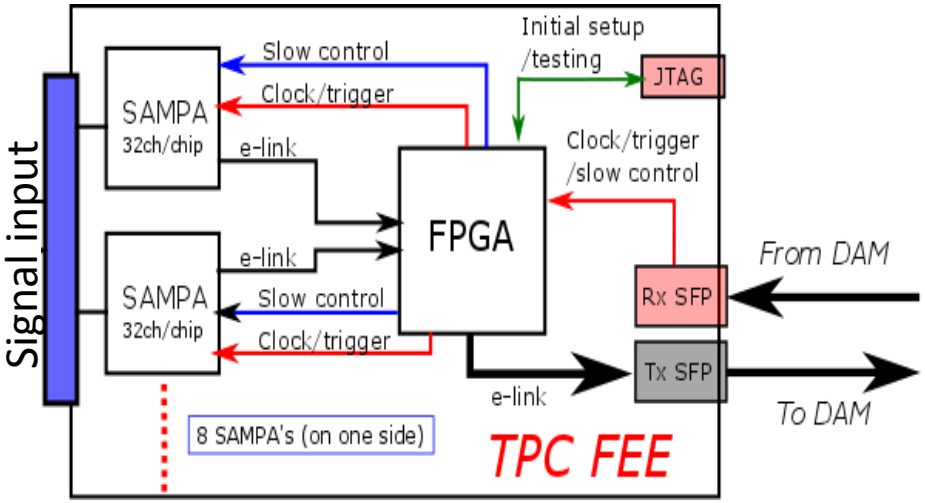


The Subsystem Technical Overview

- 154K channels from both ends of TPC
  - **One FEE takes care of 256 channels**
    - **→ 600 FEEs in total**
  - **25 FEE for 1/12 of one end**
  - **8 SAMPAs + FPGA**
  - **Operates at 10MHz sampling**
  - **Continuous readout mode**
- SAMPA = CSA + Shaper + ADC + DSP
  - **32ch input**
- FPGA receives slow control and timing/clock signal from DAM via optical fiber, and distributes to SAMPAs
- FPGA collects digitized data from SAMPAs and send them to DAM via optical fiber
- FPGA can also perform initial data reduction



FPGA candidate: Xilinx Artix-7

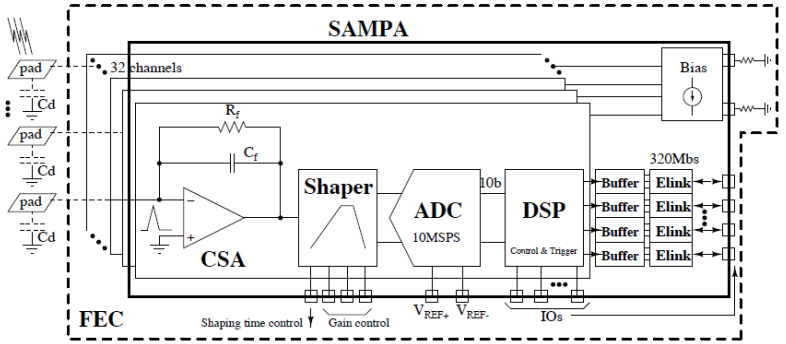
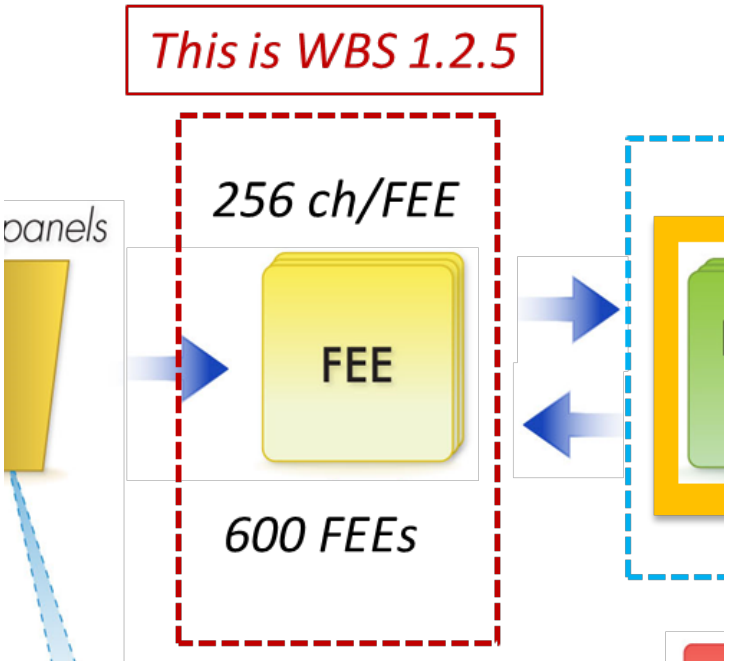


Figure 6.4: Schematic of the SAMPA ASIC for the GEM TPC readout, showing the main building blocks.

Scope

- WBS 1.2.5 includes cost for:
  - **FEE board production**
  - **Procurement of male (female) connectors on the FEE card and female (male) connectors on padplane**
  - **Test stand development and equipment to test the FEEs**

- WBS 1.2.5 doesn't include cost for:
  - **Optical fiber from FEE to DAM module**
  - **A DAM module for FEE testing**
  - **They are included in WBS 1.2.6**



Subsystem Collaborators

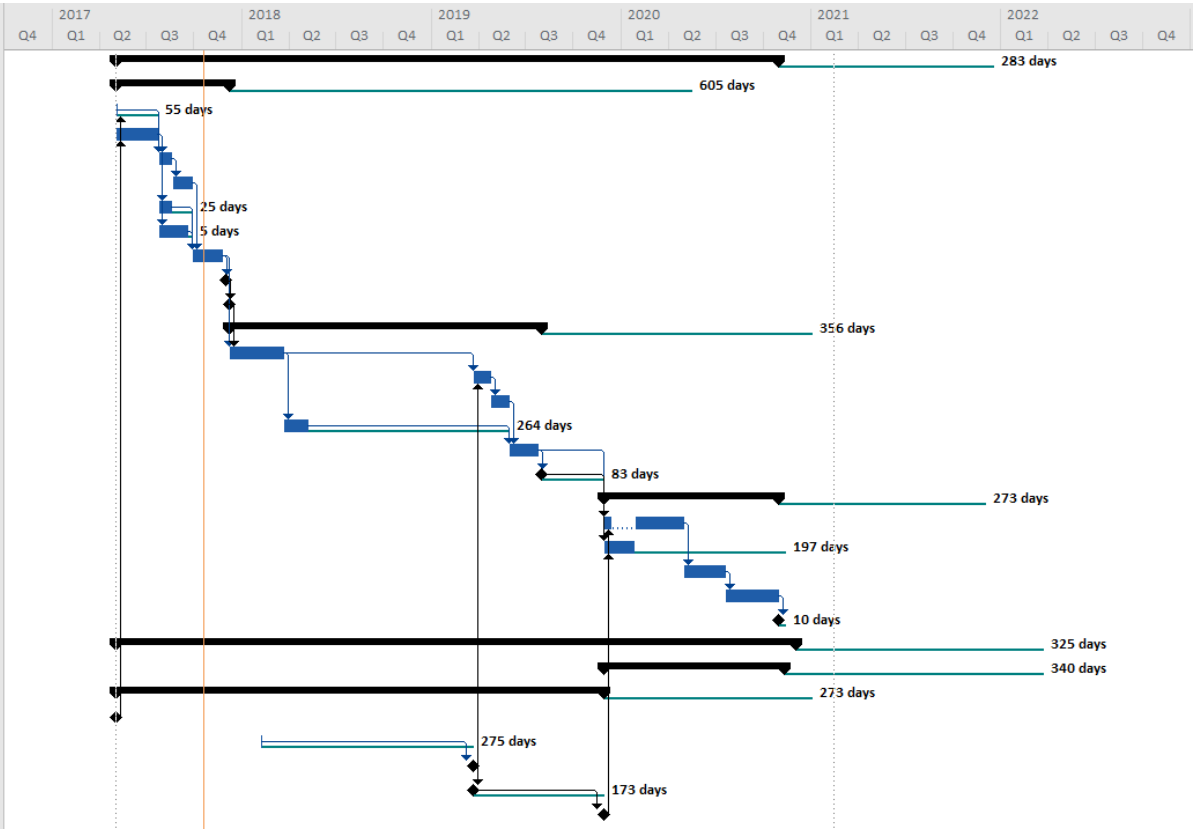
- CAM (Physicist): Takao Sakaguchi (BNL Physics)
  - **20+ years experience of detectors and electronics, including RICH detector and its FEE development (1996-2004), and HBD detector (2006-2011) in PHENIX**
- Primary engineer 1: Joe Mead (BNL Instrumentation)
  - **25 years experience in designing high speed electronic circuitry, embedded systems, and DAQ systems for high-energy/nuclear physics and neutron/photon applications**
  - **X-ray Detector (2012-) , NSLS II Beam Position Monitor (BPM) Electronics (2009-), LSST (2012- 2014), ATLAS LAr Calor. Readout (2007-2012), Neutron Detector DAQ (2000-2007), SNS BPM Electronics (2002-2005), RHIC BPM Electronics (1995-2002), PHENIX Timing System (1995-2000)**
- Primary engineer 2: John Kuczewski (BNL Instrumentation)
  - **Another very experienced electronic engineer**
- Other helps
  - **SAMPA development: M. Bregant (Univ. of Sao Paulo)**
  - **STAR iTPC experts: T. Ljubicic, B. Sheetz, F. Videbaek (BNL Physics)**
  - **ALICE TPC experts (former PHENIX collaborators): K. Read, C. Britton (ORNL), A. Oskarsson, D. Silvermyr (Lund Univ.)**

Schedule Drivers

- Prototyping will be finished before CD-2 review. Production will start after CD-2 authorization
- 3-4 months each for parts procurement, board fabrication and parts mounting, and QA testing for the final production

Year is in FY

Name	Levelir Delay	Duration
TPC FEE	0 edays	871 days
TPC FEE Prototype v1	0 edays	152 days
Write TPC FEE prototype v1 design specification	0 edays	2 days
Design TPC FEE protoype v1	0 edays	57 days
Procure TPC FEE prototype v1 components	0 edays	20 days
Fabricate TPC FEE prototype v1 boards	0 edays	25 days
Procure TPC FEE prototype v1 LV power supplies	0 edays	20 days
Develop TPC FEE Test Stand	0 edays	40 days
Assemble and test TPC FEE prototype v1	0 edays	40 days
TPC FEE Safety Review	0 edays	0 days
TPC FEE Design Review	0 edays	0 days
TPC FEE Pre-Production	0 edays	409 days
Design TPC FEE preproduction protoype	0 edays	70 days
Procure TPC FEE preproducion prototype compone	0 edays	20 days
Fabricate TPC FEE preproduction prototype boards	0 edays	25 days
Modify TPC FEE Test Stand	0 edays	30 days
Assemble and test TPC FEE preproduction prototyp	0 edays	40 days
TPC FEE Production Readiness Review	0 edays	0 days
TPC FEE Production	0 edays	227 days
Procure TPC FEE components	0 edays	70 days
Procure TPC FEE LV power supplies	0 edays	40 days
Fabricate and assemble all TPC Fee boards	0 edays	55 days
Perform QA Testing on TPC FEE	0 edays	70 days
TPC FEE Production Ends	0 edays	0 days
TPC DAM	0 edays	894 days
TPC Support Systems	0 edays	235 days
Tracker Management	0 edays	644 days
CD-0 Authorization	0 edays	0 days
CD-1, CD-2a/CD-3a Review	0 edays	3 days
CD-1, CD-2a/CD-3a Authorization	0 edays	0 days
CD-2b/CD-3b Review	0 edays	0 days
CD-2b/CD-3b Authorization	0 edays	0 days



Cost Drivers

- We performed a bottom-up cost estimate
  - **1.2.5.1: Prototype v1**
  - **1.2.5.2: Pre-production proto.**
  - **1.2.5.3: Production**

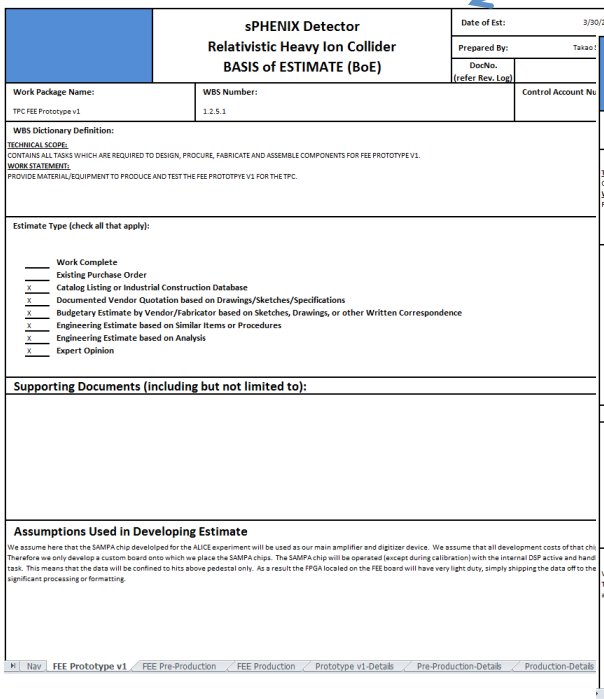
Navigation pan

sPHENIX Detector
Relativistic Heavy Ion Collider
BASIS of ESTIMATE (BoE)

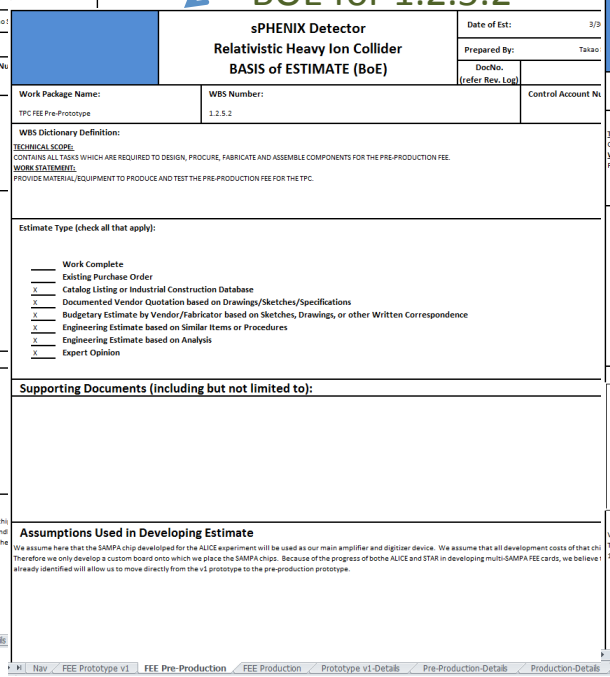
L2 Project Name	L2 WBS Number	L3 Project Name (Control Account)	L3 WBS Number
Time Projection Chamber	1.2	TPC FEE	1.2.5

Work Package Name	WBS Number	Basis of Estimate Link
TPC FEE Prototype v1	1.2.5.1	FEE Prototype v1
TPC FEE Pre-Production	1.2.5.2	FEE Pre-Production
TPC FEE Production	1.2.5.3	FEE Production

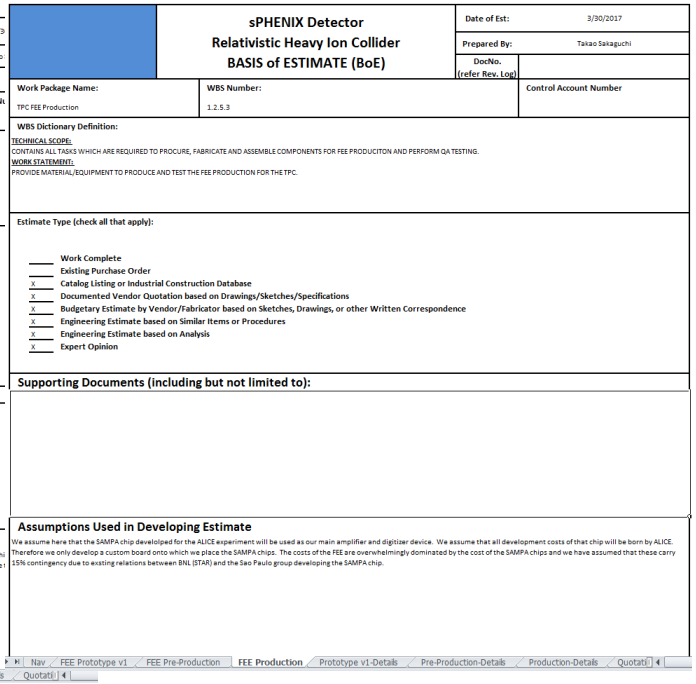
BOE for 1.2.5.1


sPHENIX Detector
Relativistic Heavy Ion Collider
BASIS of ESTIMATE (BoE)
Date of Est: 3/30/2017
Prepared By:
DocNo. (refer Rev. Log)
Work Package Name: TPC FEE Prototype v1
WBS Number: 1.2.5.1
Control Account Nu
WBS Dictionary Definition:
TECHNICAL SCOPE:
CONTAINS ALL TASKS WHICH ARE REQUIRED TO DESIGN, PROCURE, FABRICATE AND ASSEMBLE COMPONENTS FOR FEE PROTOTYPE V1.
WORK STATEMENT:
PROVIDE MATERIAL/EQUIPMENT TO PRODUCE AND TEST THE FEE PROTOTPYE V1 FOR THE TPC.
Estimate Type (check all that apply):
Work Complete
Existing Purchase Order
X Catalog Listing or Industrial Construction Database
X Documented Vendor Quotation based on Drawings/Sketches/Specifications
X Budgetary Estimate by Vendor/Fabricator based on Sketches, Drawings, or other Written Correspondence
X Engineering Estimate based on Similar Items or Procedures
X Engineering Estimate based on Analysis
X Expert Opinion
Supporting Documents (including but not limited to):
Assumptions Used in Developing Estimate
We assume here that the SAMPA chip developed for the ALICE experiment will be used as our main amplifier and digitizer device. We assume that all development costs of that chi
Therefore we only develop a custom board onto which we place the SAMPA chips. The SAMPA chip will be operated (except during calibration) with the internal DSP active and handl
task. This means that the data will be confined to hits above pedestal only. As a result the FPGA located on the FEE board will have very light duty, simply shipping the data off to the
significant processing or formatting.
Nav | FEE Prototype v1 | FEE Pre-Production | FEE Production | Prototype v1-Details | Pre-Production-Details | Production-Details

BOE for 1.2.5.2


sPHENIX Detector
Relativistic Heavy Ion Collider
BASIS of ESTIMATE (BoE)
Date of Est: 3/3
Prepared By: Takao
DocNo. (refer Rev. Log)
Work Package Name: TPC FEE Pre-Prototype
WBS Number: 1.2.5.2
Control Account Nu
WBS Dictionary Definition:
TECHNICAL SCOPE:
CONTAINS ALL TASKS WHICH ARE REQUIRED TO DESIGN, PROCURE, FABRICATE AND ASSEMBLE COMPONENTS FOR THE PRE-PRODUCTION FEE.
WORK STATEMENT:
PROVIDE MATERIAL/EQUIPMENT TO PRODUCE AND TEST THE PRE-PRODUCTION FEE FOR THE TPC.
Estimate Type (check all that apply):
Work Complete
Existing Purchase Order
X Catalog Listing or Industrial Construction Database
X Documented Vendor Quotation based on Drawings/Sketches/Specifications
X Budgetary Estimate by Vendor/Fabricator based on Sketches, Drawings, or other Written Correspondence
X Engineering Estimate based on Similar Items or Procedures
X Engineering Estimate based on Analysis
X Expert Opinion
Supporting Documents (including but not limited to):
Assumptions Used in Developing Estimate
We assume here that the SAMPA chip developed for the ALICE experiment will be used as our main amplifier and digitizer device. We assume that all development costs of that chi
Therefore we only develop a custom board onto which we place the SAMPA chips. Because of the progress of bothe ALICE and STAR in developing multi-SAMPA FEE cards, we believe t
already identified will allow us to move directly from the v1 prototype to the pre-production prototype.
Nav | FEE Prototype v1 | FEE Pre-Production | FEE Production | Prototype v1-Details | Pre-Production-Details | Production-Details | Quotati

BOE for 1.2.5.3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Relativistic Heavy Ion Collider
BASIS of ESTIMATE (BoE)
Date of Est: 3/30/2017
Prepared By: Takao Sakaguchi
DocNo. (refer Rev. Log)
Work Package Name: TPC FEE Production
WBS Number: 1.2.5.3
Control Account Number
WBS Dictionary Definition:
TECHNICAL SCOPE:
CONTAINS ALL TASKS WHICH ARE REQUIRED TO PROCURE, FABRICATE AND ASSEMBLE COMPONENTS FOR FEE PRODUCITON AND PERFORM QA TESTING.
WORK STATEMENT:
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Estimate Type (check all that apply):
Work Complete
Existing Purchase Order
X Catalog Listing or Industrial Construction Database
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We assume here that the SAMPA chip developed for the ALICE experiment will be used as our main amplifier and digitizer device. We assume that all development costs of that chip will be born by ALICE.
Therefore we only develop a custom board onto which we place the SAMPA chips. The costs of the FEE are overwhelmingly dominated by the cost of the SAMPA chips and we have assumed that these carry
15% contingency due to existing relations between BNL (STAR) and the Sao Paulo group developing the SAMPA chip.
Nav | FEE Prototype v1 | FEE Pre-Production | FEE Production | Prototype v1-Details | Pre-Production-Details | Production-Details | Quotati

Cost Drivers

- Prototyping and test stand development: $100k (with 23% contingency)
- Production
  - **SAMPA (7800 chips): $350k**
  - **FPGA (750 chips): $75k**
  - **All other peripherals: $150k**
  - **Board prod. and mounting costs: $120k**
  - **Power supply (22 units): $110k**
  - **$810k is the net total. $960k with 19% contingency**

Purchase for 80% yield of good tested boards

Contingency numbers are the weighted average of those for each item

	A	B	C	D	E	F	G	J	K
1	WBS	Description	Item	Vendor	Total	Status	Basis of Estimate	Wt Contingency	Total
2	1.2.5.3	TPC FEE Production						0.19	
3	1.2.5.3.1	Procure TPC FEE components						0.19	$576,000
4			SAMPA chip	CERN	$351,000	Pending	4800 + 3000 chips (~$45/chip)		
5			FPGA (Artix-7)	Xilinx	$75,000	Pending	Weq quote (98 * 600 +25% spare)		
6			Optical transmitter/receiver	Avago	$37,500	Pending	50 * 600 + 25% spare		
7			Resistor/capacitor/regulator	Digikey	$75,000	Pending	100 * 600 + 25% spare		
8			Card Connectors	Samtec	$37,500	Pending	50 * 600 + 25% spare		
9	1.2.5.3.2	Procure TPC FEE LV power supplies						0.16	$116,484
10			10AWG 6T00UP Cable	Belden	$6,000	Pending	$1.5/ft, 4000ft.		
11			MegaPac chassis (5V)	Vicor West Coast	$110,484	Pending	manufacture quote (5022 * 20 + 2 spare)		
12	1.2.5.3.3	Fabricate and assemble all TPC Fee boards						0.20	$115,500
13			Initial fee		$2,000	Pending			
14			Board fabrication		$75,000	Pending	100 * 600 + 25% spare		
15			parts mounting initial fee		$1,000				
16			Parts mounting		$37,500	Pending	50 * 600 + 25% spare		

Basis of Estimate and Resource-Loaded Schedule

- All documents are in place

sPHENIX Detector
Relativistic Heavy Ion Collider
BASIS of ESTIMATE (BoE)

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		parts mounting initial fee		$1,000				
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Relativistic Heavy Ion Collider
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Date of Est: 3/30/2017
Prepared By: Takao Sakaguchi
DocNo. (refer Rev. Log):

Work Package Name:	WBS Number:	Control Account Number
TPC FEE Prototype v1	1.2.5.1	

WBS Dictionary Definition:

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Nav | FEE Prototype v1 | FEE Pre-Production | FEE Production | Prototype v1-Details | Pre-Production-Details | Production-Details | Quotati

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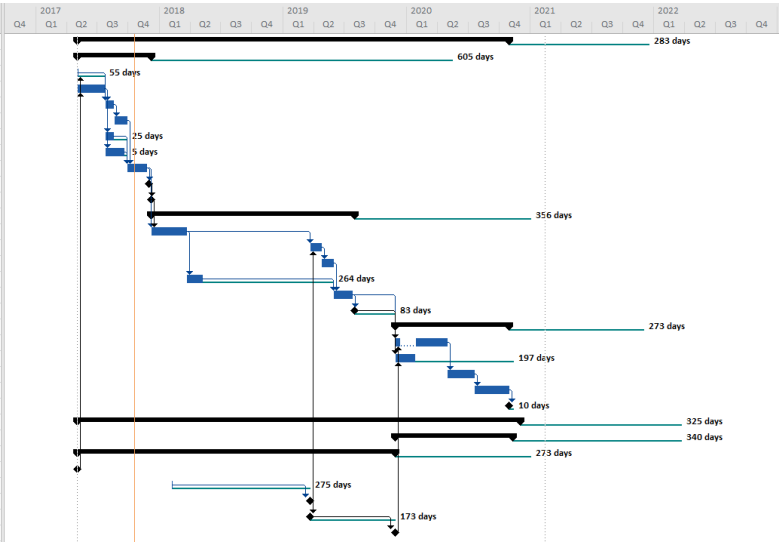
CD-2b/CD-3b Authorization	0 edays	0 days

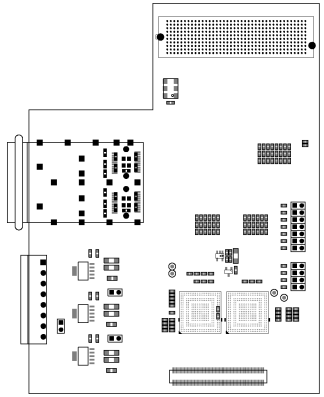


Status and Highlights (I)

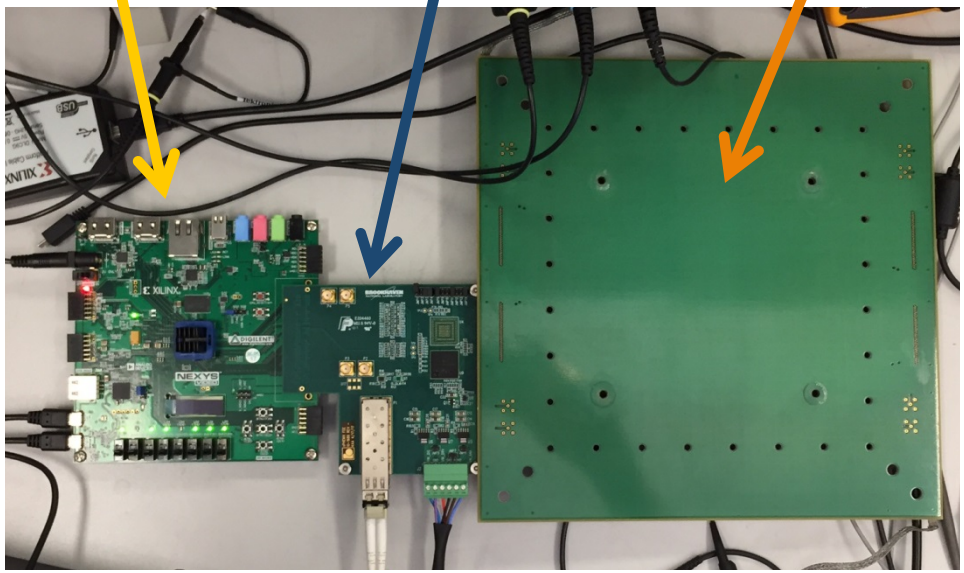
- Small-scale prototype was produced and is being tested
  - **Board consists of two SAMPAs and a SFP (optical module)**
  - **Purpose is to check interface of SAMPA and FPGA**
  - **FPGA function is provided by Xilinx Artix-7 evaluation board**
- Found and fixed several interface mismatch
- Succeeded in performing slow control of SAMPA and reading out ADC and sync data through FPGA memory
- Attached a prototype padplane to the prototype FEE, and now trying reading out the data with injecting pulses

Xilinx Artix-7 evaluation board

SAMPA + SFP board



Prototype padplane

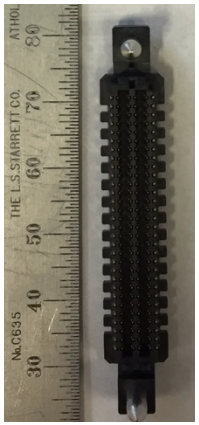


Status and Highlights (II)

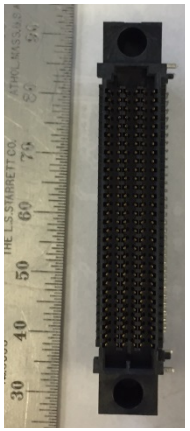
- Design of full-scale prototype is in progress.
- Full-scale prototype design will be passed to board routing as soon as we finished evaluating basic features of SAMPA with small-scale prototype
- Selecting of peripheral parts are almost done.

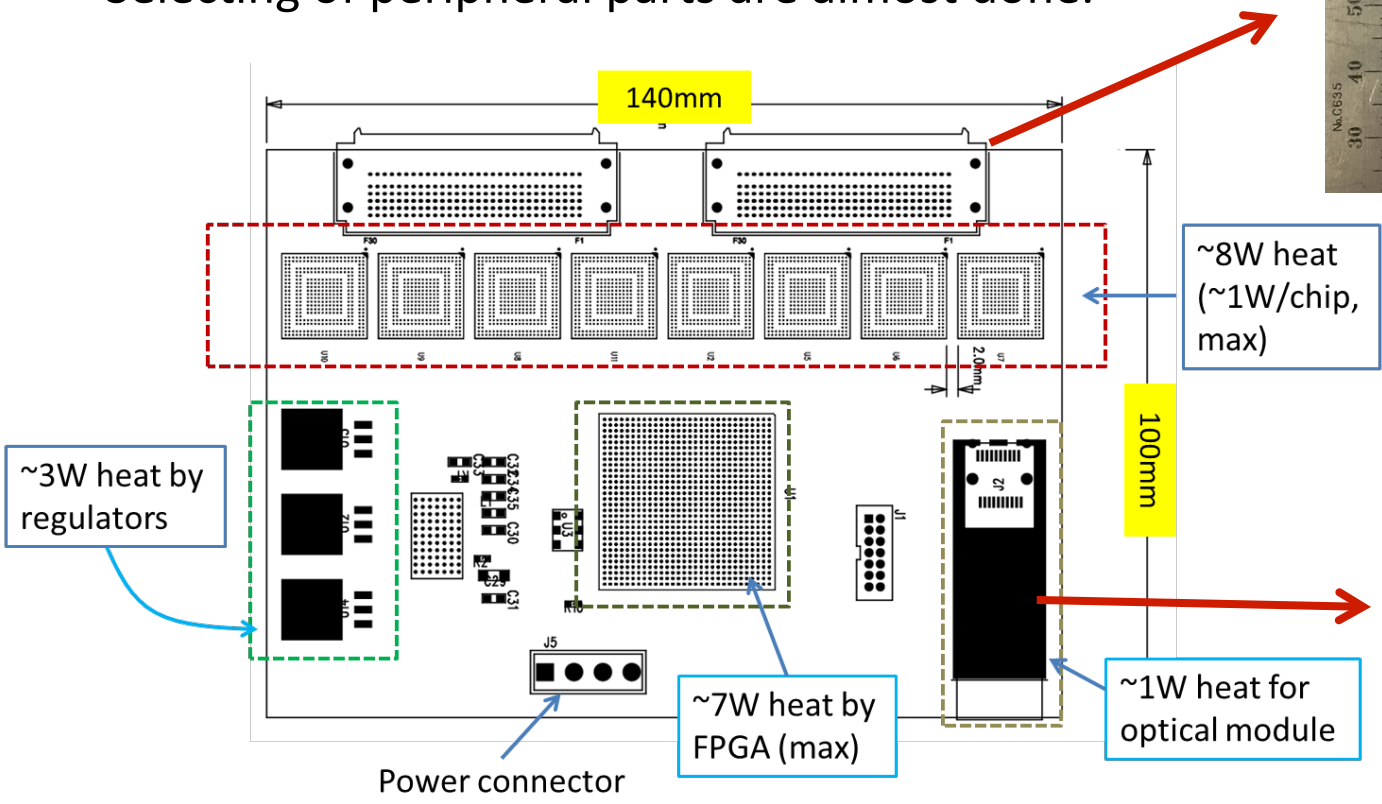
Signal connectors

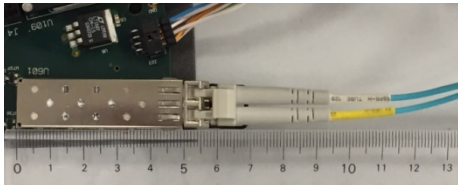
Padplane side



FEE side







Summary

- We have produced the cost and schedule for the TPC FEE (WBS 1.2.5) by bottom-up estimate
  - **$100K for prototyping, $960K for final production, including contingency**
- Enough resource of engineering as well as technical consultation from outside sPHENIX is available
- Excellent progress has been made for prototyping
- Parts for final production will be readily available upon necessity
  - **We have been in close contact with SAMPA development, production, and testing team so that the chips will be readily provided upon request**

Back Up

Design parameters

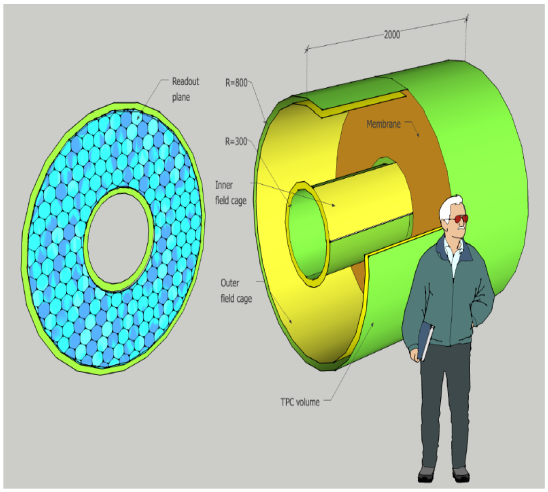
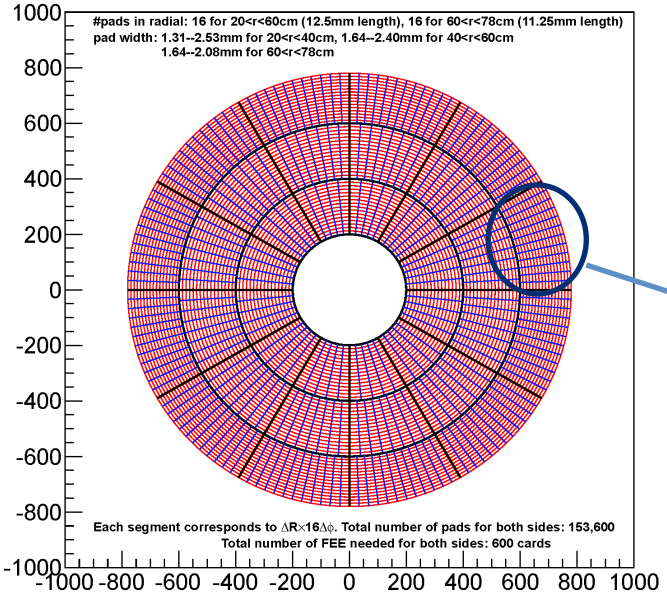
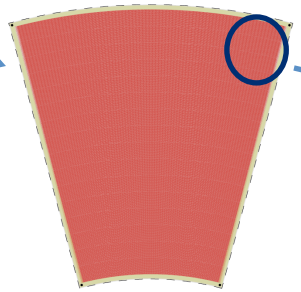
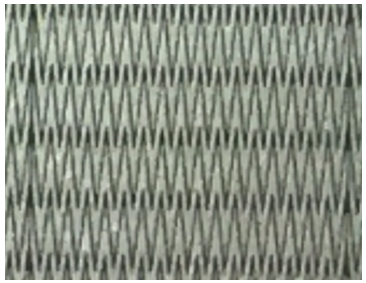


Figure 4.26: Schematic layout of TPC main elements.



- 154K readout channels from both ends
  - **40 measurements (clusters) in radial direction**
- 15KHz is the baseline trigger rate
  - **limit of DAQ rate prior to livetime fall-off**
  - **We assume that beam interaction may happen as much as 100KHz for |z|<1m**
- dN_{ch}/dy = 180 (minbias Au+Au @ 200GeV) → 400 tracks in $|\eta|<1.1$
  - **Background and fakes effectively doubles the number of tracks; 800 tracks in the TPC**
- Raw rate: 940Gbits/s @ 100KHz
  - **Caveat: Radially-averaged rate**
  - **η dependent acceptance change is taken into account**



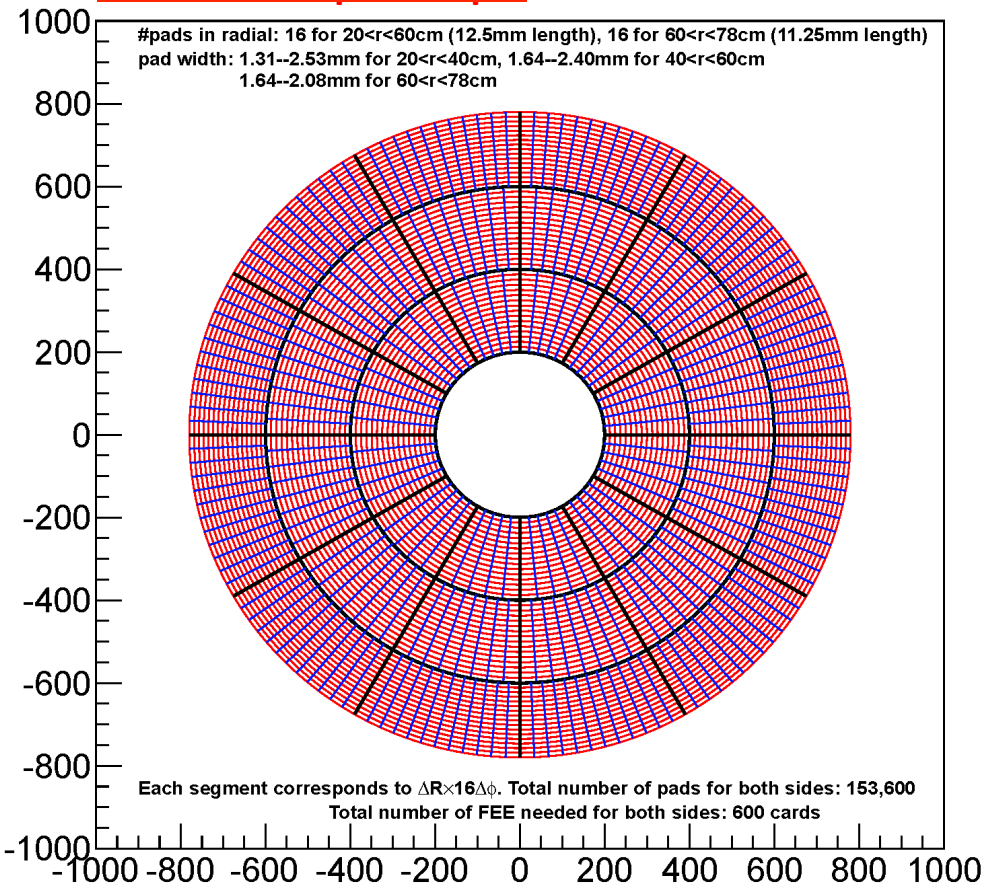


Padplane layout

- New pad layout (30<r<78cm)
  - **Three segments in radial direction, each divided into 16 (8 for 30<r<40cm)**
  - **12 segments in phi direction, each divided into multiple of 16**
  - **Matching to number of input to a FEE**
  - **Each cell in the right figure corresponds to 16 pads in phi**
- Variable pad size as a function of radial position
- Total 153,600 pads for both side
  - **600 FEE cards**
- Data Rate (no header included)
  - **1.42Gbps/board for 30<r<40cm**
  - **1.45Gbps/board for 40<r<60cm**
  - **0.77Gbps/board for 60<r<80cm**
  - **→ 28Gbps/(1/12 full azimuth)**

5 FEEs for 30<r<40cm, 8 for 40<r<60cm, 12 for 60<r<78cm, for each 1/12 of full azimuth

Each cell = 16pads in phi

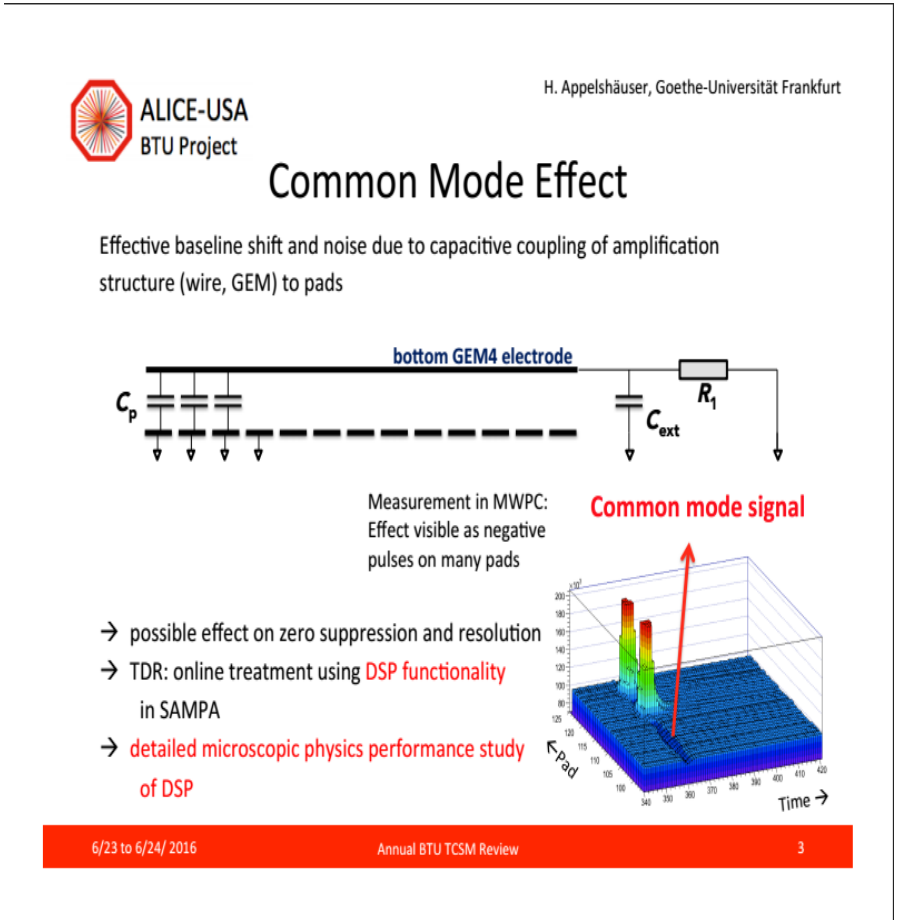


Data rate calculation

- Raw data (100% duty factor is assumed)
  - **Sampling rate in z-direction: 10MHz (= 100nsec)**
  - **Pulse peaking time is 160nsec (fixed from SAMPA's specification), which leads to ~350nsec for whole pulse shape.**
    - **More than 4 samples in timing (z) direction is necessary. We decided on taking 5 samples including pre-signal**
  - **One cluster will be spread over 3 pads in r-ϕ plane**
    - **Coming from the characteristics of the Ne2K (Ne - CF_4 - iC_4H_{10}: 95% - 3% - 2%) gas**
  - **We measure 40 clusters for one track**
  - **Each sample is 10 bits: 40 clusters * 15 * 10 bits = 6 Kbits/track**
  - **800 tracks per event: 6Kbits/track * 800 = 4.8 Mbits/event**
    - **This number doesn't take eta-dependent acceptance change of TPC into account**
  - **At 100 KHz: 4.8 Mbits/event * 100 KHz = 480 Gbits/s**
- With header of SAMPA (40% increase at maximum): 670Gbits/s
  - **With eta-dependent acceptance change: 940Gbits/s**

Common mode noise

- Common mode noise issue (ALICE found)



- Common Mode removal is what the on-board DSP for the SAMPA chip is designed to do.
  - But, this is within a chip, i.e. 32 ch
- The technique:
  - Find a large number of “empty channels”.
  - See if they all dip below zero together.
  - Correct everyone up by the amount of the dip.
- ALICE ended up with 5MHZ sampling instead of 10MHz in order to fit the bandwidth of GBTx
  - SAMPA itself can drain all the data