sPHENIX Director's Review
INTT

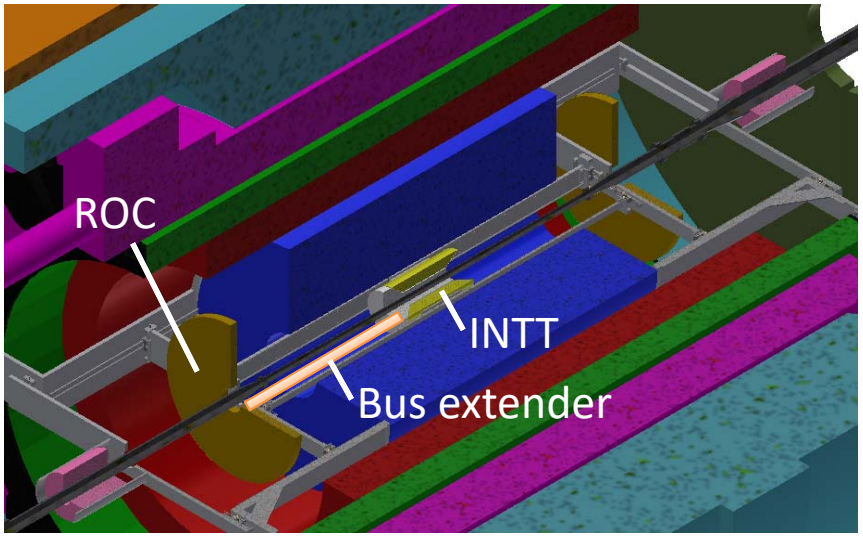
August 2-4, 2017

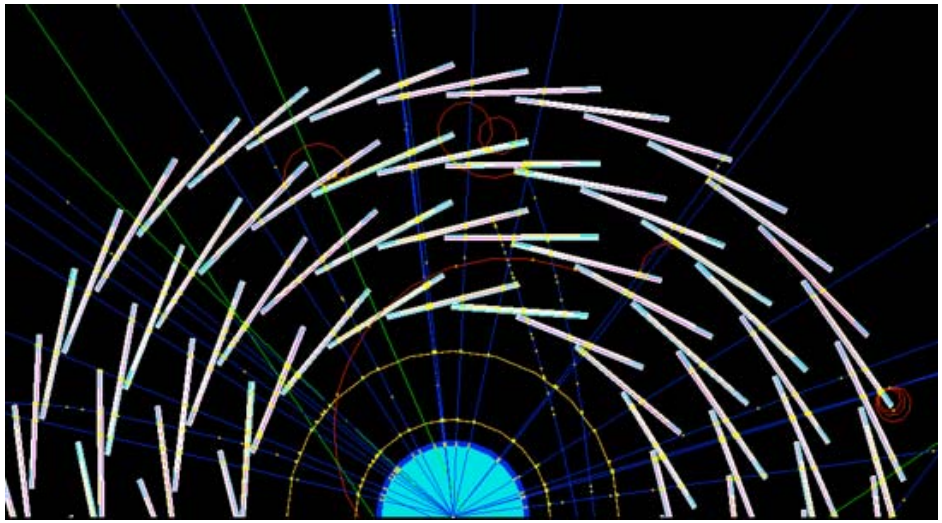
BNL

The Subsystem

Intermediate silicon tracking (INTT) adds to the robustness of pattern recognition, momentum reconstruction, and capability of high multiplicity trigger in a challenging environment of high luminosity and high multipliciy.

1. contribute unique association between inner and outer trackers
2. ensure both high track reconstruction efficiency and purity
3. azimuthal 2π and $|\eta| < 1.1$ coverages at $|z_{vtx}| < 10$ cm
4. our planes of strip detectors from Layer 0 to Layer 3
   - same readout chip and electronics as used in the PHENIX FVTX
   - cooling by air or high-thermal-conductivity-plate
   - maintain low material budget



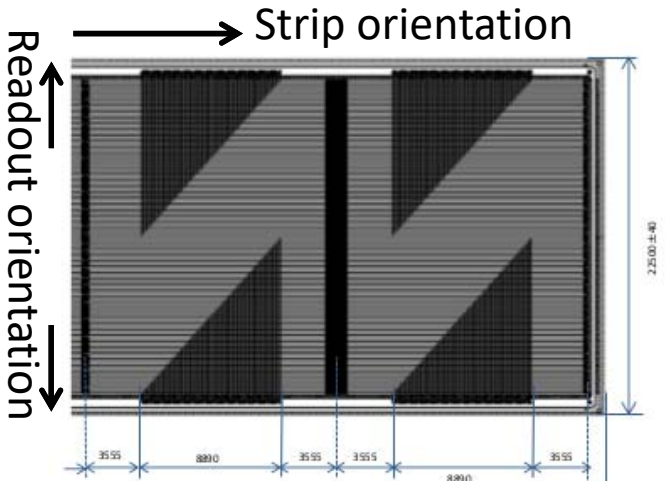


The Subsystem Technical Overview

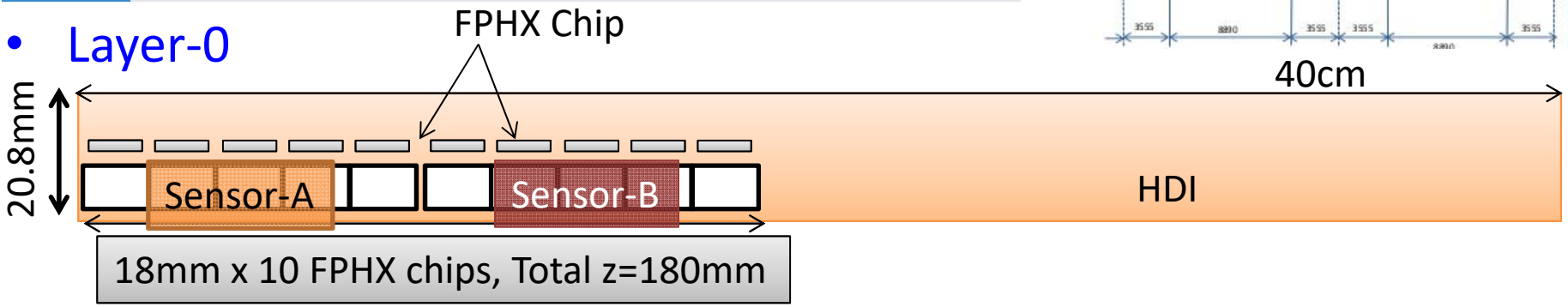
- Silicon Sensors
  - silicon strip sensors manufactured by Hamamatsu Photonics Co.
  - 78mm pitch strip sensors are oriented parallel to beam direction
  - Thickness (200 – 320μm) is under optimization.
- HDI
  - Same 7 layers design and layout as FVTX.
  - Less technological challenge in circuit wise (line width, pitch,etc) than FVTX's, but longer 40cm.
- Ladder
  - High thermal conductivity plate + air/liquid cooling is under development.
- Bus Extender
  - Long 1.3 meter (factor of 3 longer than FVTX's) is required due to spatial constraint where ROC can be located.
  - Technical challenge to establish by multilayered FPC.
- Readout Chip and Electronics
  - Reuse FVTX's FPHX chips and electronics.

Scope

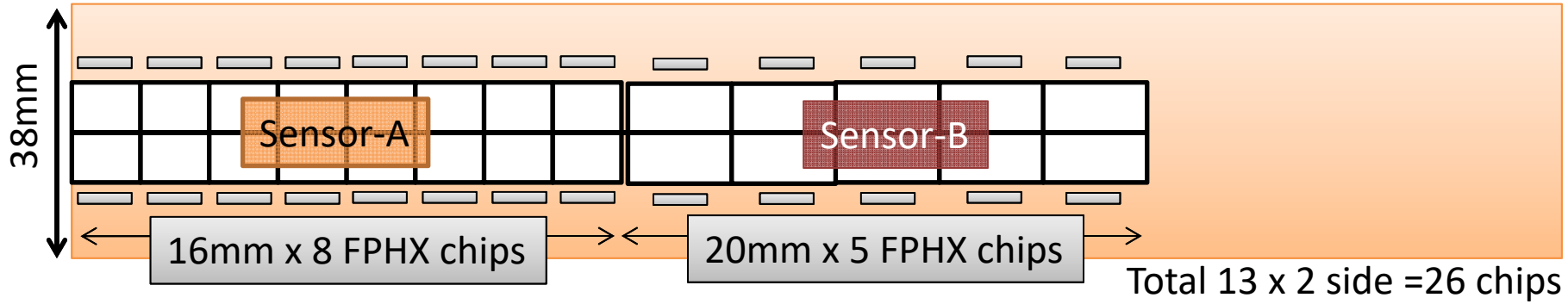
Layer	Radius (cm)	The number of ladders	Strip size (φ x z, mm)
0	6	48	0.078 x 18 (18)
1	8	26	0.086 x 16 (20)
2	10	32	0.086 x 16 (20)
3	12	38	0.086 x 16 (20)



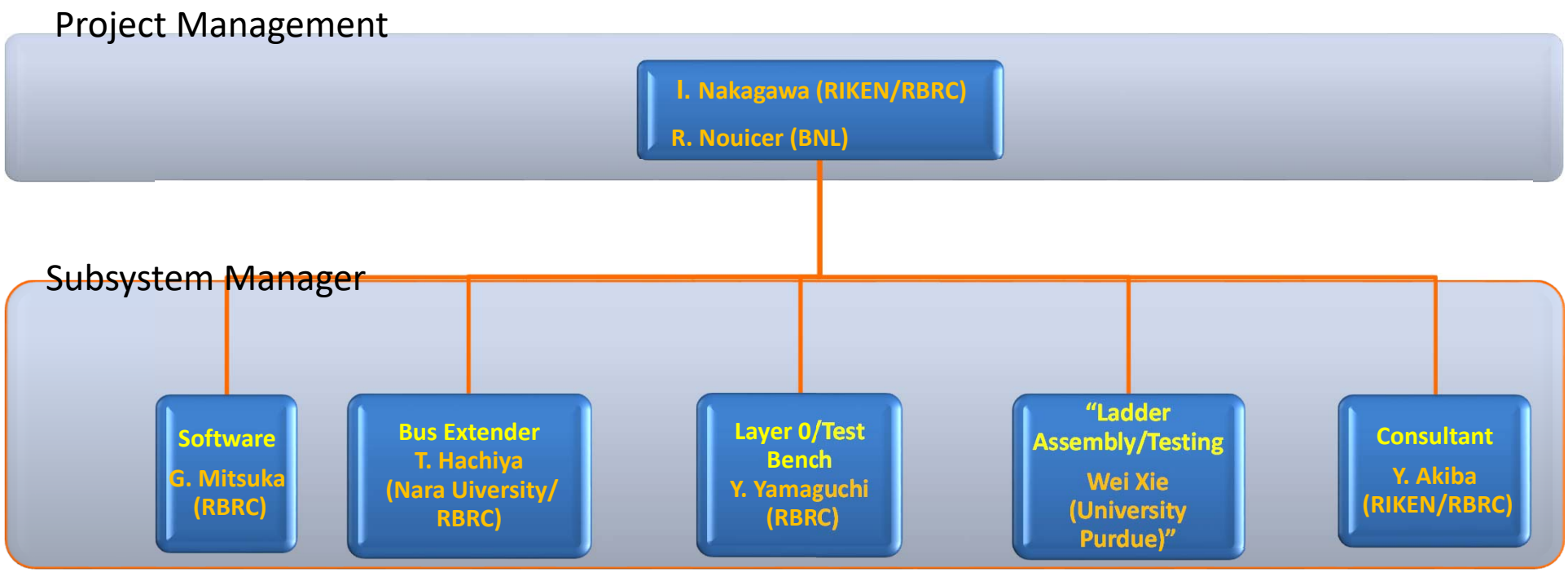
- Layer-0



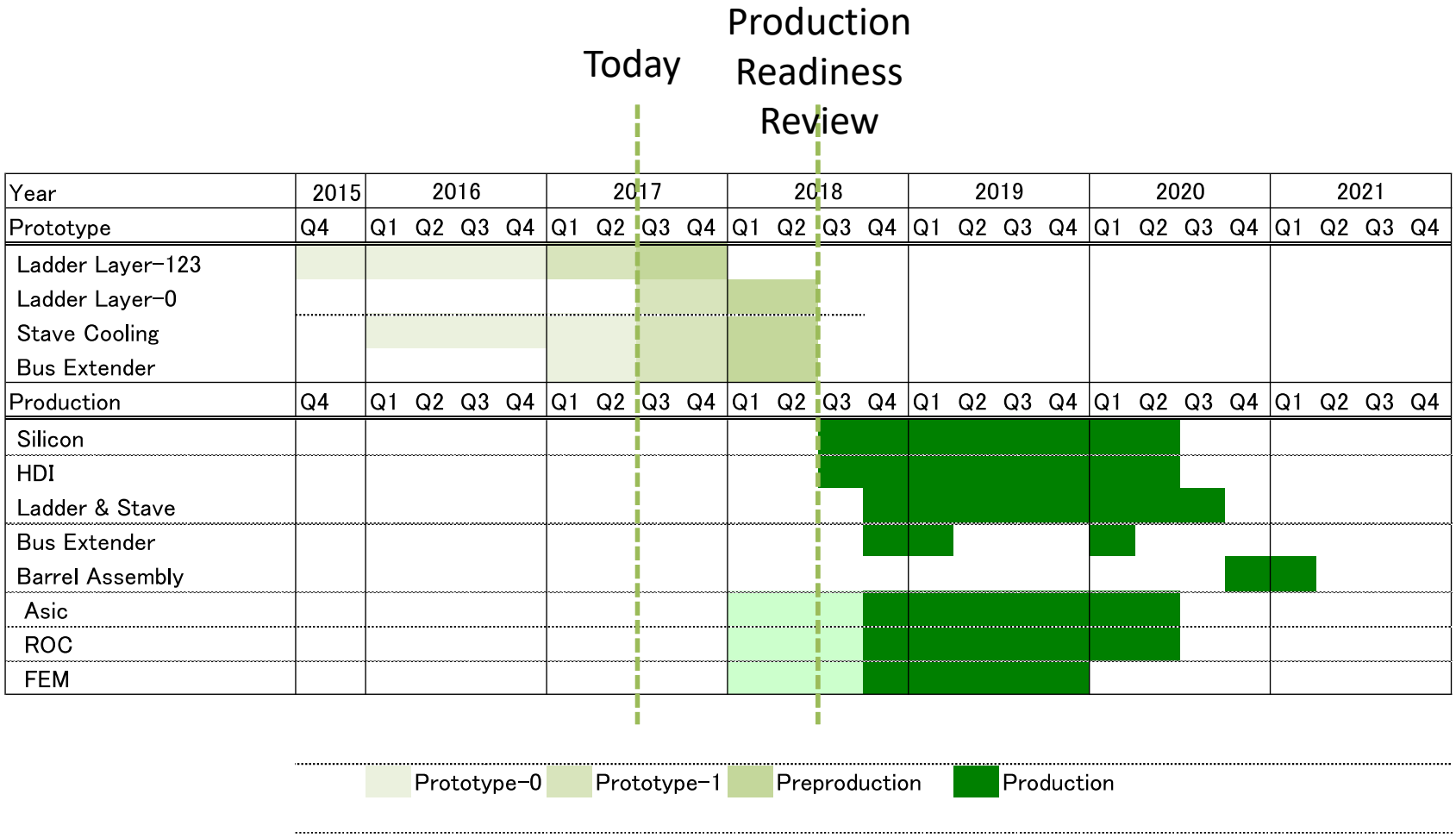
- Layer-1,2,3



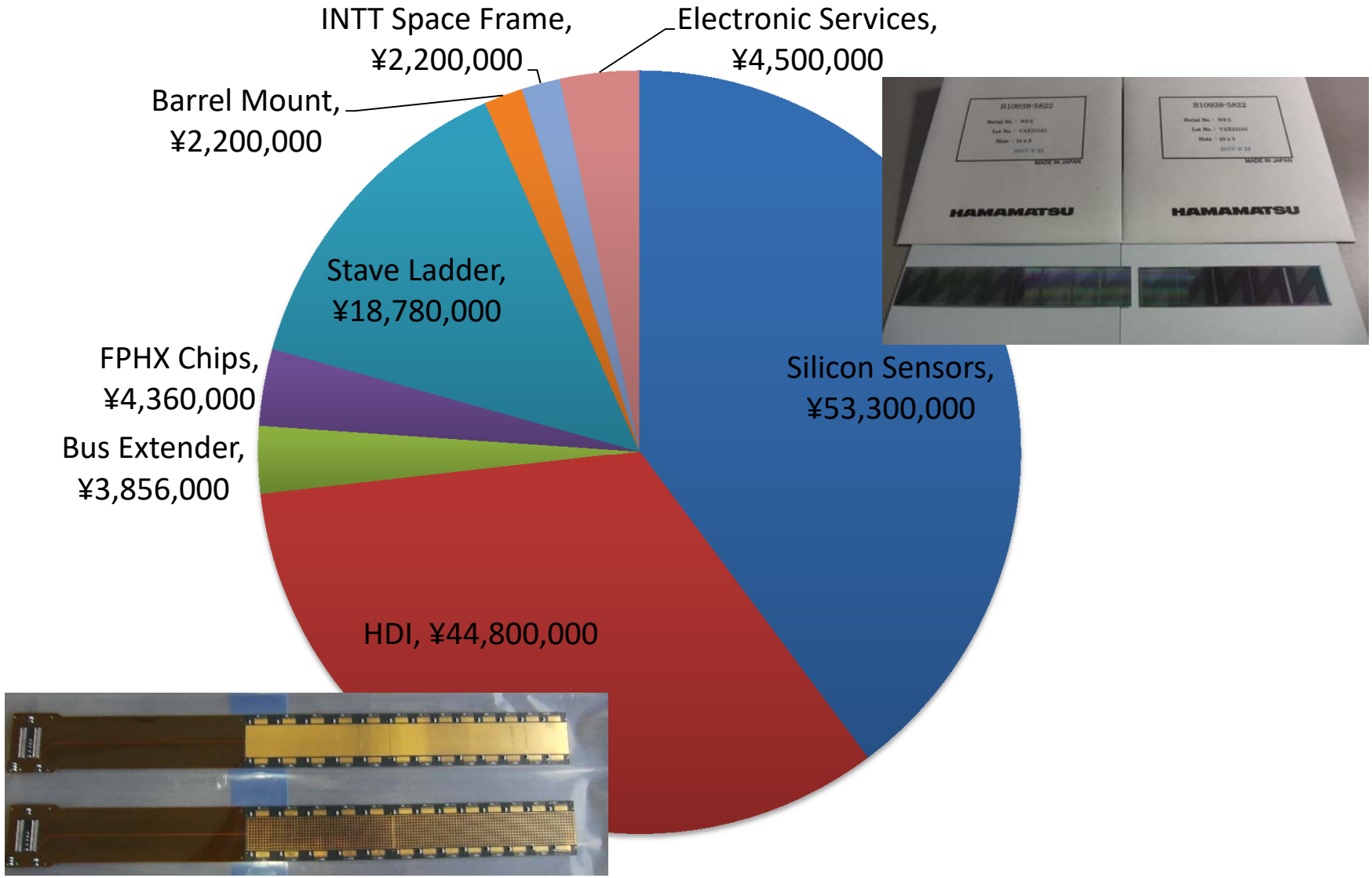
Subsystem Collaborators



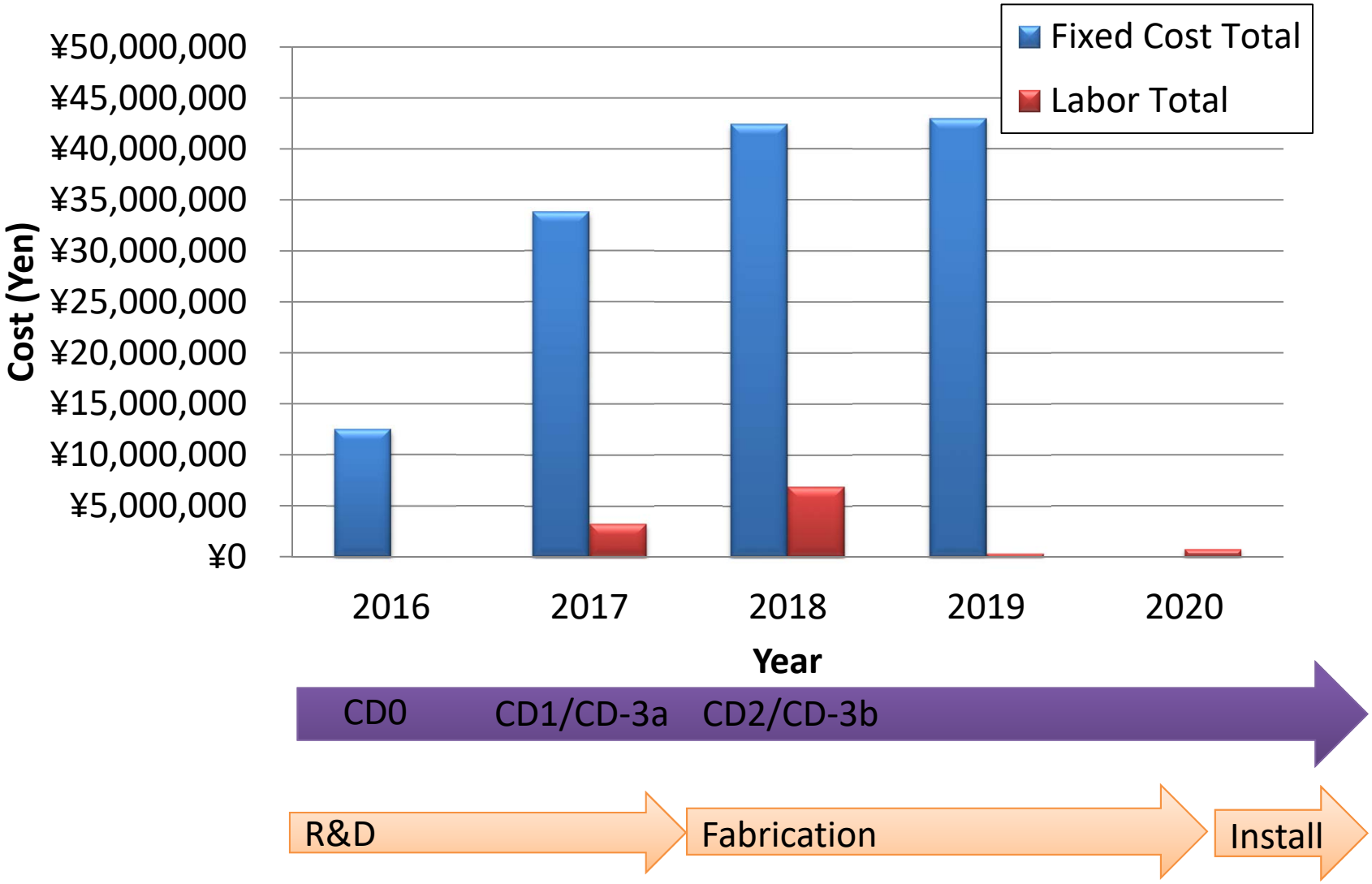
Schedule Drivers



Cost Drivers



Basis of Estimate and Resource-Loaded Schedule



Status and Highlights

3 prototype Silicon Ladders for Layer1,2,3 are assembled in BNL (June, 2017)

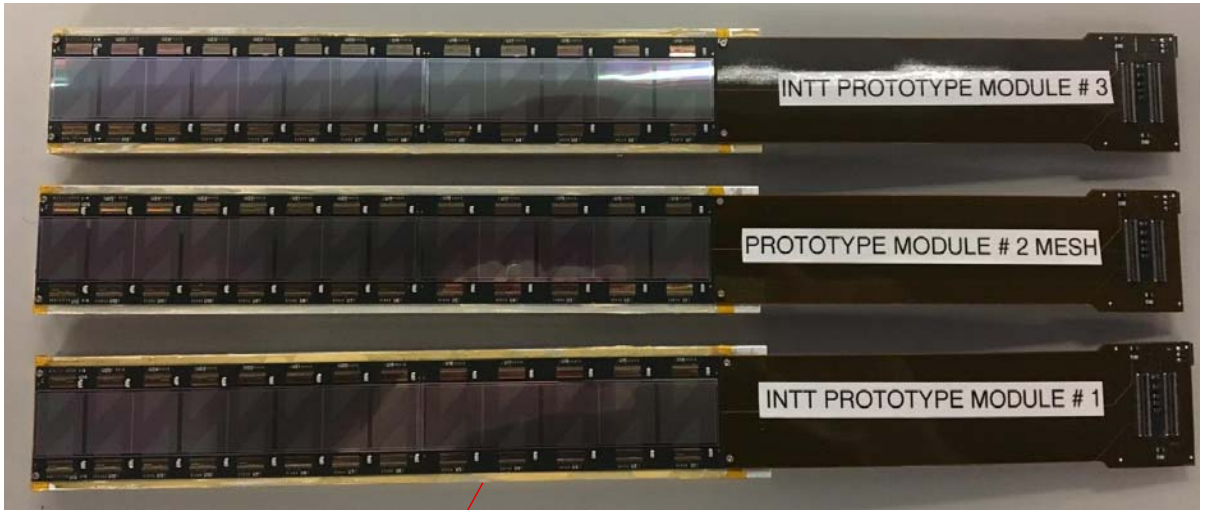
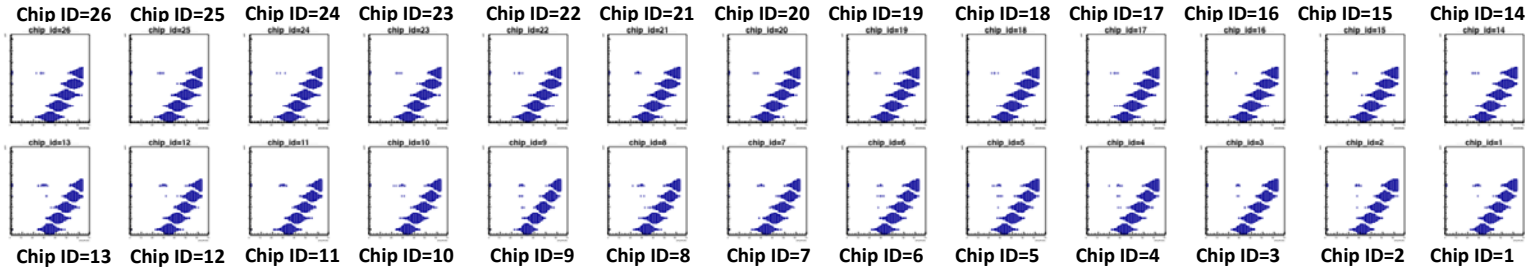


plate	Type-A	Type-B	V_{bias}	T_{front} & T_{back}	Note
solid	320∝m	320∝m	100V	T_{front}=20.3 T_{back}=26.5	Chip17: always dead. Chip21: No wire to sensor Light leak at front side

Overall response were confirmed to be good. Minor issues to be addressed.

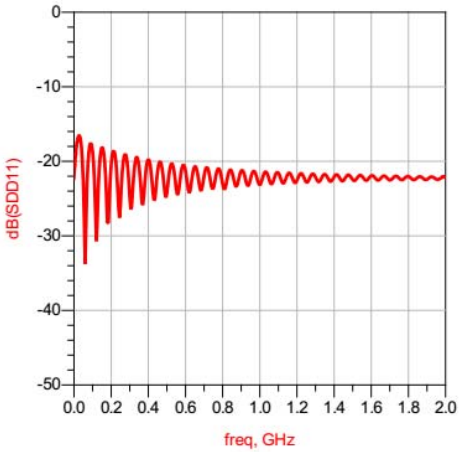
ADC vs pulse amplitude



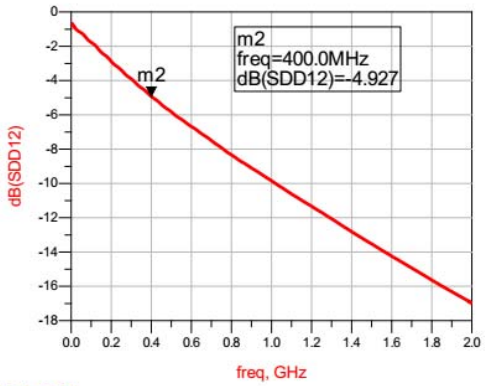
Good response between input calibration pulse and output ADC

Status and Highlights

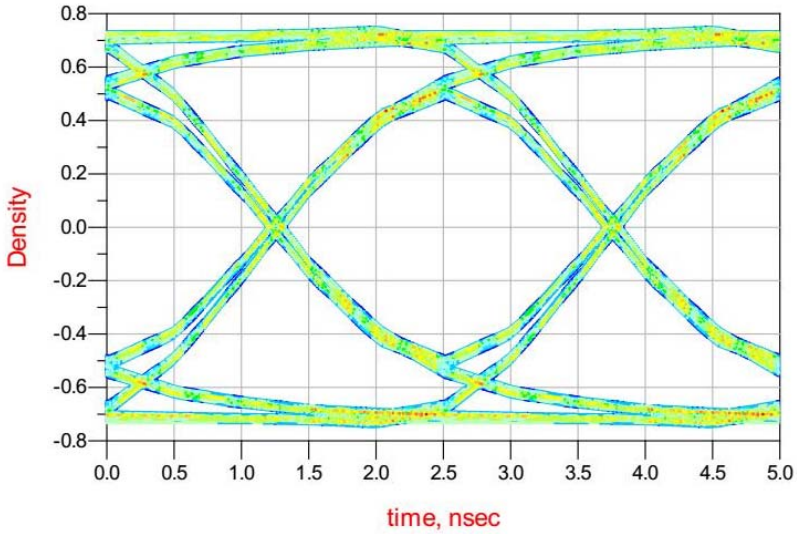
- Bus Extender
  - Electromagnetic field simulation study of 1.3m FPC is ongoing by Tokyo Metropolitan Industrial Technology Institute.



-5dB @ 4MHz



"DD"



  - R&D with a company who has an experience to manufacture a single layer 1.3m FPC.

Issues and Concerns or Summary

1. R&D status is on schedule.
2. No major issues are found in the ladder prototype for layer-1,2,3.

- Issues and concerns:

Bus Extender

- Multilayered 1.3 meter long bus extender by FPC hasn't been established yet.
- Longer the FPC, the wider line width and pitch are required, which leads massive cable and connectors.
- Engineering investigation is urgent how much space can be allocated for the bus extender and connectors within the spatial constraint between MVTX and TPC inner boundaries.

Cooling

- Heat transfer by high thermal conductivity plate over 20cm long HDI has not been established.
- Need to design full air/liquid cooling for additional material and complicated system as a trade off in case above doesn't work.