sPHENIX Director's Review
1.2.6 TPC Data Aggregator Module (DAM)

Jin Huang (BNL)

August 2-4, 2017

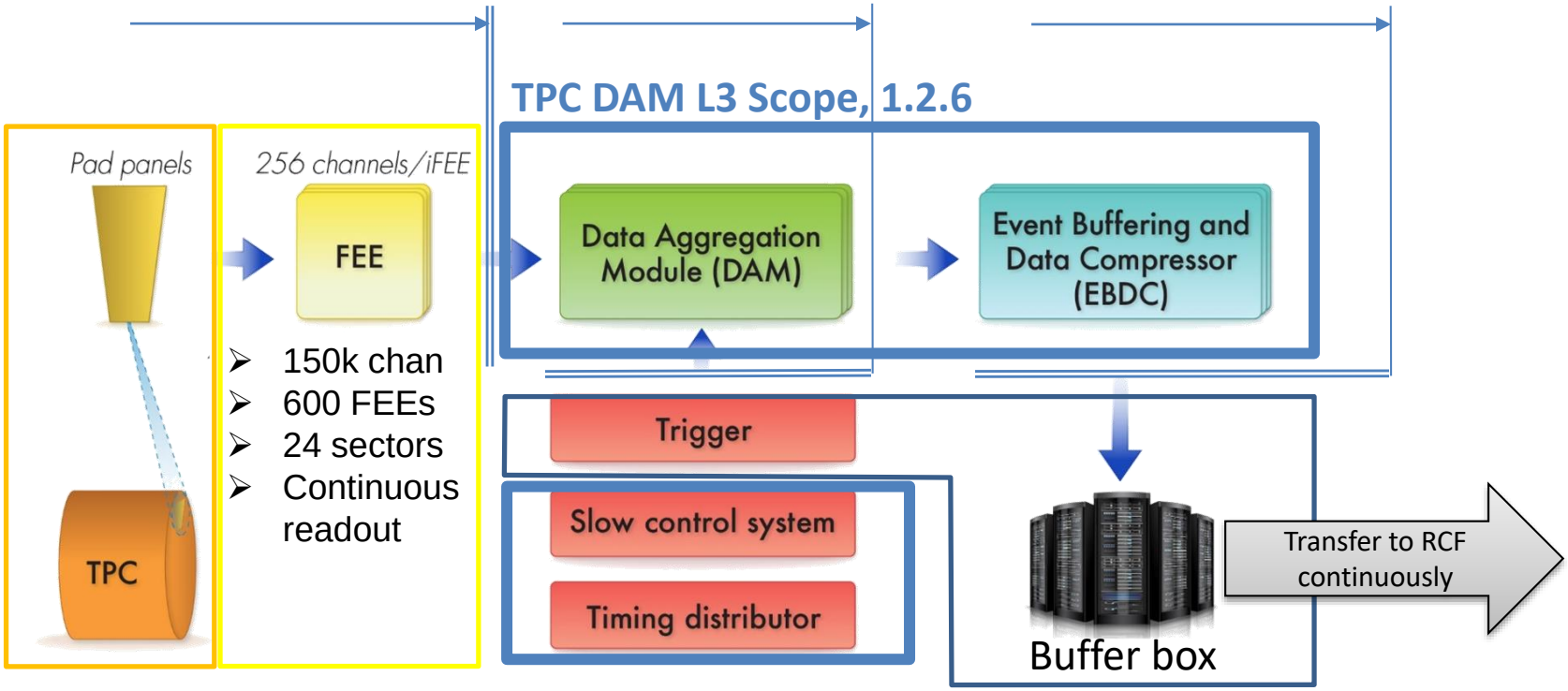
BNL

The Subsystem

Input data stream:
600 4+ Gbps bidirectional fibers links
Max continuous: 4 Gbps / fiber
Average continuous: 1.6 Gbps x 600 fibers

Clock/Trigger input:
Optical links
Clock = 9.4 MHz
Trigger Rate = 15 kHz

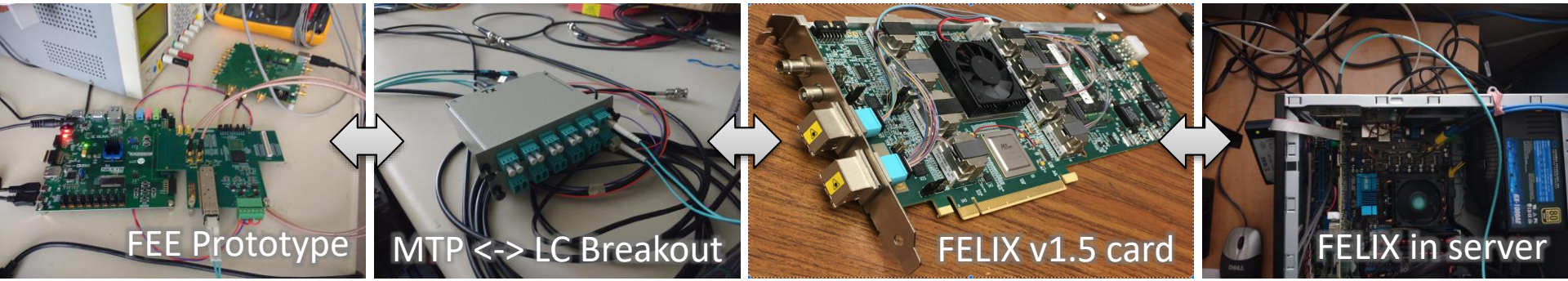
Output data stream to buffer box:
24 x 10 Gbps Ethernet via fiber
After FPGA based triggering and clustering
Total continuous output: 80 Gbps



The Subsystem Technical Overview

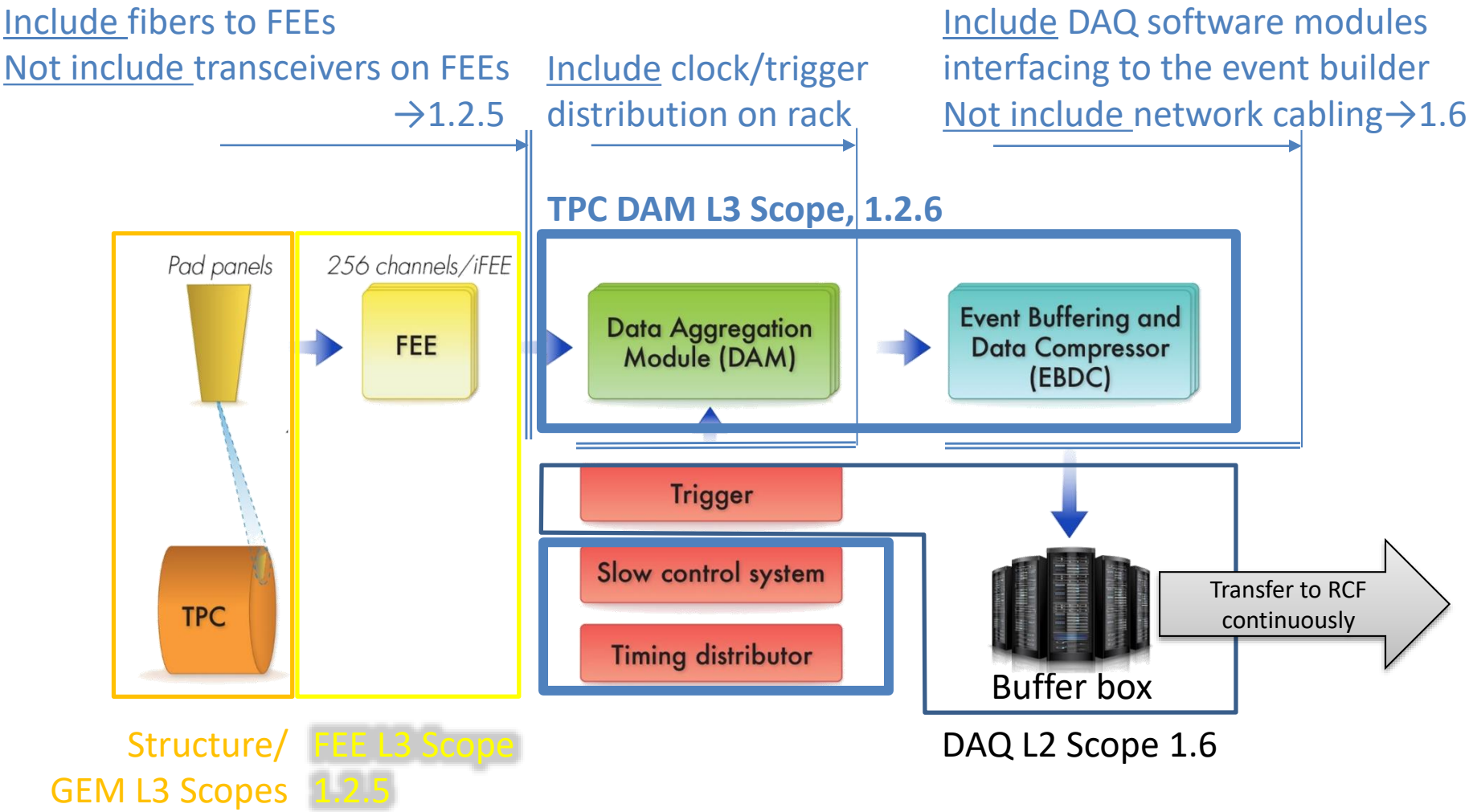
- Collect data from 600 bi-directional 4+ Gbps fiber links to FEEs at rate of 940 Gbps
- Reducing data via triggering, clustering and compression to reduce data to 80 Gbps
- Driven to use large-FPGA based data acquisition cards with multi-10Gbps input and PCIe Gen3 output, hosted on commodity servers.
  - **Similar architecture adopted for ATLAS, LHCb, ALICE upgrade for 2020+**
- Default implementation taking advantage of BNL-developed FELIX PCIe card
  - **48-bidirectional 10 Gbps optical link (require 25 bidirectional link @ 4 Gbps)**
  - **A large FPGA: Xlinx Ultrascale (XCKU115), optimizing cost/link**
  - **PCIe Gen3 x16 link to server, demonstrated to 101 Gbps (require >10 Gbps)**

FELIX Prototype v1.5 card (borrowed from BNL/ATLAS group) used in TPC test stand already



Scope

- Data Aggregation Modules (DAM) + Event Buffering and Data Compressor (EBDC) servers
- Timing trigger distribution on DAM/EBDC server rack in DAQ room
- Interfaces detailed as following:

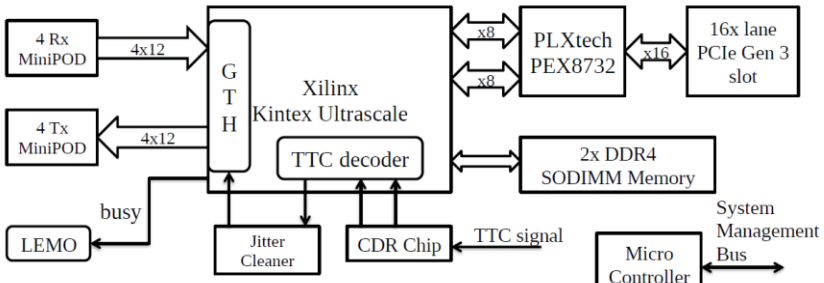


Subsystem Collaborators

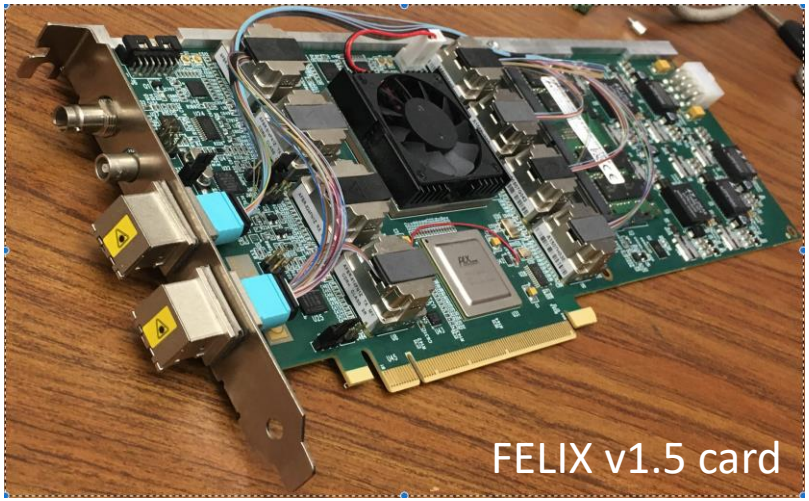
- Jin Huang (BNL/Physics) CAM
  - **Associate Physicist, heavy-flavor topical group co-convener**
  - **Past projects highlight: commissioned DAQ for PHENIX forward silicon tracker, a successful upgrade @ RHIC featuring 2-Tbps continuous readout**
- John Kuczewski (BNL/Instrumentation Division)
  - **Experienced digital developer**
  - **Expert of development for electronics, FPGA and drivers**
  - **Past projects highlight: LSST CCD readout electronics**
- Joe Mead (BNL/Instrumentation Division)
  - **Senior engineer**
  - **25 years experience in designing high speed electronic circuitry, embedded systems, and DAQ systems for high-energy/nuclear physics and neutron/photon applications**
  - **Past projects highlight: designer of timing system for the PHENIX experiment; ATLAS LAr Calor. Readout; Neutron Detector DAQ**
- Joint development with TPC FEE (WBS 1.2.5) and DAQ (WBS 1.6)

Synergistic collaboration

- In close collaboration with BNL Physics Omega group:
  - **Developed the BNL-711 PCIe card, which is chosen for ATLAS FELIX project, and used in ATLAS phase I upgrade and forward**
  - **Leading the finalization of FELIX PCIe card design**
- Sharing resource in FELIX development:
  - **Lend us a FELIX v1.5 card for prototyping**
  - **Sharing firmware blocks and PCIe driver software**
  - **Consultation**
- Feedback on FELIX v2.0 timing mezzanine design

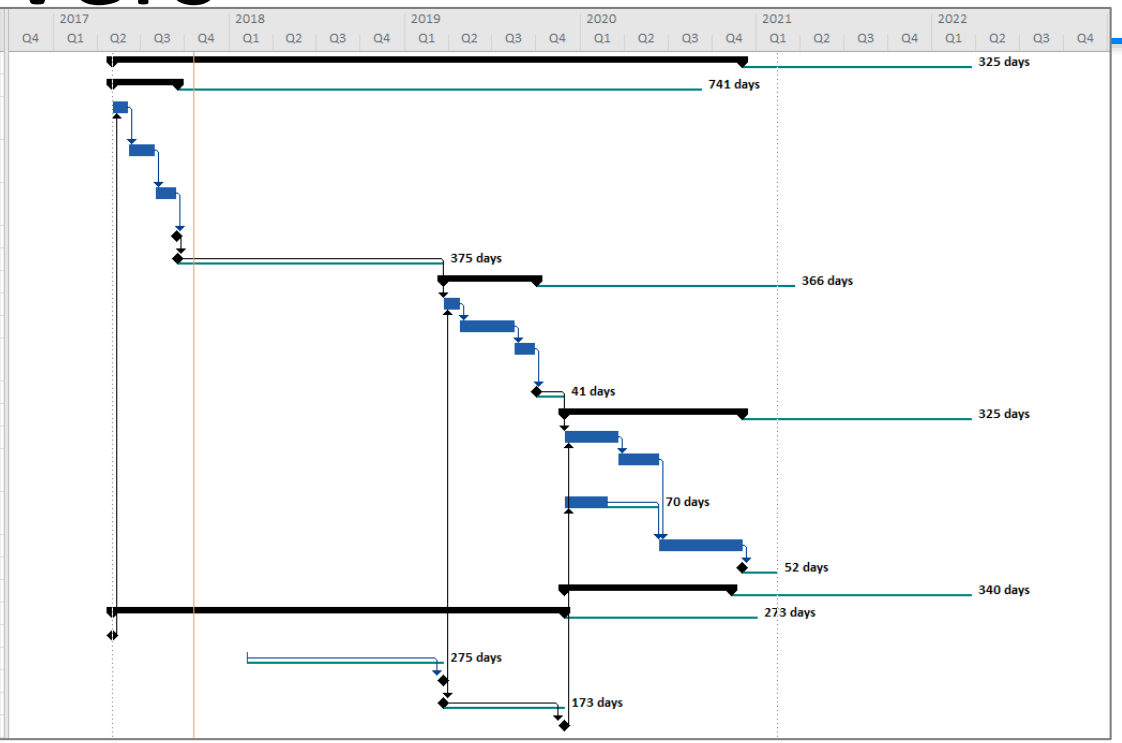


FELIX v1.5 internal diagrams



Schedule Drivers

Name	Levelir Delay	Duration
TPC DAM	**0 edays**	**894 days**
TPC DAM Evaluation --FELIX 1.5	**0 edays**	**96 days**
Write Design Spec for TPC DAM prototype v1	0 edays	22 days
Develop TPC DAM prototype v1 Test Stand	0 edays	40 days
Measure TPC DAM prototype v1 Throughput	0 edays	30 days
TPC DAM Safety Review	0 edays	0 days
TPC DAM Design Review	0 edays	0 days
TPC DAM Evaluation -- FELIX 2.0	**0 edays**	**132 days**
Procure FELIX 2.0 board for TPC DAM	0 edays	20 days
Develop TPC DAM FPGA Algorithm	0 edays	80 days
Measure Throughput of FELIX 2.0 for TPC DAM	0 edays	30 days
TPC DAM Production Readiness Review	0 edays	0 days
TPC DAM Production	**0 edays**	**250 days**
Procure TPC DAM Felix 2.0 boards	0 edays	75 days
Perform QA Testing on TPC DAM FELIX 2.0 boards	0 edays	55 days
Procure of TPC EDBC Computers and Peripherals	0 edays	60 days
Test Full TPC DAM System	0 edays	120 days
TPC DAM Production Ends	0 edays	0 days
TPC Support Systems	**0 edays**	**235 days**
Tracker Management	**0 edays**	**644 days**
CD-0 Authorization	0 edays	0 days
CD-1, CD-2a/CD-3a Review	0 edays	3 days
CD-1, CD-2a/CD-3a Authorization	0 edays	0 days
CD-2b/CD-3b Review	0 edays	0 days
CD-2b/CD-3b Authorization	0 edays	0 days



- Q3 FY19: Complete DAM implementation & Test: DAM production readiness review: Q4 FY19
- Q4 FY19 – Q4 FY20 : Procurement & Test
- 320-day schedule float: NOT on critical path
- Scheduling risk for FELIX card production is low:
  - **Already received v1.5 prototype card for the prototyping stage, 1.2.6.1**
  - **After the planned installation of ATLAS Phase-I upgrade (planned delivery @ end 2018, one year *prior* our procurement)**
  - **In the very unlikely case that ATLAS FELIX project were to be significantly delayed, we would use the *existing* FELIX v1.5 design for TPC DAM production**
- Scheduling risk for EBDC server production is low:
  - **Commodity computing**
  - **Procurement scheduled at the latest stage of the production to take advantage of commercial computing development**

Cost Drivers

- FELIX PCIe card: 230k$ + 25% contingency
  - **24 cards + 20% spare @ 8k / card**
  - **Driven by FPGA cost**
- Commodity server: 187k$ + 40% contingency
  - **2U 24-core server supporting full size PCIe Gen3 x16 + SMBus**
  - **24 servers + 20% spare @ 6.5k / server**
  - **40% Contingency assigned due to the uncertainty of number of CPU cores required for data compression.**
  - **Contingency band will reduce as prototyping, algorithm development and test with simulated FELIX output data.**
- Next leading cost - data fibers based on quote: 76k$ + 20% cont.

Navigate through BOE 1.2.6

sPHENIX Detector
Relativistic Heavy Ion Collider
BASIS of ESTIMATE (BoE)

L2 Project Name	L2 WBS Number	L3 Project Name (Control Account)	L3 WBS Number
Time Projection Chamber	1.2	TPC DAM	1.2.6

Work Package Name	WBS Number	Basis of Estimate Link
TPC DAM Evaluation -- FELIX 1.5	1.2.6.1	TPC DAM Evaluation --FELIX 1.5
TPC DAM Evaluation -- FELIX 2.0	1.2.6.2	TPC DAM Evaluation -- FELIX 2.0
TPC DAM Production	1.2.6.3	TPC DAM Production

Item	Vendor	Total	Status	Basis of Estimate	Contingency	Item Contingency	Wt Contingency	Total	Contingency	Total w/
							0.21	$306,001	$62,738	
FELIX Production PCIe cards, 24cnt + 20% spare	BNL ATLAS DAQ Group	$229,879	Pending	Unofficial quote	0.21	$47,513.43				
48-fiber MTP (M)-MTP (F) cable 5m, 2x48cnt + 20% spare	Computer Crafts Inc.	$32,026	Pending	Quote: CCI/T40418PF48-005	0.20	$6,405.12				
48-fiber MTP (F)-MTP (F) cable 58m, 48cnt + 20% spare	Computer Crafts Inc.	$35,424	Pending	Quote: CCI/T40408PF48-058	0.20	$7,084.80				
1U 19" 12 port MPO feedthru panel with 12X MPO couplers, 2x4+25% spare	Computer Crafts Inc.	$720	Pending	Quote: CCI/56348-MT	0.20	$144.00				
48F MTP(M) - LC Hydra assembly, 48cnt + 20% spare	Computer Crafts Inc.	$7,822	Pending	Quote: CCI/100	0.20	$1,564.42				
MTP Coupler, 48cnt + 20% spare	Computer Crafts Inc.	$130	Pending	Quote: CCI/100	0.20	$25.92				
							0.39	$205,901	$81,188	
2U rack servers, 24cnt + 20% spare	Microway	$187,200	Pending	Experience, Requ	0.40	$74,880.00				
TPC timing distribution board - PCB, 1cnt + 1 spare	Many	$400	Pending	Experience	0.40	$160.00				
TPC timing mezzanine - PCB, 24cnt + 20% spare	Many	$1,440	Pending	Experience	0.40	$576.00				
SFP+ Optical TX/RX, 48cnt + 20% spare	Avnet	$5,213	Pending	Catalog: AFBR-709DMZ	0.20	$1,042.50				
LC duplex fiber, 48cnt + 20% spare	Computer Crafts Inc.	$648	Pending	Quote: CCI/F26268P302-001	0.20	$129.60				
SMT Chip Resistor Capacitor	Digikey	$1,000	Pending	Experience	0.40	$400.00				
Peripheral accessories and cables	Many	$10,000	Pending	Experience	0.40	$4,000.00				

Computer Crafts, Inc
57 Thomas Rd, P.O. Box 644
Hawthorne, NJ 07507-0644
USA
Phone: (973) 423-3500
Fax (973) 423-9536

SALES QUOTE SQ17038

Prepared By: John Fox
Date: 3/30/2017

Customer: Brookhaven National Labs
Customer Contact: Jin HUANG

Dear: Jin HUANG,
Thank You for your interest in our products. We are pleased to provide you with a following quotation.

Line	Part Number	Delivery (ARO)	QTY	UoM	Unit Price	Extended Price
1	CCI/100176	2 weeks	750	EA	$1.85	$1,387.50
	COUPLER LC/LC Duplex, Aqua, Zirconia Sleeve, No Logo, RoHS and EU REACH Compliant.					
2	CCI/F26268P302-001	28 days	750	EA	$11.25	$8,437.50
	LC to LC duplex Uni-Boot, 2mm OM3 Aqua, 1 meter length					
3	CCI/F32358D48-0.5	28 Days	45	EA	$135.00	$6,075.00
	48 fiber MTP(M) with reduced spring push (1.3") to (4") Prizm nonpeelable OM3 ribbon fiber. 0.5M					
4	CCI/T40408PF48-058	28 Days	60	EA	$615.00	$36,900.00
	48F MTP(F) to 48F MTP(F) on OM3 3.8mm round aqua jacket Cable. Polarity straight (1-1, 48-48) 75 meter length on a collapsible reel					
5	CCI/56745-48MT-OM3	28 Days	60	EA	$262.20	$15,732.00
	24X LC Duplex to 48F MTP(M) Cassette. OM3					
6	CCI/1000450-18I-48F	28 days	30	EA	$135.80	$4,074.00
	48F MTP(M) - LC Hydra assembly 900um OM3 18" length					
7	CCI/HSQ8P-52NBN-4203N-001M	28 Days	60	EA	$219.00	$13,140.00
	48F MTP(M) to 4X 12F MTP(F) 50/125 OM3 on 3.0mm OFNP round jackets. 1 meter breakout, 1 meter overall length.					
8	CCI/BSF8P-43NBN-1603N-001M	28 Days	150	EA	$118.00	$17,700.00
	12F MTP(M) to 6X LC Duplex, 2mm zipcord OM3, 1 meter breakout, 1 meter length.					
9	CCI/56340-AQ	28 Days	150	EA	$136.50	$20,475.00
	12 FIBER MTP(M) TO LC HYDRA INSIDE A CASSETTE, MT COUPLER TO 6X DUPLEX LC COUPLERS					

sPHENIX Detector
Relativistic Heavy Ion Collider
BASIS of ESTIMATE (BoE)

Date of Est: 3/1/2017
Prepared By: Jin Huang
DocNo. (refer Rev. Log)

Work Package Name	WBS Number:	Control Account Number
TPC DAM Production	1.2.6.3	

WBS Dictionary Definition:

TECHNICAL SCOPE:
CONTAINS ALL TASKS WHICH ARE REQUIRED TO PRODUCE THE DAM FOR THE TPC.
WORK STATEMENT:
PROCURE ALL PARTS AND PERFOM QA TESTING FOR THE FINAL TPC DAM.

Estimate Type (check all that apply):

- ___ Work Complete
- ___ Existing Purchase Order
- X Catalog Listing or Industrial Construction Database
- ___ Documented Vendor Quotation based on Drawings/Sketches/Specifications
- ___ Budgetary Estimate by Vendor/Fabricator based on Sketches, Drawings, or other Written Correspondence
- X Engineering Estimate based on Similar Items or Procedures
- ___ Engineering Estimate based on Analysis
- X Expert Opinion

Assumptions Used in Developing Estimate

We assume that FELIX production 2.0 version will suit our needs. Furthermore, we assume that we will require one FELIX card per TPC sector, housed in its own high speed PC. Costs for the 12 core rack servers are included in the scope of this WBS rather than as a part of infrastructure. Additionally, we carry partial costs of the timing distributuion system as appropriate for our system's fractional load.

Details of the Base Estimate (Explanation of the Work)

The estimate includes production, quality assurance, and installation of the DAM system. Fiber costs are born in this WBS rather than in the TPC FEE to which the DAM module is connected.

Cost Summary

(follow link for detailed summary)

Entries into the detailed cost summary have been color coded based upon the apropriate level iof contingency that is applied to the item with green being the lowest contingency and red being the highest. The cost before contingency and with contingency are summarized below.

Task	Cost	Cost + Contingency
Procure TPC DAM Felix 2.0 boards	$ 306,000.58	$ 368,738.27
Procure of TPC EDBC Computers and Peripherals	$ 205,900.51	$ 287,088.61
Total	$ 511,901.09	$ 655,826.88

Contingency

The contingency has been evaluated independently for each line items in accord with the standard sPHENIX contingency guidelines. Contingencies spread over several items are weighted by item cost to determine a summary contingency for each WBS entry. We have used guidance from ATLAS to set the FELIX board contingency at 25% and all other components of the final DAM module production are set to 40% contingency.

Basis of Estimate and Resource-Loaded Schedule

- FELIX PCIe card: 230k$ + 25% contingency
  - **Assume final FELIX production card production is ready at our schedule**
    - **Well into final prototyping stage, producing pre-production card as speaking**
    - **Planned for production of ATLAS Phase-I upgrade (delivery end 2018)**
- Commodity server: 187k$ + 40% contingency
  - **6.5k / server based on online catalog quote @ DELL and expert's experience with procurement of scientific computing**
- Next leading cost - data fibers based on quote: 76k$ + 20% cont.
  - **Fiber distribution designed:**
    - **48-fiber trunk + patch panels from DAQ room to exp. Hall**
    - **48 MTP-> LC duplex breakout on TPC**
  - **Quoted each part from Computer Crafts, Inc.**

BOE WBS 1.2.6 TPC DAM, sheet Production -- Details

Item	Vendor	Total	Status	Basis of Estimate	Contingency	Item Contingency	Wt Contingency	Total	Contingency	Total w/ Contingency	Grand Total	Grand Total w/ Contingency
											$511,901	$655,827
							0.21	$306,001	$62,738	$368,738		
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MTP Coupler, 48cnt + 20% spare	Computer Crafts Inc.	$130	Pending	Quote: CCI/100106	0.20	$25.92						
							0.39	$205,901	$81,188	$287,089		
2U rack servers, 24cnt + 20% spare	Microway	$187,200	Pending	Experience, Require R&D for spec	0.40	$74,880.00						
TPC timing distribution board - PCB, 1cnt + 1 spare	Many	$400	Pending	Experience	0.40	$160.00						
TPC timing mezzanine - PCB, 24cnt + 20% spare	Many	$1,440	Pending	Experience	0.40	$576.00						
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SMT Chip Resistor Capacitor	Digikey	$1,000	Pending	Experience	0.40	$400.00						
Peripheral accessories and cables	Many	$10,000	Pending	Experience	0.40	$4,000.00						

Risk Registry

- **No item** in TPC DAM 1.2.6 is considered risky.
- Relates to **moderate risk** to the downstream DAQ/storage risk (WBS 1.6 DAQ)

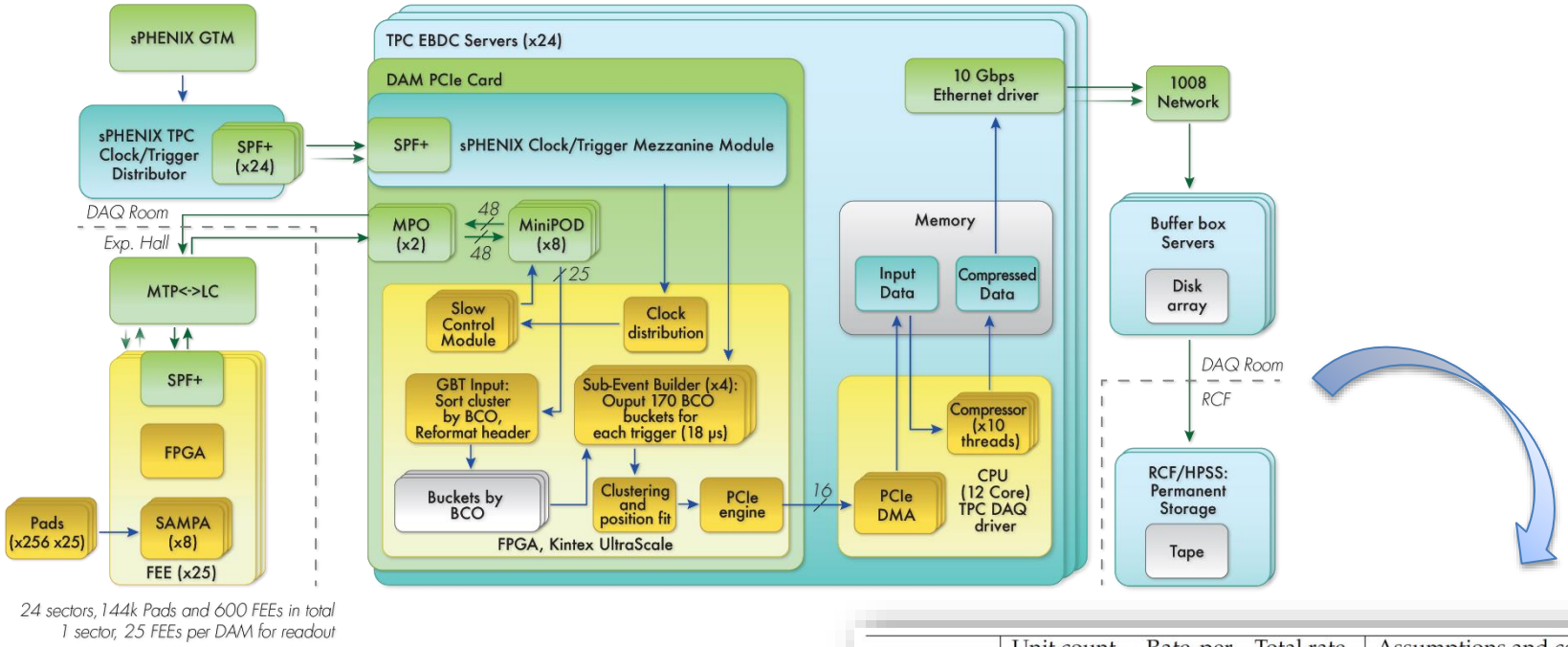
Risk registry, TPC WBS 1.2

T. Hemmick	1.2 TPC	Procure v1a GEMs	Delivery date on v1-shapes GEMs leaves less than one month before magnet test.	The test will require that we use existing GEMs which will be 10x10cm^2. This will require a special module to adapt the smaller square GEMs to the	R&D Phase	20%	Cost $10k for square-GEM adapter parts	Low	In case the proper GEMs for the v1a prototype are not in hand, an adapter plate will be requires to fit an existing GEM-stack to allow the magnet test to proceed.
T. Hemmick	1.2 TPC	Performance failure of v2 prototype	The v2 prototype fails in any performance criterion that requires more thasn trivial re-design.	If the v2 prototype fails, then there will need to be a v3 prototype added to the cycle.	R&D phase	5%	Schedule: 2 months of float lost. Cost:$15k (only gain	Moderate	We will add a design cycle of a smaller device than the full sized field cage if the v1 prototype fails. We will proceed on v2 only after success of the small version.
T. Hemmick	1.2 TPC	Failure or delay of CERN production	Factories wait upon GEM foil delivery and suffer schedule shifts.	The factory production of modules is critical path and will directly affect schedule.	production	10%	Schedule: 3-5 months	Moderate	We will monitor carefully the success of CERN foil production and will hire a technician who will exclusively work on producing GEM foils for our project. If delays still occur, we will seek a second vendor.
T. Hemmick	1.2 TPC	SAMPA Chip Failure	SAMPA chips fail to match performance specifications.	Affects delivery of the TPC since FEE must be applied before delivery.	production	2%	Schedule: Unknown since mediation	Moderate	ALICE and STAR shall be forced to mitigate the situation and if not, alternatives such as the sALTRO and DREAM chips must be considered.

Risk registry, DAQ WBS 1.6. See talk DAQ/Trigger by Dr. Martin Purschke

M. Purschke	1.6 DAQ/Trigger	Storage	The TPC or other subsystem cannot meet	Data volume, especially from the TPC, too high	Production	Moderate 30%	cost ($100K)	Moderate	Invest in more local storage, change compression algorithms

Status and Highlights: Design



24 sectors, 144k Pads and 600 FEEs in total
1 sector, 25 FEEs per DAM for readout

For each one of the 24 TPC Sectors,

- 25 FEEs with 1 SPF+/FEE
- 12 LC duplex <-> 48F MTP on TPC cage
- 2x 48F MTP connect TPC cage <-> DAM
- Readout by 1 FELIX PCIe Card
- Hosted on 1 server

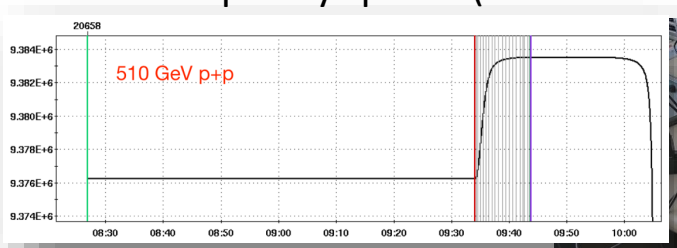
Implementing the design in DAQ test stand

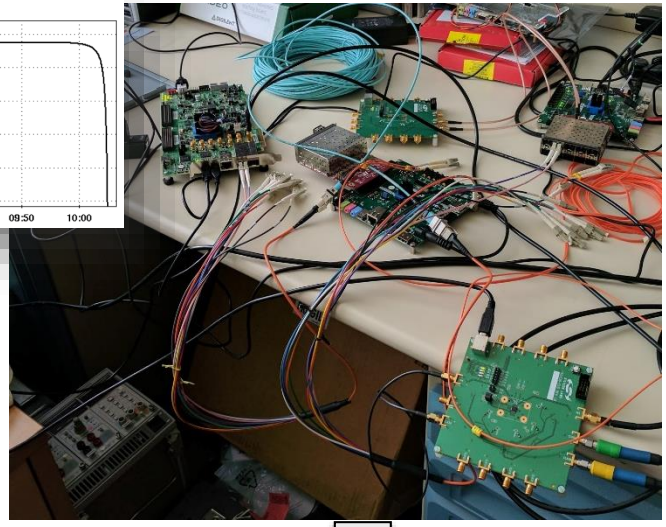
	Unit count	Rate per unit	Total rate	Assumptions and comments
Data on FEE Fibers	600 fibers	1.6 Gbps	940 Gbps	100kHz Au+Au collision assumed. Rate is radial position dependent. The max data rate is 2 Gbps for the inner-radius FEEs.
Data in BCO-buckets	24 DAMs	40 Gbps	970 Gbps	Unpack SAMPA data and add two 10-bit header per wavelet
After triggering	24 DAMs	11 Gbps	280 Gbps	Event builder collect 170-BCO buckets of hits after each trigger. This reduce data to 29%
After clustering	24 DAMs	5.7 Gbps	140 Gbps	Cluster finding and fitting on DAM FPGA. Expecting a reduction of total data volume to 50% based on STAR and ALICE experience.
After compression	24 EBDCs	3.4 Gbps	80 Gbps	Lossless compression on EBDC CPUs. Assuming the PHENIX experience of a reduction of total data volume to 60%
Buffer box data logging	Buffer box system	80 Gbps	80 Gbps	Logging TPC data to disk in buffer box system in sPHENIX counting house.

Status and Highlights: Test Stand

Function generator mimic repeated RHIC clock ramping (triangle pattern)

RHIC frequency spread (due to ramp) is large, 9.362 MHz ±22 kHz





DAM/FELIX
Kintex-7 Ultrascale

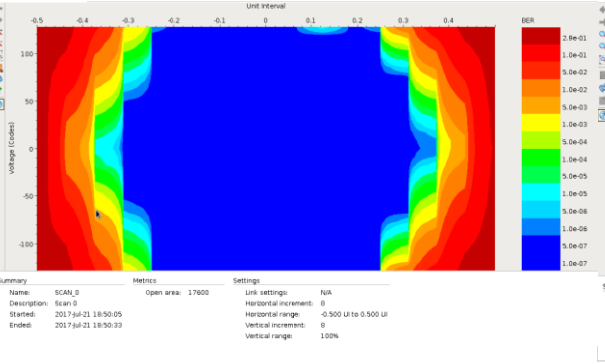
Downlink: 4.8 Gb/s
Multiples of RHIC clock (9.4 MHz)
Recover clock from 8b/10b

Optical Links

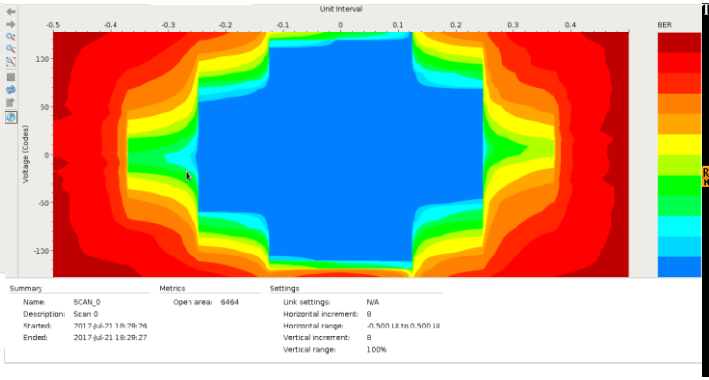
FEE
Atrix-7

Uplink: 4.8 Gb/s, fixed clock

Uplink iBERT @ DAM: 1.46e-13

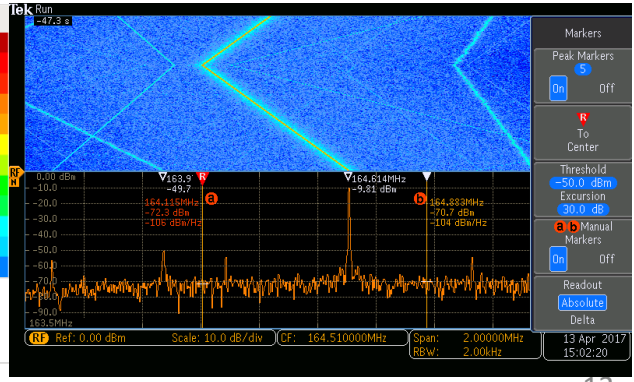


Downlink iBERT @ FEE: 1. 023e-13



Test recovered "RHIC" clock

Kintex 7 (eval board for now) -> Atrix 7 (eval board)



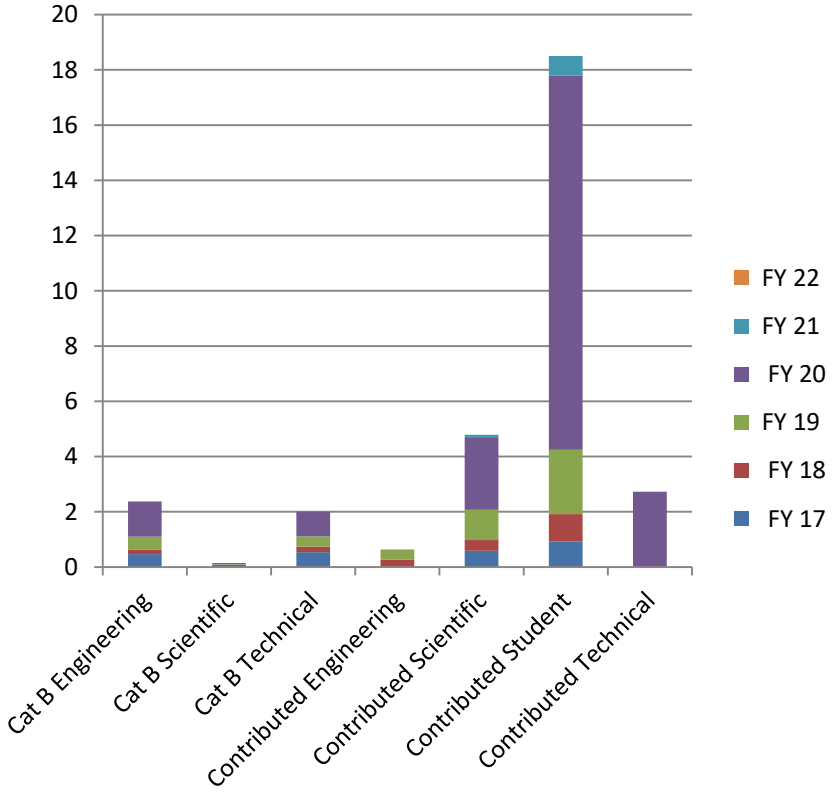
Summary

- Low risk in DAM hardware design: taking advantage of FELIX PCIe card, a DAQ development for ATLAS upgrade at BNL, and commodity computing
- Produced the cost and schedule for the TPC DAM (WBS 1.2.6) by bottom-up estimate
- Prototype test progress well
- Challenges:
  - **Reach the targeted data reduction factor, including implementing a reliable clustering algorithm in FELIX FPGA**
  - **Integration and system test with TPC FEEs and with sPHENIX DAQ prior to beam**

Back Up

Labor profile, TPC 1.2

- FTE Profile by Category



- FTE Profile by Fiscal Year

Row Labels	FY 17	FY 18	FY 19	FY 20	FY 21	FY 22
Cat B	**1.08**	**0.37**	**0.87**	**2.21**	**0.00**	**0.00**
Engineering	0.47	0.16	0.48	1.28	0.00	0.00
Scientific	0.07	0.01	0.02	0.04	0.00	0.00
Technical	0.54	0.20	0.37	0.89	0.00	0.00
Contributed	**1.51**	**1.65**	**3.78**	**18.92**	**0.79**	**0.00**
Engineering	0.00	0.27	0.36	0.00	0.00	0.00
Scientific	0.59	0.39	1.09	2.63	0.08	0.00
Student	0.92	0.99	2.33	13.56	0.70	0.00
Technical	0.00	0.00	0.00	2.73	0.00	0.00
Grand Total	**2.59**	**2.02**	**4.65**	**21.12**	**0.79**	**0.00**

This is sum manpower for all TPC 1.2 scopes.

Rate estimation

Table 3.3: Raw data rate estimate for sPHENIX TPC and ALICE TPC cases

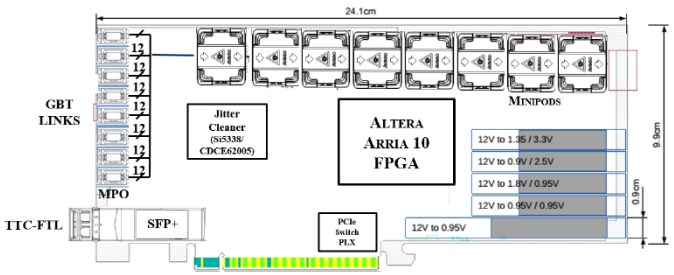
Parameters	sPHENIX (Au+Au 200 GeV)	ALICE (Pb+Pb 5.5 TeV)	Notes
dN/dy (Minbias) η coverage of TPC # of tracks in TPC	180 2.2 ($\lvert\eta\rvert$ <1.1) 396	500 1.8 ($\lvert\eta\rvert$ <0.9) 900	
Effective # of tracks in TPC (accounted for r-dep. η coverage change)	560	1690	note 1
Effective factor for track # increase for accounting albedo background	2	2	note 2
# of measurements in r # of samples in ϕ # of samples in timing # of bits of each sample	40 3 5 10	159 2 10 10	$\phi\times$time$\sim$20 bins for ALICE (from TDR)
Data volume increase factor by SAMPA header	1.4	1.4	Absolute maximum
Data volume/event (bits) Data volume/event (bytes)	9.41×10^{6} 1.18×10^{6}	1.50×10^{8} 1.88×10^{7}	note 3
Collision rate [kHz]	100	50	
Total data rate (bits/sec) Total data rate (bytes/sec)	9.41×10^{11} 1.18×10^{11}	7.52×10^{12} 9.41×10^{11}	

note 1: ALICE didn't estimate from first principle. We estimated for them.
note 2: We doubled the number of tracks to account for the background, based on STAR's experience.
note 3: Product of the previous seven rows. ALICE estimated the data volume as 160 Mbits/evt.

Table 3.4: TPC DAM and EBDC rate estimation

	Unit count	Rate per unit	Total rate	Assumptions and comments
Data on FEE Fibers	600 fibers	1.6 Gbps	940 Gbps	100kHz Au+Au collision assumed. Rate is radial position dependent. The max data rate is 2 Gbps for the inner-radius FEEs.
Data in BCO-buckets	24 DAMs	40 Gbps	970 Gbps	Unpack SAMPA data and add two 10-bit header per wavelet
After triggering	24 DAMs	11 Gbps	280 Gbps	Event builder collect 170-BCO buckets of hits after each trigger. This reduce data to 29%
After clustering	24 DAMs	5.7 Gbps	140 Gbps	Cluster finding and fitting on DAM FPGA. Expecting a reduction of total data volume to 50% based on STAR and ALICE experience.
After compression	24 EBDCs	3.4 Gbps	80 Gbps	Lossless compression on EBDC CPUs. Assuming the PHENIX experience of a reduction of total data volume to 60%
Buffer box data logging	Buffer box system	80 Gbps	80 Gbps	Logging TPC data to disk in buffer box system in sPHENIX counting house.

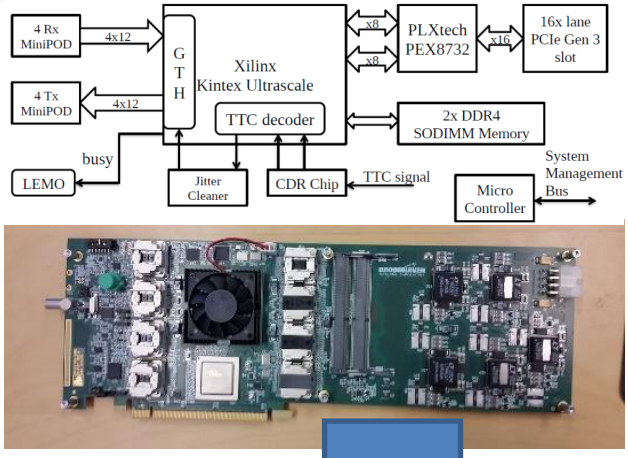
Comparing to CRU/PCIe40



(b) PCIe40 Schematic.

(a) PCie40.

CRU/ PCIe40



FELIX

FPGA Family Name	Xilinx Virtex 6	Altera Stratix V GX	Xilinx Virtex 7	Altera Arria 10 GX **	Xilinx Virtex Ultrascale	Altera Stratix 10	CRU Requirements #	Xlinux Kintex Ultrascale
Status		available	available	ES available from Q2'15	available	end of 2017		**Available**
FPGA part number	XC6VLX240T	5SGXEA7	XC7VX690T	**10AX115**	XCVU190	10SG280		**XCKU115**
Used in	C-RORC	AMC40	MP7	**PCIe40**				**BNL 711, FELIX v1.5 prototype**
Logic Elements / Cells [M]	0.241	0.622	0.693	1.15	1.9	2.8		**1.451**
FFs [M]	0.3	0.939	0.866	1.7	2.14			**1.3**
LUTs [M]	0.15	0.235	0.433	0.425	1.07			**0.66**
18/20 Kb RAM Blocks	832	2560	2940	**2713**	7560	11721	**1920 / 2560**	**4320**
Total Block RAM (Mb)	15	50	53	**53**	133	229	**40 / 53**	**75.9**
≥ 10 Gb/s Transeivers	24	48	80	**96**	60	144	**48**	**(48 input + 48 output fiber links in FELIX)**
PLLs	12	28	20	32	60	48		**48**
PCIe x8, Gen3	2 (Gen2)	4	3	4	6	6		**6**

TPC Detector is the majority user (>70%) of CRU boards. CRU requirements is measured against TPC detector specific logic occupancy.

** Altough the maximum number of links of the Arria10 family is 96 links, the FPGA equiping the PCIe40 board has only 72 links

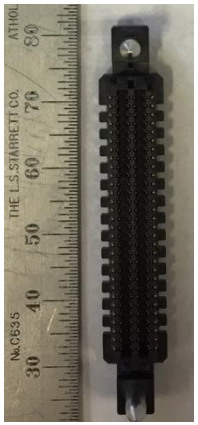
ATLAS group estimated 48x GBP unpacking and PCIe output use ~20% FELIX Resource

Status and Highlights (II)

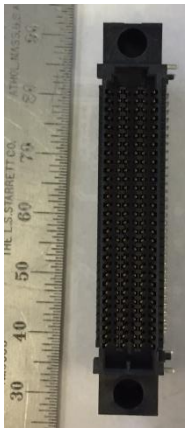
- Design of full-scale prototype is in progress.
- Full-scale prototype design will be passed to board routing as soon as we finished evaluating basic features of SAMPA with small-scale prototype
- Selecting of peripheral parts are almost done.

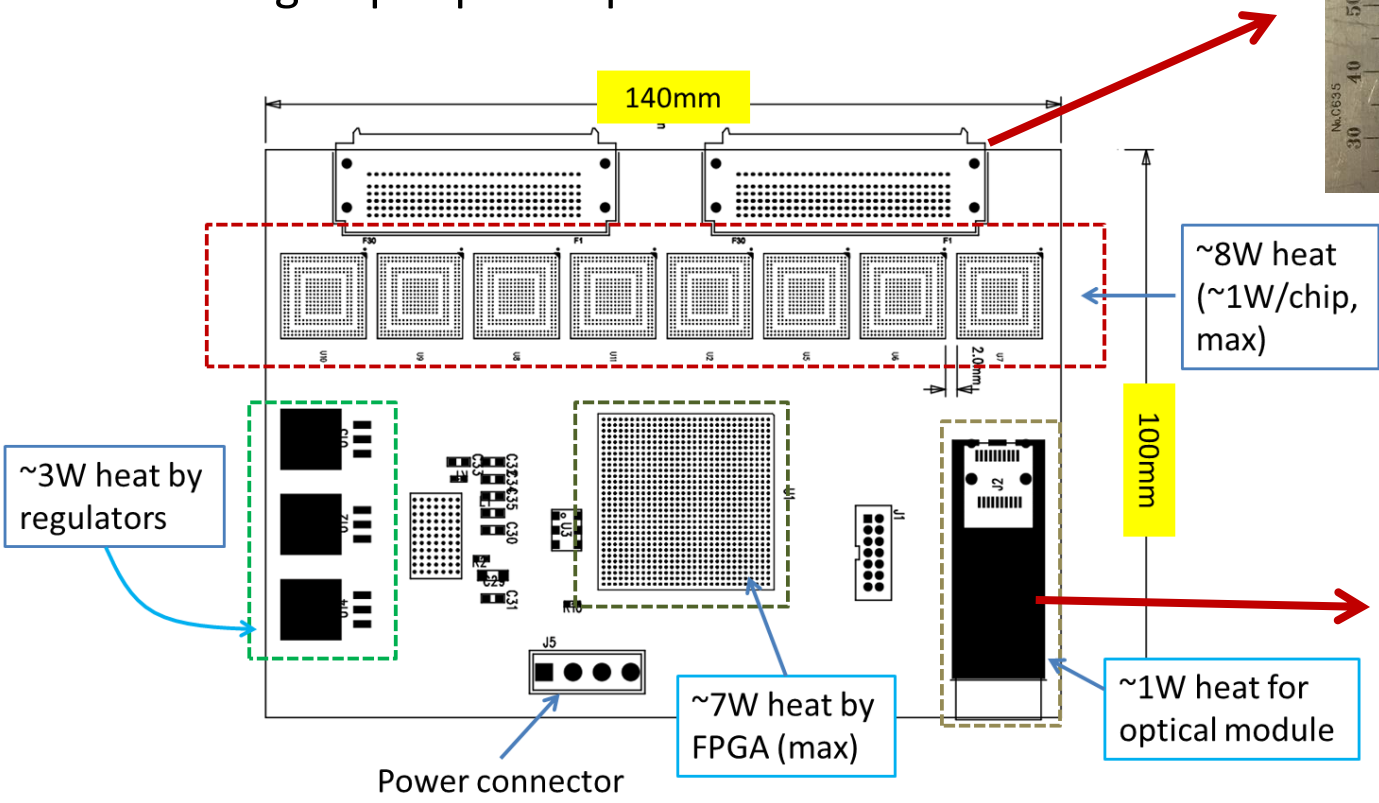
Signal connectors

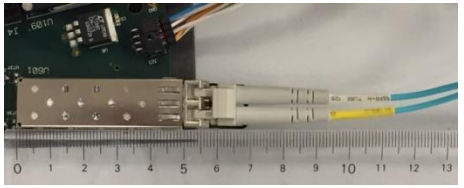
Padplane side



FEE side





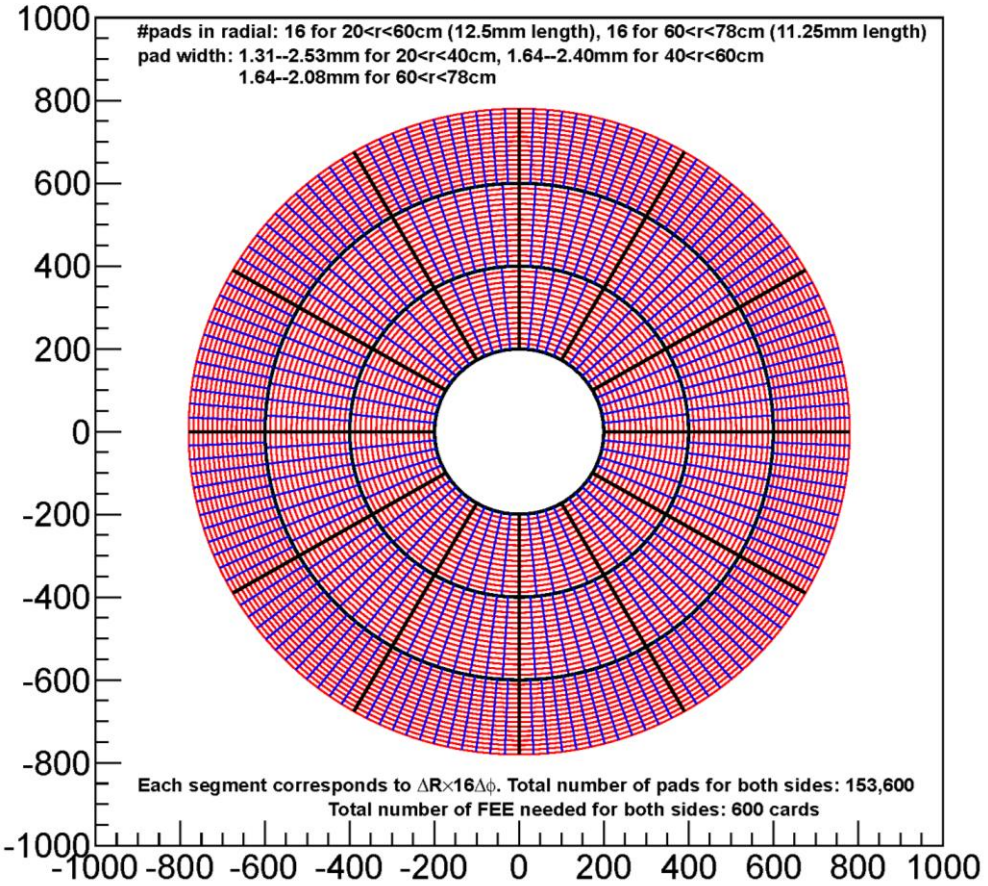


Padplane layout

- New pad layout (30<r<78cm)
  - **Three segments in radial direction, each divided into 16 (8 for 30<r<40cm)**
  - **12 segments in phi direction, each divided into multiple of 16**
  - **Matching to number of input to a FEE**
  - **Each cell in the right figure corresponds to 16 pads in phi**
- Variable pad size as a function of radial position
- Total 153,600 pads for both side
  - **600 FEE cards**
- Data Rate (no header included)
  - **1.42Gbps/board for 30<r<40cm**
  - **1.45Gbps/board for 40<r<60cm**
  - **0.77Gbps/board for 60<r<80cm**
  - **→ 28Gbps/(1/12 full azimuth)**

5 FEEs for 30<r<40cm, 8 for 40<r<60cm, 12 for 60<r<78cm, for each 1/12 of full azimuth

Each cell = 16pads in phi

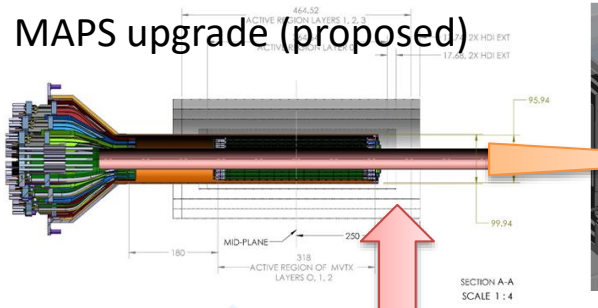


Data rate calculation

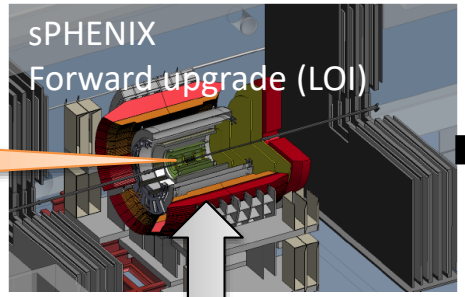
- Raw data (100% duty factor is assumed)
  - **Sampling rate in z-direction: 10MHz (= 100nsec)**
  - **Pulse peaking time is 160nsec (fixed from SAMPA's specification), which leads to ~350nsec for whole pulse shape.**
    - **More than 4 samples in timing (z) direction is necessary. We decided on taking 5 samples including pre-signal**
  - **One cluster will be spread over 3 pads in r-ϕ plane**
    - **Coming from the characteristics of the Ne2K (Ne - CF_4 - iC_4H_{10}: 95% - 3% - 2%) gas**
  - **We measure 40 clusters for one track**
  - **Each sample is 10 bits: 40 clusters * 15 * 10 bits = 6 Kbits/track**
  - **800 tracks per event: 6Kbits/track * 800 = 4.8 Mbits/event**
    - **This number doesn't take eta-dependent acceptance change of TPC into account**
  - **At 100 KHz: 4.8 Mbits/event * 100 KHz = 480 Gbits/s**
- With header of SAMPA (40% increase at maximum): 670Gbits/s
  - **With eta-dependent acceptance change: 940Gbits/s**

Advanced DAQ for RHIC and eRHIC

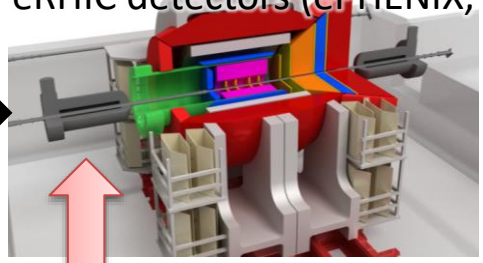
MAPS upgrade (proposed)



sPHENIX Forward upgrade (LOI)



eRHIC detectors (ePHENIX, BeAST, ...)



Deliver to FEEs:
Timing with 10-500 MHz beam clock, Slow control, O(1000) links

Advanced DAQ for RHIC and eRHIC

Trigger-less, O(1000) 10-Gbps bi-directional links, FPGA-based data reduction, Connect customized FEE to commodity computing

Data downlinks:
O(100k) ADC channels @ 10-100 MHz
O(100M) Pixels channels
O(100 Tbps) from FEE before reduction
O(100 Gbps) to disk after FPGA+CPU reduction

RHIC/eRHIC Timing

Online Farm

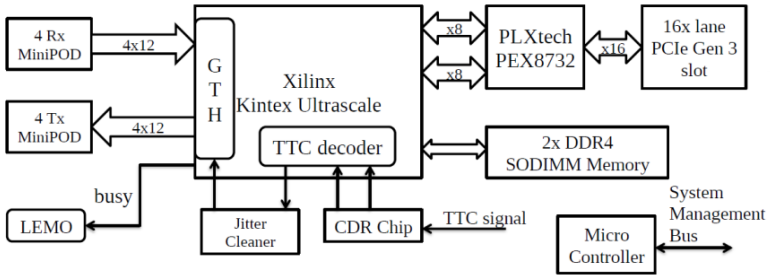
Data Storage

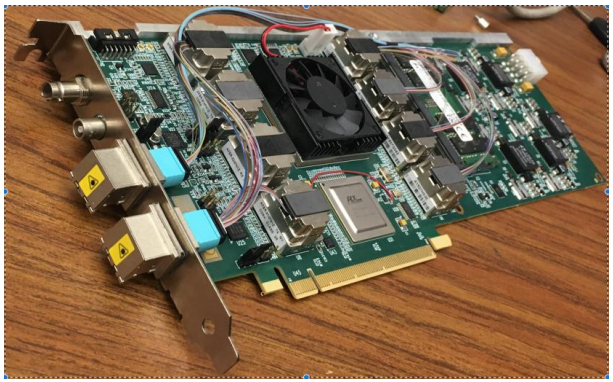
Jin Huang <jhuang@bnl.gov>

ATLAS/FELIX BNL-711 PCIe Card

Credit: Kai Chen (BNL), https://indico.bnl.gov/conferenceDisplay.py?confId=2653

- BNL-711 Board chosen for ATLAS FELIX project, and used in ATLAS phase I upgrade, which is projected to complete before sPHENIX.
- Readout for ATLAS Phase-I sub-system of Liquid Argon Calorimeter, Level-1 calorimeter trigger, New small wheel of the muon spectrometer

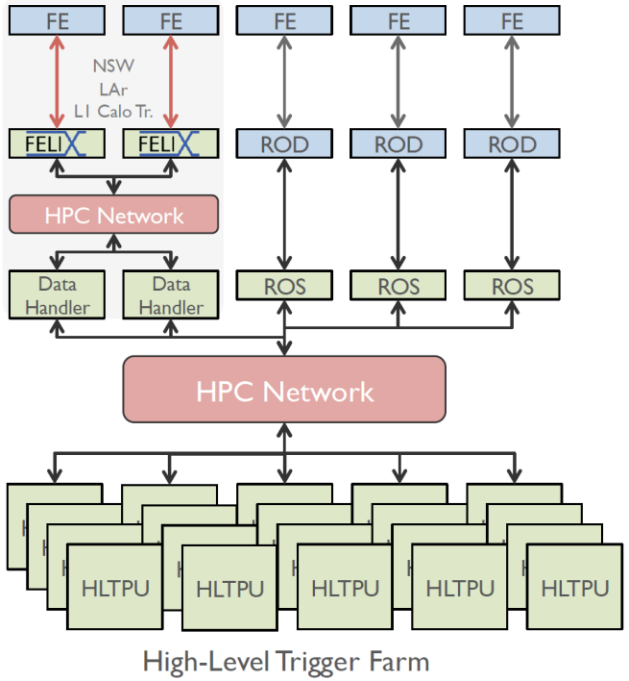




Versatile Link, GBT (GigaBit Transceiver)

PCs

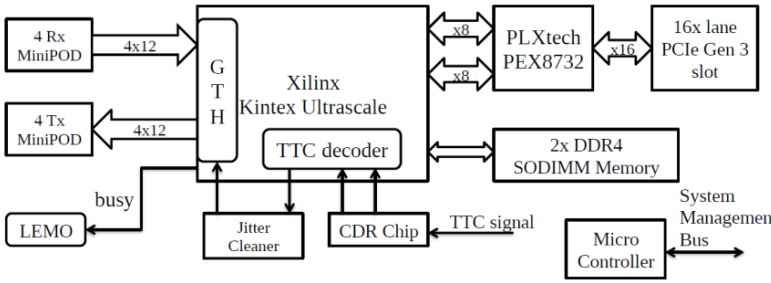
40 Gb Ethernet, Infiniband



ATLAS/FELIX Card for sPHENIX?

Credit: Kai Chen (BNL), https://indico.bnl.gov/conferenceDisplay.py?confId=2653

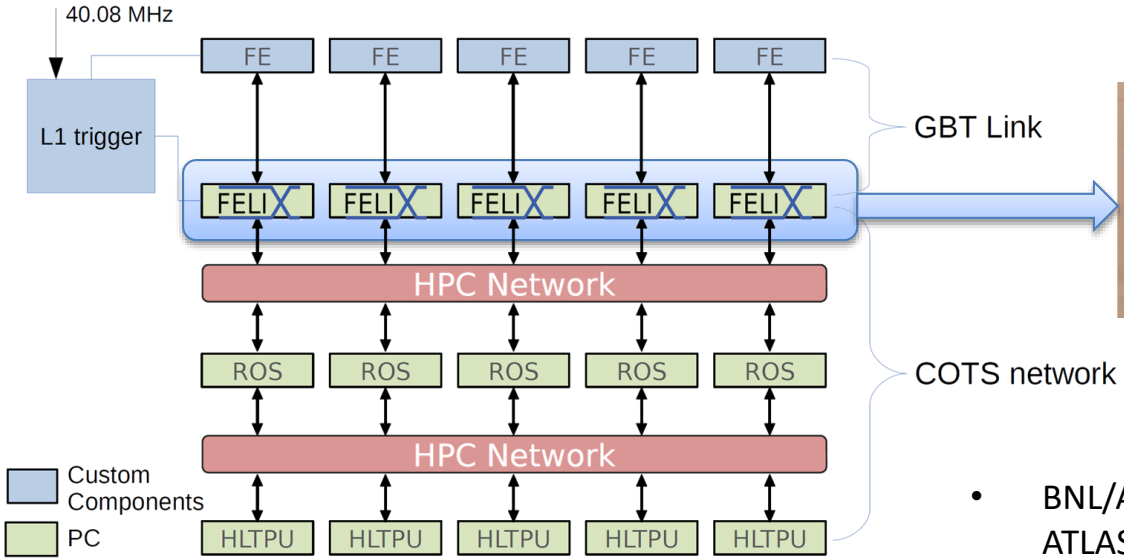
- Main features for FELIX PCIe Card
  - **Design: BNL/Omega group, Layout: BNL/Instrumentation, Goal: multiple users.**
  - **A large Kintex Ultrascale FPGA, 1.5 M Logical Cells (24x Logical Cells of FVTX FEM card)**
  - **48 bi-directional GBT link via two 48-F MTP connectors**
  - **PCIex16 Gen3, 101 Gbps demonstrated**
  - **2x DDR4 memory slots (v1.0, v1.5), removed v2.0**
  - **TTC-timing input (v1.0, v1.5), timing mezzanine card (v2.0)**
- Timeline and availability:
  - **Current version: v1.5 prototype, can be ordered now**
  - **Next version: v2.0 pre-production, design completed, layout on-going, expect available Oct 2017**
  - **FELIX production system delivery expected end 2018 for ATLAS Phase-I upgrade. ATLAS needing 100+ card with various flavor of firmware depending on subsystem configurations.**
- BNL/Omega group, Local expert expressed willing for help us to adapt FELIX in sPHENIX
  - **Boards for initial evaluation test**
  - **Support firmware software development, timing mezzanine card design**
  - **The team is also help in possible use of FELIX card in proto-Dune.**
  - **The FELIX team is open for inputs in guiding the design to be more generic to various users.**

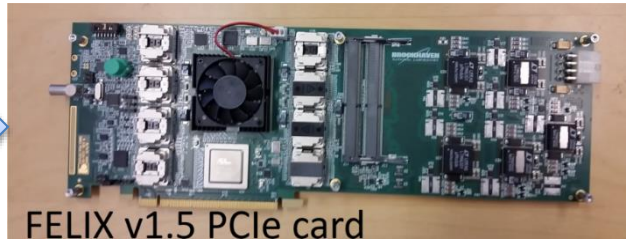


FELIX v1.5 Card in test stand

FELIX

ATLAS DAQ structure for mid-2020s: Front-End Link eXchange (FELIX)

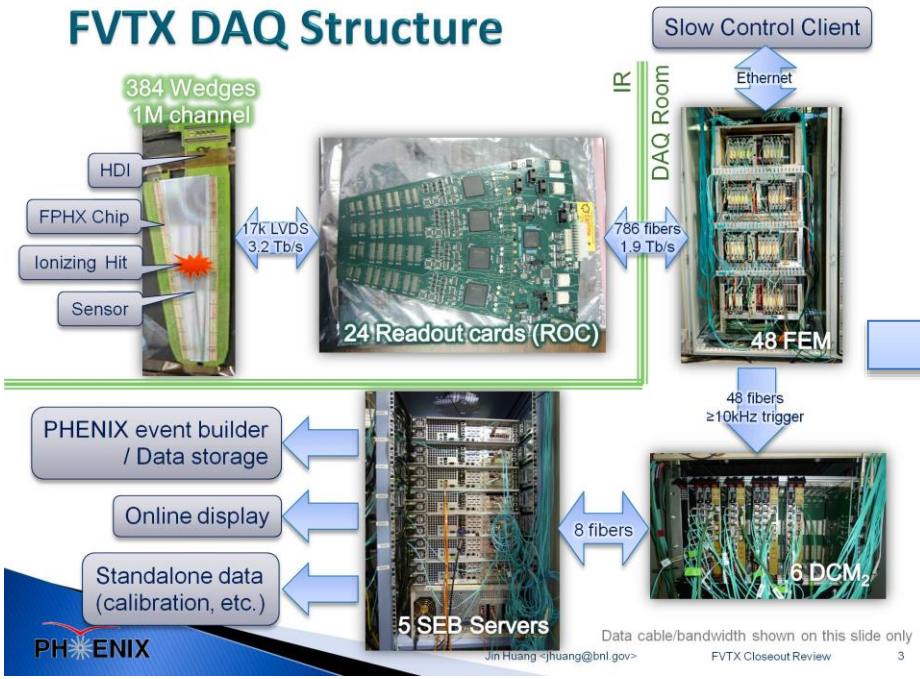




- Using high performance large-FPGA optical link card to bridge custom FEE and commodity computing
- Besides ATLAS, similar architecture also proposed for ALICE and LHCb upgrades

- BNL/ATLAS group is finalizing FELIX PCIe card for ATLAS DAQ upgrades for 2020s. Significant DAQ hardware R&D @ HEP..

Comparing to current RHIC trigger-less DAQ



2020s

2x (FELIX Card on commodity server)

- FVTX detector @ PHENIX carries one of most advanced DAQ @ RHIC, successful upgrade in 2012, continuous readout & triggering capability
- FELIX would reduce the five crates of custom DAQ electronics to just two FELIX PCIe cards in terms of FPGA resource and data process rate

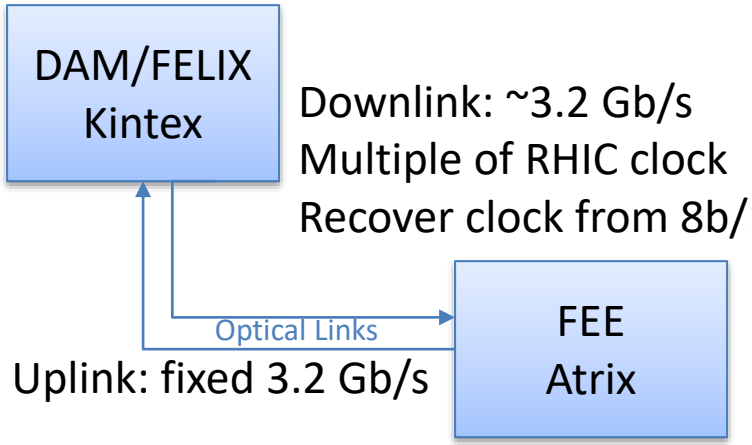
Schedule

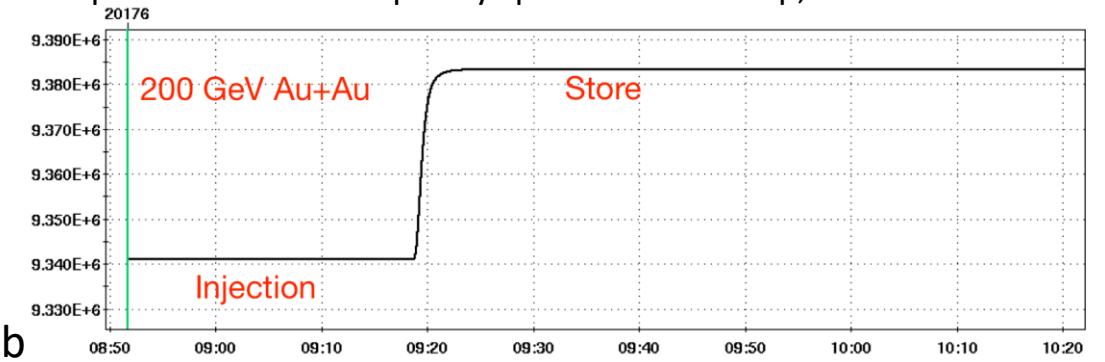
- Not on the critical path for TPC (1.2)
- Prior to CD-2:
  Schedule driven by FPGA and DAQ firmware software development
- Scheduling risk for FELIX card production is low:
  - **Already received v1.5 prototype card for the prototyping stage, 1.2.6.1**
  - **Well into final prototyping stage, producing pre-production card as speaking**
  - **Planned for production of ATLAS Phase-I upgrade (delivery end 2018)**
- Scheduling risk for EBDC server production is low:
  - **Commodity computing**
  - **Procurement scheduled at the latest stage of the production to take advantage of commercial computing development**

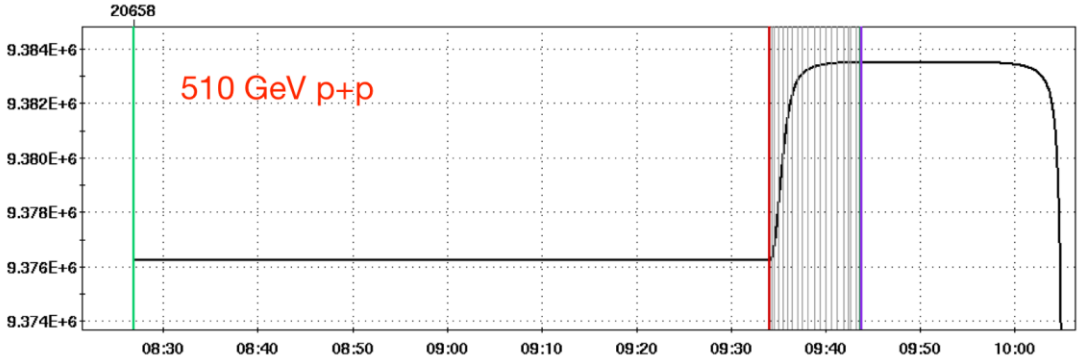
Kintex -> Atrix SFP+ fiber links with RHIC clock delivery

- One of the feature of the design is to use FELIX distribution slow control and RHIC clock to 25x FEE.
- Use RHIC clock (~9.4 MHz) as base frequency. Multiply x14 as fiber clock + slow control data in via 8b/10b encoder
- Recover RHIC clock on FEE, and slow control data via 8b/10b decoder
- John Kuczewski (BNL, instrumentation): tested with expected RHIC clock frequency spread (due to ramp). Excellent error rate

Special requirement: RHIC frequency spread due to ramp, 9.362 MHz ±22 kH







TPC Outlook and possible use in MAPS

- The TPC group acquired v1.5 FELIX PCIe card to setup a test stand and evaluate DAQ feasibility. Plan to switch to pre-production cards end 2017. Meanwhile, we would also want to learn to CRU, prior to final decision on the readout cards.
- After Ming's request, a v1.5 FELIX PCIe card has been manufactured for MVTX.
- It makes sense to try pursuing the same system for MAPS+TPC readout, and share production batch, DAQ expertise and effort in timing distribution, card/server pool, event-building software development