sPHENIX Director's Review
Calorimeter Digitizer

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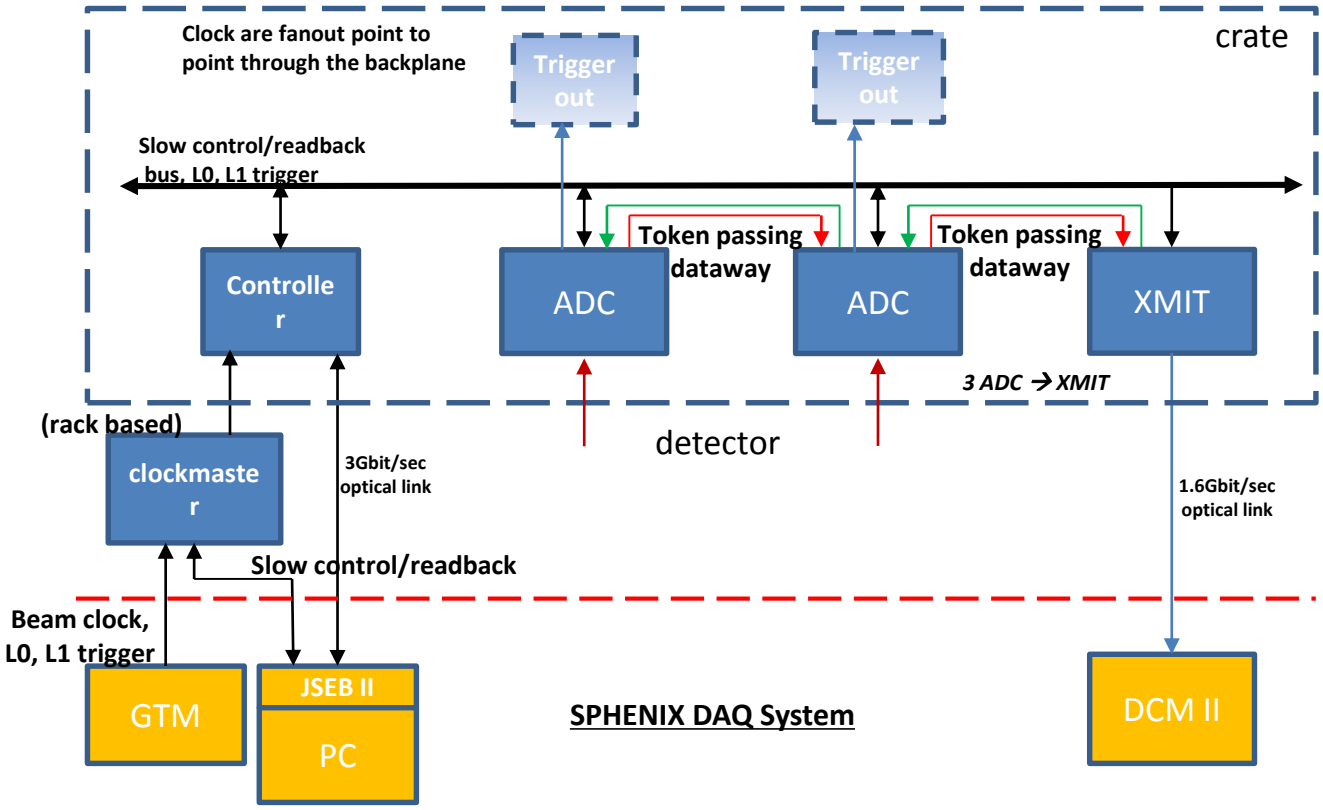
BNL

The Subsystem

- The calorimeter digitizer system
  - Off detector ADC system for both EM and Hadronic calorimeter.
  - Received the amplified signal from on-detector amplify through cables
  - Digitize the signal at 6x beam crossing rate, ~ 60 MHz, with 14 bits ADC
    - Offset the baseline to use most of the ADC range.
  - Provide at least 40 beam crossing of data buffers to cover L1 trigger latency
  - Provide Level 1 trigger primitives.
  - have at least 4 Level 1 events buffer.
    - Maximum 31 ADC samples per channel per events, 16 samples planned.
  - Up to 15 KHz Level 1 trigger rate.
  - Send Level 1 trigger events to the DAQ system.

The Subsystem Technical Overview



Crate based system.

Signals are cable from the on-detector electronics.

Digitized with 14 bit ADC.

Receive timing information the SPHENIX Granule Timing Module (GTM)

Generate L1 trigger primitives (not in the reference design)

Receive L1 trigger and send out L1 triggered event data to Data Collection Module II (DCMII).

Provide buffer for both the 40 beam crossing L1 delay buffer and 4 L1 triggered events

Scope

- The sub-system consists of
  - 432 ADC boards
    - 64 channel per board
      - EMCAL 24576 Channels, HCAL 3072 channels.
  - 144 XMIT modules
  - 36 crates
  - Power supplies
  - Up to 36 clock master modules

Subsystem Collaborators

- Currently we have only Columbia University handle this project.
  - BNL is helping integration and DAQ test.
  - Other groups can help us when the time ready for production or further long term testing.
- This is the 3rd ADC system we have done in the last 10 years.
  - The PHENIX HBD 60 MHz 12 bits ADC (48 channel per board).
  - The MicroBooNe PMT readout, 64 MHZ 12 bits system.
    - The difference for this ADC system are ADC baseline shifting, serial backplane pathway, trigger primitive generators and more channel in the same space

Schedule Drivers

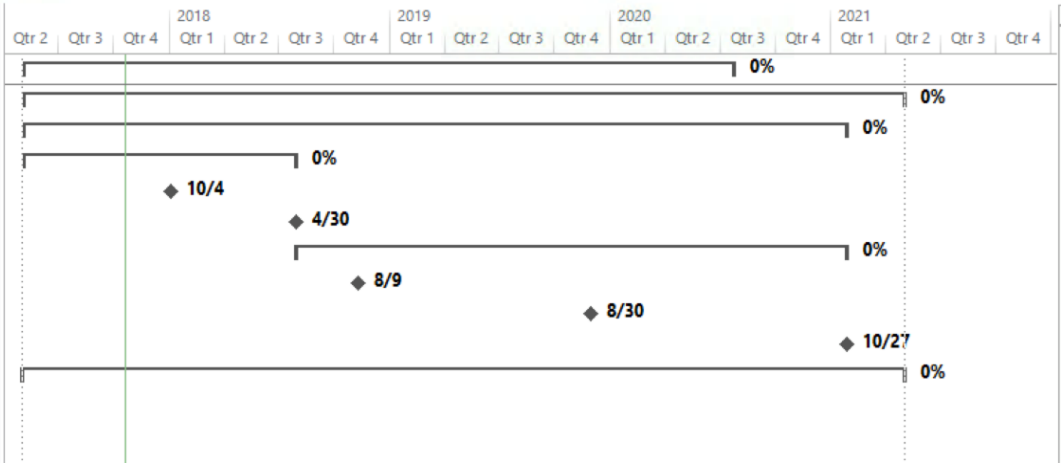
- The ADC system prototype works
  - Low Noise
  - ADC data unpack
  - Data buffering & trigger data readout
  - Trigger primitive path
- The electronics is off detector
  - Little detector mechanical constraint.
- If the testing with detector continues to be successful, we have not much schedule constraint.

Cost Drivers

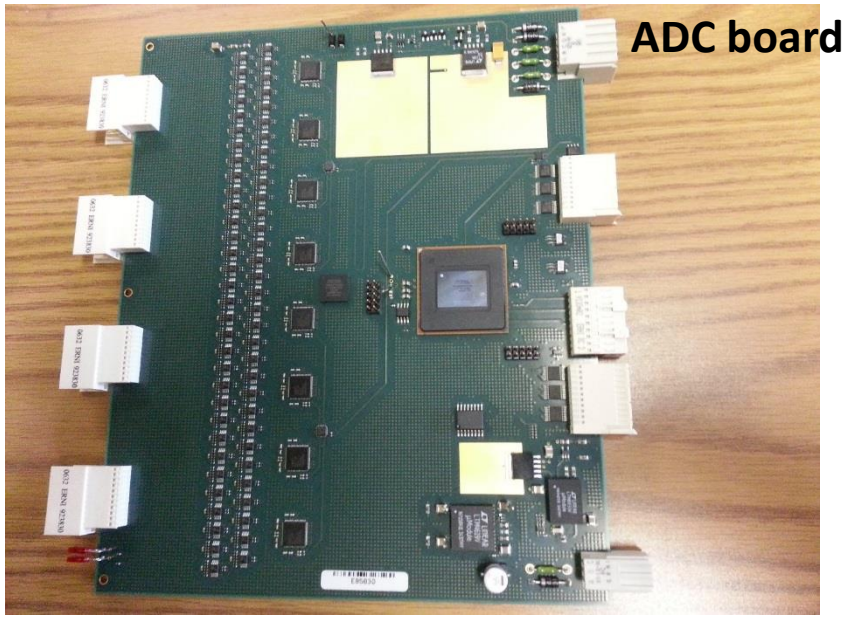
- The cost drivers are on the ADC board.
  - The 8 channel Analog Device ADC AD9257 ($84 per chip)
    - 64 channel board → 8 ADCs per board
  - The Altera Arria 5 FPGA ($322.10 per chip)
    - receive the ADC data and data manipulation, L1 delay, 5 events buffer and generating trigger primitives.
  - The differential receiver, AD8132 ($2.10 per chip)
    - Receiver the differential signals from the cable. One per channel.
  - The PCB board ($210 per board)
  - The PCB assembly ($285 per board)

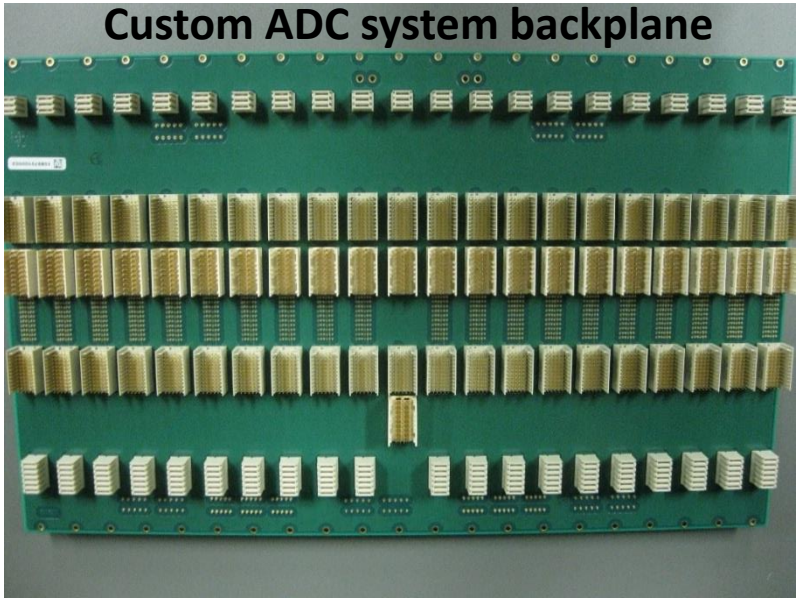
Basis of Estimate and Resource-Loaded Schedule

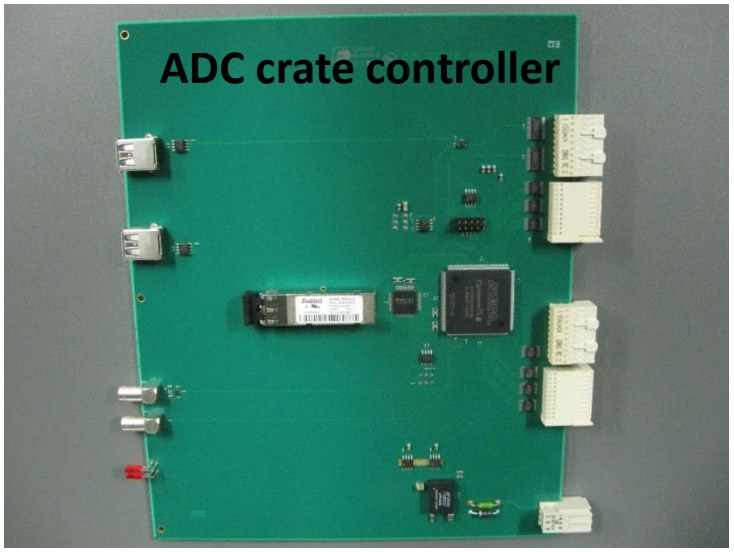
WBS	Task Name	Fixed_Cost_s
1.5.1	**Optical Sensors**	$1,095,500.
1.5.2	**Calorimeter Front End Electronics**	$1,684,900.
1.5.3	**Calorimeter Digitizer System**	$1,700,600.
1.5.3.1	**Calorimeter Digitizer: Preproduction Prototype**	$75,000.00
1.5.3.1.13	Calorimeter Digitizer Safety Review Complete	$0.00
1.5.3.1.19	Calorimeter Digitizer Preproduction Complete	$0.00
1.5.3.2	**Calorimeter Digitizers: Production**	$1,625,600.
1.5.3.2.12	Calorimeter Digitizer Readiness & Safety Review Complete	$0.00
1.5.3.2.14	Calorimeter Digitizer Procurement Start	$0.00
1.5.3.2.18	Calorimeter Digitizer Production Complete	$0.00
1.5.4	**Project Management**	$0.00

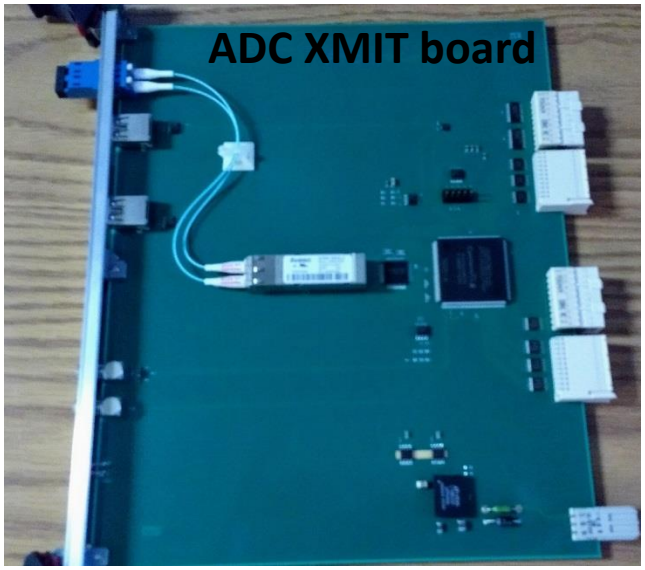


Status and Highlights





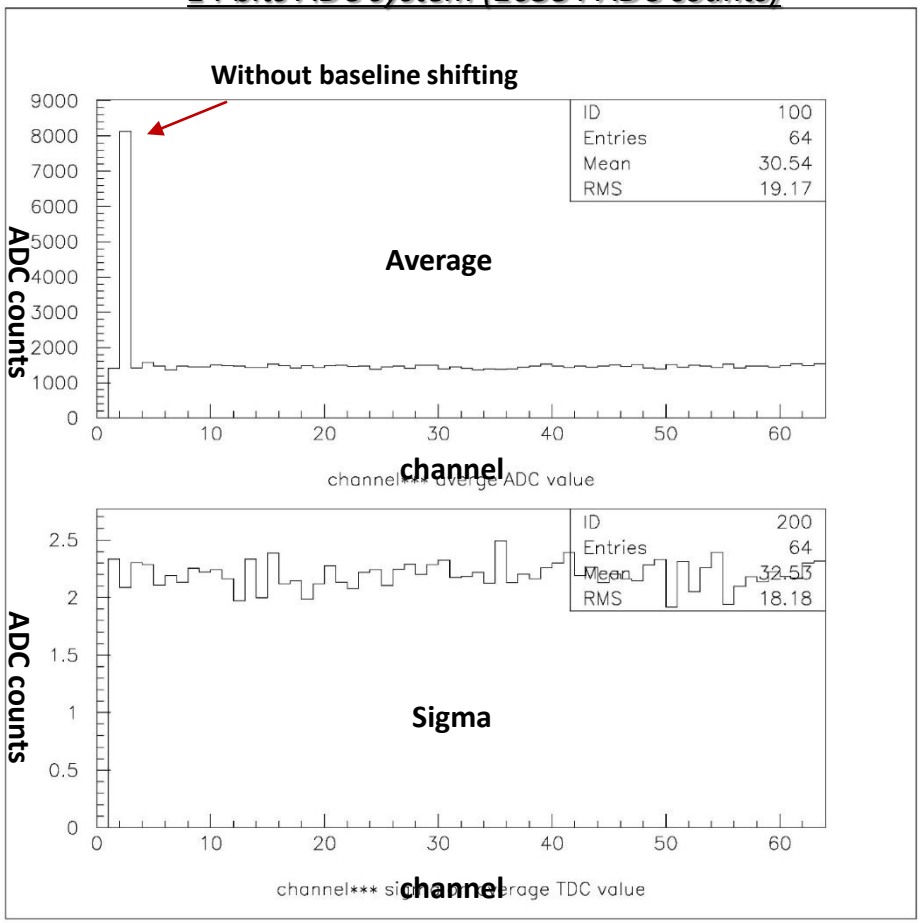




Status and Highlights

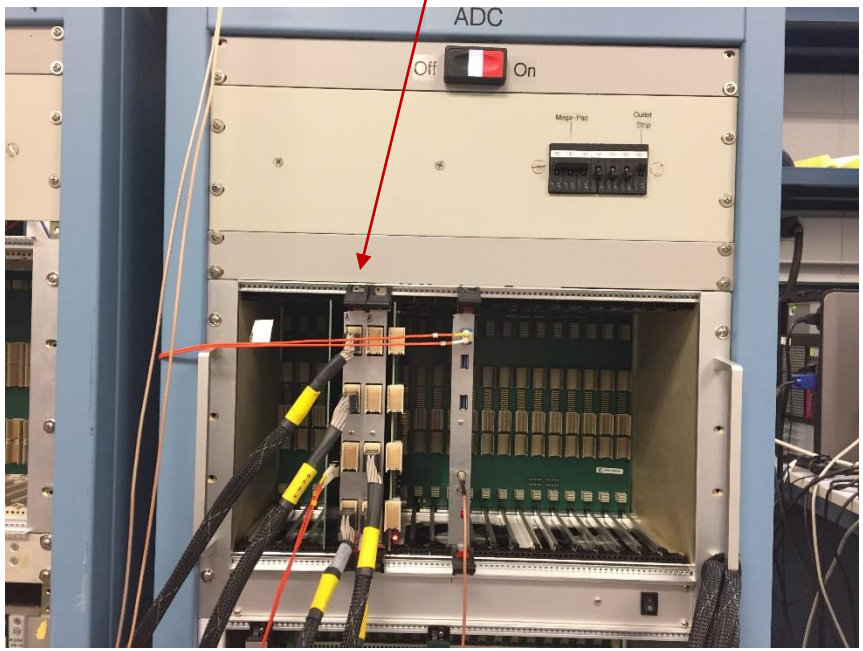
ADC baseline histogram (without signal cables)

14 bits ADC system (16384 ADC counts)



Test stand in BNL

3 ADCs boards



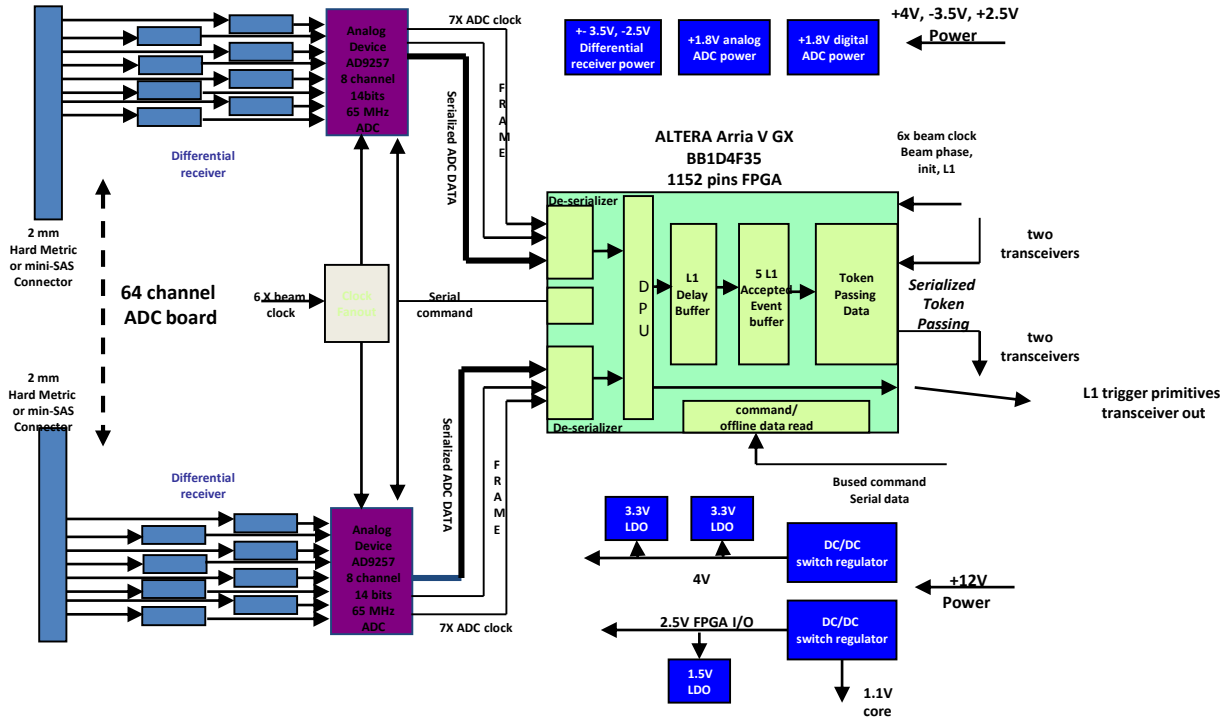
Summary

- We have construct first round of the digitizer system.
  - All first round prototype boards works so far.
    - ADC board has low analog noise.
    - Digital logics work so far
    - Trigger daughter card seems to work.
  - Some modification may be necessary when interface with sphenix timing system
    - Just affect the crate controller.
  - BNL test stands ongoing
    - Going reasonable well.
    - Fine tune tests will be done.

Back Up

sPHENIX ADC Module Block Diagram

RHIC beam clock 9.6MHz



The ADC system has 14 bits output (0- 16383 ADC counts)

The ADC input is differential, need to supply both + and – inputs (peak-peak range is 2V)

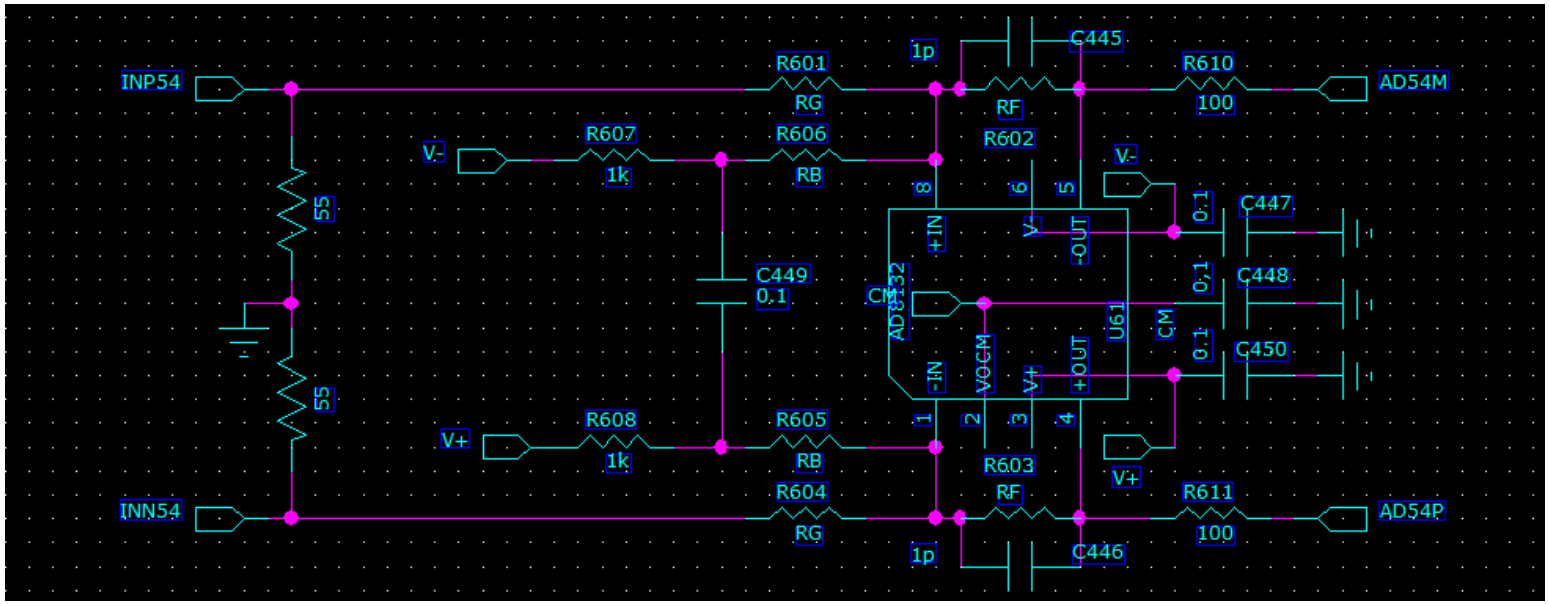
(122 μV per ADC counts)

+1V on the positive side and –1V on the negative side

8192 ADC count happened when V+, V- difference is zero

Our signal only swing one side

To get full range we need to offset the signals. → (the point to introduce the noise)

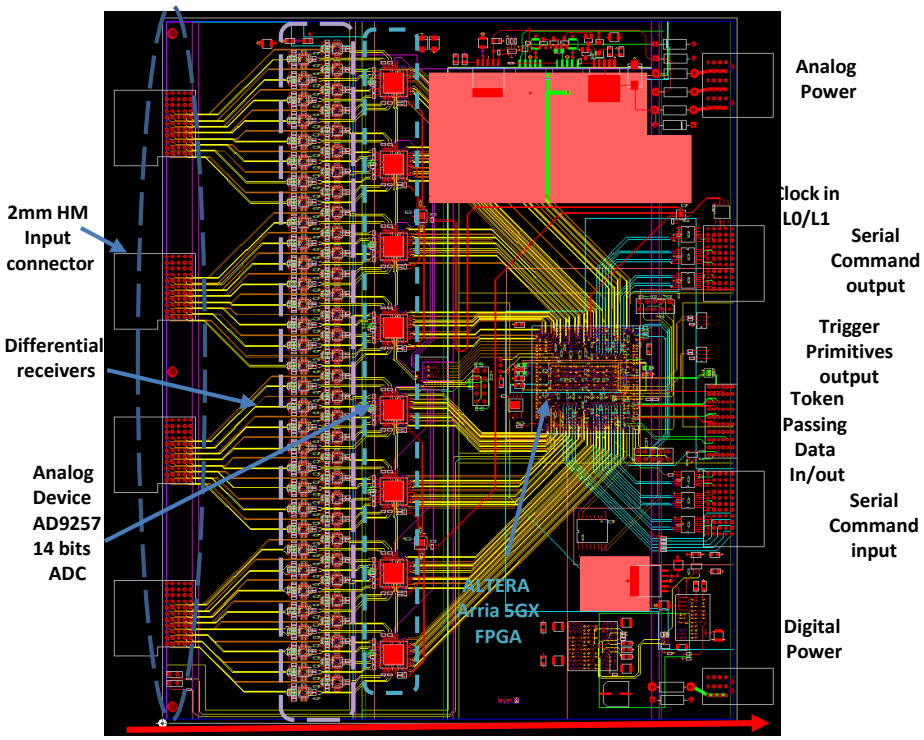


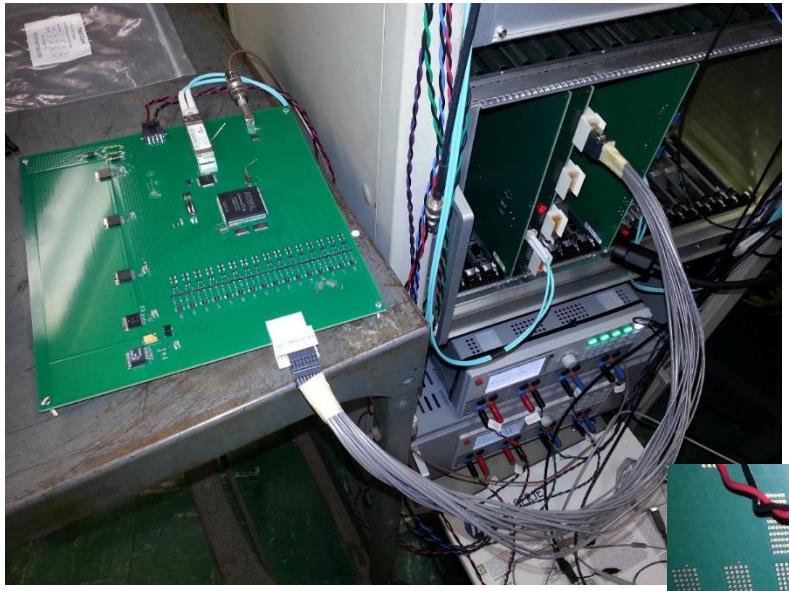
SPHENIX ADC board

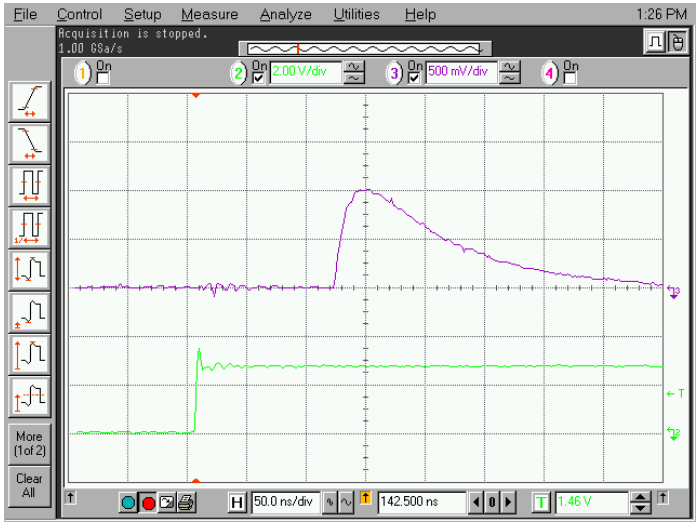
64 channel inputs
2mm HM connectors
160mm by 190mm (6U board)

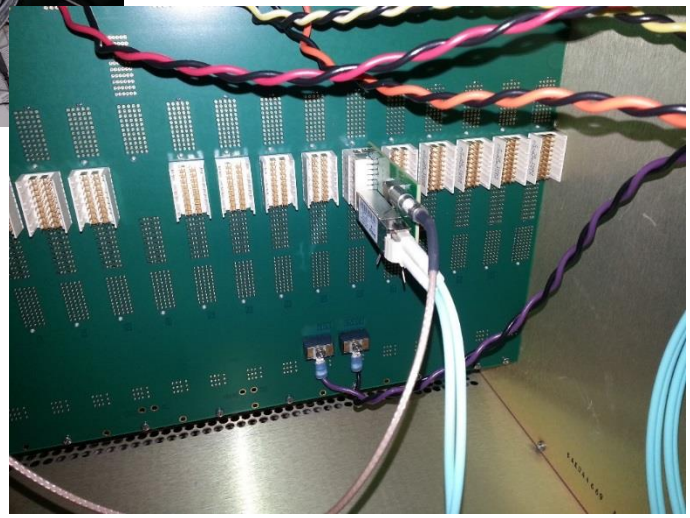
The 8 channel 14 bits ADC will be running at 6x beam crossing rate ~ 60 MHz

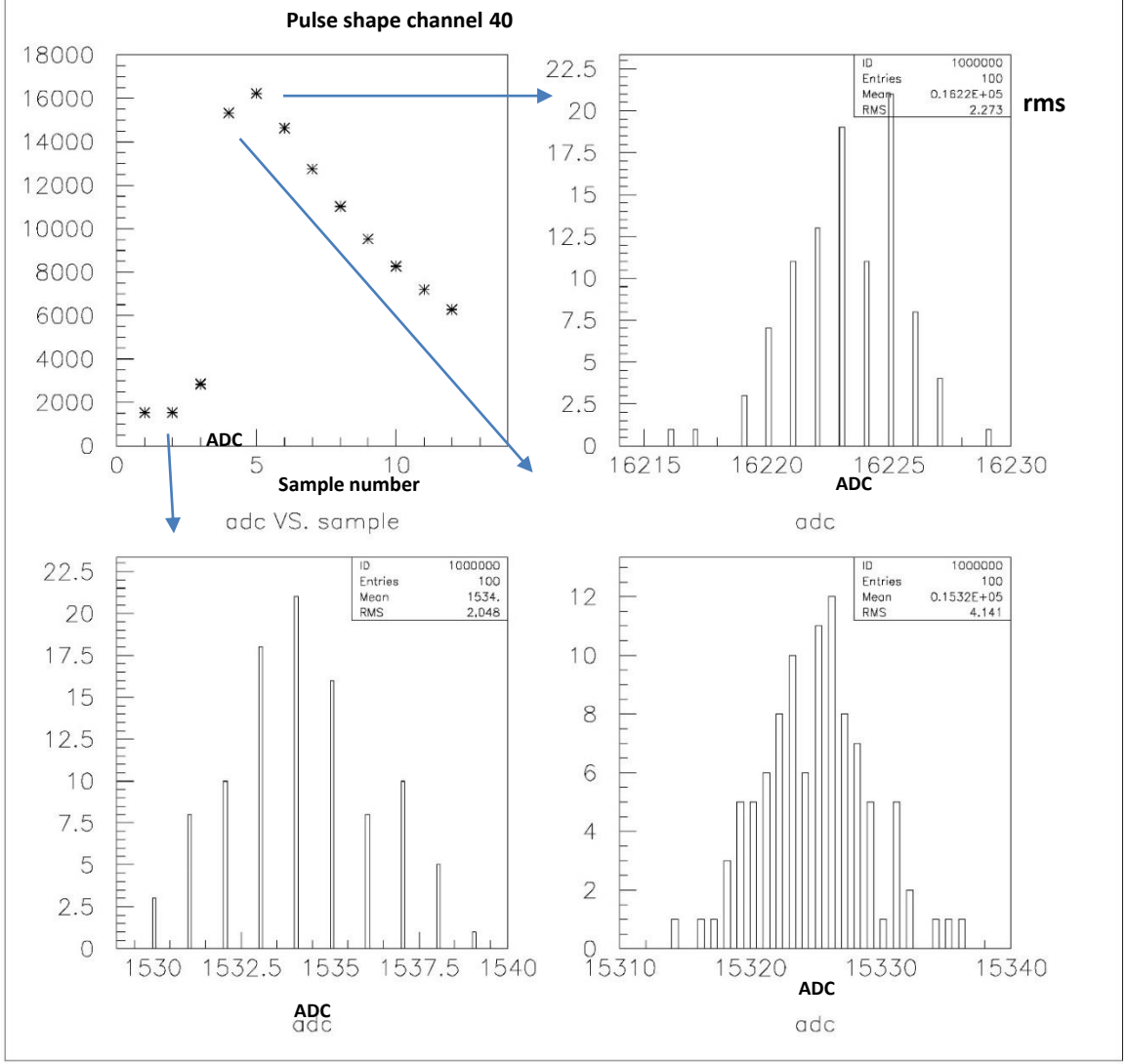
Altera Arria 5GX FPGA de-serialize data, provide 5 events buffer, 40 beam crossing L1 delay, token passing data, L1 trigger primitives output






File Control Setup Measure Analyze Utilities Help 1:26 PM
Acquisition is stopped.
1.00 GSa/s
2.00 V/div
500 mV/div
More (1of 2)
Clear All
50.0 ns/div
142.500 ns
1.46 V




Pulse shape channel 40
ADC
Sample number
adc VS. sample
rms
ID 1000000
Entries 100
Mean 0.1622E+05
RMS 2.273
ADC
adc
ID 1000000
Entries 100
Mean 1534.
RMS 2.048
ADC
adc
ID 1000000
Entries 100
Mean 0.1532E+05
RMS 4.141
ADC
adc